RELIABILITY REPORT

FOR

MAX11642EEG+T

PLASTIC ENCAPSULATED DEVICES

June 5, 2017

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

 Eric Wright Reliability Engineer	 Brian Standley Manager, Reliability

Conclusion

The MAX11642EEG+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX11638/MAX11639/MAX11642/MAX11643 are serial 8-bit analog-to-digital converters (ADCs) with an internal reference. These devices feature on-chip FIFO, scan mode, internal clock mode, internal averaging, and AutoShutdown(tm). The maximum sampling rate is 300ksps using an external clock. The MAX11642/MAX11643 have 16 input channels and the MAX11638/MAX11639 have 8 input channels. These four devices operate from either a +3V supply or a +5V supply, and contain a 10MHz SPI/QSPI(tm)/MICROWIRE®-compatible serial port. The MAX11638/MAX11639 are available in 16-pin QSOP packages. The MAX11642/MAX11643 are available in 24-pin QSOP packages. All four devices are specified over the extended -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	8-Bit, 16-/8-Channel, 300ksps ADCs with FIFO and Internal Reference
B. Process:	C6Y
C. Number of Device Transistors:	31874
D. Fabrication Location:	Japan
E. Assembly Location:	Philippines, Thailand
F. Date of Initial Production:	September 22, 2011

III. Packaging Information

A. Package Type:	24-pin QSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Bondwire:	Au (0.8 mil dia.)
E. Mold Material:	Epoxy with silica filler
F. Assembly Diagram:	#05-9000-4054
G. Flammability Rating:	Class UL94-V0
H. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
I. Single Layer Theta Ja:	105°C/W
J. Single Layer Theta Jc:	34°C/W
K. Multi Layer Theta Ja:	88°C/W
L. Multi Layer Theta Jc:	34°C/W

IV. Die Information

A. Dimensions:	90X130 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.6 microns (as drawn)
G. Isolation Dielectric:	SiO_2
H. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 4340 \times 495 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 0.43 \times 10^{-9}$

$\lambda = 0.43$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the C6Y Process results in a FIT Rate of 0.90 @ 25C and 15.55 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AC88 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1200V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX11642EEG+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 1000 hrs.	DC Parameters & functionality	495	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.