RELIABILITY REPORT

FOR

MAX11168EUB+T

PLASTIC ENCAPSULATED DEVICES

January 19, 2016

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Eric Wright
Quality Assurance
Reliability Engineer

Conclusion

The MAX11168EUB+ T successfully met the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX11168 is a 16-bit, 500ksps, SAR ADC offering excellent AC and DC performance with true bipolar input range, internal reference, and small size. The MAX11168 measures a ±5V (10VP-P) input range while operating from a single 5V supply. Patented charge-pump architecture allows direct sampling of high-impedance sources. The MAX11168 integrates a low drift reference with internal buffer, saving the cost and space of an external reference. This ADC achieves 92.3dB SNR and -101dB THD. The MAX11168 guarantees 16-bit no-missing codes and ±0.75 LSB INL (typ).
The MAX11168 communicates using an SPI-compatible serial interface at 2.5V, 3V, 3.3V, or 5V logic. The serial interface can be used to daisy-chain multiple ADCs for multichannel applications and provides a busy indicator option for simplified system synchronization and timing. The MAX11168 is offered in a 10-pin, 3mm x 5mm, µMAX package and is specified over the -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	16-Bit, 500ksps, ±5V SAR ADC with Internal Reference in µMAX
B. Process:	S45
C. Number of Device Transistors:	35573
D. Fabrication Location:	USA
E. Assembly Location:	USA, Philippines, Thailand
F. Date of Initial Production:	May 1, 2014

III. Packaging Information

A. Package Type:	10-pin µMax
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4678
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	180°C/W
K. Single Layer Theta Jc:	42°C/W
L. Multi Layer Theta Ja:	113.1°C/W
M. Multi Layer Theta Jc:	42°C/W

IV. Die Information

A. Dimensions:	62 X 87 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.4 microns (as drawn)
F. Minimum Metal Spacing:	0.6 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 79 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.9 \times 10^{-9}$

$\lambda = 13.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.04 @ 25°C and 0.69 @ 55°C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing

The AC91 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM: +/- 2500V per JEDEC JESD22-A114
ESD-CDM: +/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX11168EUB+ T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	79	0	T2UZBQ002B, D/C 1220

Note 1: Life Test Data may represent plastic DIP qualification lots.