

RELIABILITY REPORT
FOR
MAX11043ATL+
PLASTIC ENCAPSULATED DEVICES

April 26, 2010

MAXIM INTEGRATED PRODUCTS

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Approved by
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Conclusion

The MAX11043ATL+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description	V.Quality Assurance Information
II.Manufacturing Information	VI.Reliability Evaluation
III.Packaging Information	IV.Die Information
.....Attachments	

I. Device Description

A. General

The MAX11043 features 4 single-ended or differential channels of simultaneous-sampling ADCs with 16-bit resolution. The MAX11043 contains a versatile filter block and programmable-gain amplifier (PGA) per channel. The filter consists of seven cascaded 2nd-order filter sections for each channel, allowing the construction of a 14th-order filter. The filter coefficients are user-programmable. Configure each 2nd-order filter as lowpass (LP), highpass (HP), or bandpass (BP) with optional rectification. Gain and phase mismatch of the analog signal path is better than -50dB. The ADC can sample up to 800ksps per channel. A 40MHz serial interface provides communication to and from the device. The SPI(tm) interface provides through-put of 1600ksps; 4 channels at 400ksps per channel or 2 channels at 800ksps per channel. A software-selectable scan mode allows reading the ADC results while simultaneously updating the DAC. Other features of the MAX11043 include an internal (+2.5V) or external (+2.0V to +2.8V) reference, power-saving modes, and a PGA with gains of 1 to 64. The PGA includes an equalizer (EQ) function that automatically boosts low-amplitude, high-frequency signals for applications such as CW-chirp radar. The MAX11043 includes two 8-bit coarse DACs that set the high and low references for a second-stage 12-bit fine DAC, typically used for VCO control. Use software controls to write to the DAC or step the DAC up and down under hardware control in programmable steps. The device operates from a +3.0V to +3.6V supply. The MAX11043 is available in a 40-pin, 6mm x 6mm TQFN package and operates over the extended -40°C to +125°C temperature range.

II. Manufacturing Information

A. Description/Function:	4-Channel, 16-Bit, Simultaneous Sampling ADCs with PGA, Filter, and 8-/12-Bit Dual-Stage DAC
B. Process:	TS25EF
C. Number of Device Transistors:	318000
D. Fabrication Location:	Taiwan
E. Assembly Location:	Thailand
F. Date of Initial Production:	July 26, 2008

III. Packaging Information

A. Package Type:	40-pin TQFN 6x6
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3603
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	38°C/W
K. Single Layer Theta Jc:	1.4°C/W
L. Multi Layer Theta Ja:	27°C/W
M. Multi Layer Theta Jc:	1.4°C/W

IV. Die Information

A. Dimensions:	159 X 159 mils
B. Passivation:	HDP Oxide, Nitride
C. Interconnect:	Ti/TiN/AlCu/TiN
D. Backside Metallization:	None
E. Minimum Metal Width:	n/a
F. Minimum Metal Spacing:	n/a
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{408 \times 9706 \times 77 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 3.0 \times 10^{-9}$$

$\lambda = 3.0$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the TS25EF Process results in a FIT Rate of 1.0 @ 25C and 17.5 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The AC79 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX11043ATL+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 408 hrs.	DC Parameters & functionality	77	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data