



RELIABILITY REPORT  
FOR  
MAX105ECS+  
PLASTIC ENCAPSULATED DEVICES

January 21, 2010

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.  
SUNNYVALE, CA 94086

|                                   |
|-----------------------------------|
| <b>Approved by</b>                |
| Ken Wendel                        |
| Quality Assurance                 |
| Director, Reliability Engineering |

## Conclusion

The MAX105ECS+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents

|  |   |
|--|---|
| <b>I. ....Device Description</b>         | <b>V. ....Quality Assurance Information</b> |
| <b>II. ....Manufacturing Information</b> | <b>VI. ....Reliability Evaluation</b>       |
| <b>III. ....Packaging Information</b>    | <b>IV. ....Die Information</b>              |
| <b>.....Attachments</b>                  |   |

### I. Device Description

#### A. General

The MAX105 is a dual, 6-bit, analog-to-digital converter (ADC) designed to allow fast and precise digitizing of in-phase (I) and quadrature (Q) baseband signals. The MAX105 converts the analog signals of both I and Q components to digital outputs at 800MSPS while achieving a signal-to-noise ratio (SNR) of typically 37dB with an input frequency of 200MHz, and an integral nonlinearity (INL) and differential nonlinearity (DNL) of  $\pm 0.25$  LSB. The MAX105 analog input preamplifiers feature a 400MHz, -0.5dB, and a 1.5GHz, -3dB analog input bandwidth. Matching channel-to-channel performance is typically 0.04dB gain, 0.1 LSB offset, and 0.2 degrees phase. Dynamic performance is 36.4dB signal-to-noise plus distortion (SINAD) with a 200MHz analog input signal and a sampling speed of 800MHz. A fully differential comparator design and encoding circuits reduce out-of-sequence errors, and ensure excellent metastable performance of only one error per 1016 clock cycles. In addition, the MAX105 provides LVDS digital outputs with an internal 6:12 demultiplexer that reduces the output data rate to one-half the sample clock rate. Data is output in two's complement format. The MAX105 operates from a +5V analog supply and the LVDS output ports operate at +3.3V. The data converter's typical power dissipation is 2.6W. The device is packaged in an 80-pin, TQFP package with exposed paddle, and is specified for the extended (-40° C to +85° C) temperature range. For a lower-speed, 400MSPS version of the MAX105, please refer to the MAX107 data sheet.

## II. Manufacturing Information

|                                  |   |
|----------------------------------|---|
| A. Description/Function:         | Dual, 6-Bit, 800Msps ADC with On-Chip, Wideband Input Amplifier |
| B. Process:                      | GST2  |
| C. Number of Device Transistors: |   |
| D. Fabrication Location:         | Oregon  |
| E. Assembly Location:            | Korea   |
| F. Date of Initial Production:   | April 28, 2001  |

## III. Packaging Information

|  |                          |
|--|--------------------------|
| A. Package Type:   | 80-pin TQFP              |
| B. Lead Frame:   | Copper                   |
| C. Lead Finish:  | 100% matte Tin           |
| D. Die Attach:   | Conductive               |
| E. Bondwire:   | Au (1.2 mil dia.)        |
| F. Mold Material:  | Epoxy with silica filler |
| G. Assembly Diagram:   | #05-7001-0501            |
| H. Flammability Rating:  | Class UL94-V0            |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 3                  |
| J. Multi Layer Theta Ja:   | 28°C/W                   |
| K. Multi Layer Theta Jc:   | 2°C/W                    |

## IV. Die Information

|                            |  |
|----------------------------|--|
| A. Dimensions:             | 150 X 149 mils                                   |
| B. Passivation:            | Si <sub>3</sub> N <sub>4</sub> (Silicon nitride) |
| C. Interconnect:           | Au   |
| D. Backside Metallization: | None   |
| E. Minimum Metal Width:    | 2 microns (as drawn)                             |
| F. Minimum Metal Spacing:  | 2 microns (as drawn)                             |
| G. Bondpad Dimensions:     | 5 mil. Sq.                                       |
| H. Isolation Dielectric:   | SiO <sub>2</sub>                                 |
| I. Die Separation Method:  | Wafer Saw  |

## V. Quality Assurance Information

- |                                   |   |
|-----------------------------------|---|
| A. Quality Assurance Contacts:    | Ken Wendel (Director, Reliability Engineering)<br>Bryan Preeshl (Managing Director of QA)       |
| B. Outgoing Inspection Level:     | 0.1% for all electrical parameters guaranteed by the Datasheet.<br>0.1% For all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm  |
| D. Sampling Plan:                 | Mil-Std-105D  |

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 10.7 \times 10^{-9}$$
$$\lambda = 10.7 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the GST2 Process results in a FIT Rate of 0.06 @ 25C and 1.10 @ 55C (0.8 eV, 60% UCL)

### B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

### C. E.S.D. and Latch-Up Testing

The AC28 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000 V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

**Table 1**  
Reliability Evaluation Test Results

**MAX105ECS+**

| TEST ITEM                         | TEST CONDITION                                    | FAILURE IDENTIFICATION        | SAMPLE SIZE | NUMBER OF FAILURES |
|-----------------------------------|---|-------------------------------|-------------|--------------------|
| <b>Static Life Test</b> (Note 1)  |   |                               |             |                    |
|                                   | Ta = 150°C<br>Biased<br>Time = 192 hrs.           | DC Parameters & functionality | 45          | 0                  |
| <b>Moisture Testing</b> (Note 2)  |   |                               |             |                    |
| HAST                              | Ta = 130°C<br>RH = 85%<br>Biased<br>Time = 96hrs. | DC Parameters & functionality | 77          | 0                  |
| <b>Mechanical Stress</b> (Note 2) |   |                               |             |                    |
| Temperature<br>Cycle              | -65°C/150°C<br>1000 Cycles<br>Method 1010         | DC Parameters & functionality | 77          | 0                  |

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data