

RELIABILITY REPORT  
FOR  
**LM4050xxxx**  
PLASTIC ENCAPSULATED DEVICES

August 23, 2006

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.  
SUNNYVALE, CA 94086

Written by

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Quality Assurance  
Manager, Reliability Operations

## Conclusion

The LM4050 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The LM4050 is a precision two-terminal, shuntmode, bandgap voltage reference available in fixed reverse breakdown voltages of 1.225V, 2.048V, 2.500V, 3.000V, 3.3V, 4.096V, and 5.000V. Ideal for space-critical applications, the LM4050 is offered in the subminiature 3-pin SC70 surface-mount packages (1.8mm x 1.8mm), 50% smaller than comparable devices in SOT23 surface-mount package (SOT23 versions are also available).

Laser-trimmed resistors ensure excellent initial accuracy. With a 50ppm/°C temperature coefficient, this device is offered in three grades of initial accuracy ranging from 0.1% to 0.5%. The LM4050 has a 60µA to 15mA shunt-current capability with low dynamic impedance, ensuring stable reverse breakdown voltage accuracy over a wide range of operating temperatures and currents. The LM4050 does not require an external stabilizing capacitor while ensuring stability with any capacitive loads.

The LM4050 specifications are guaranteed over the temperature range of -40°C to +125°C.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Reverse Current (cathode to anode)	20mA
Forward Current (anode to cathode)	10mA
Continuous Power Dissipation (TA = +70°C)	
3-Pin SC70 (derate 2.17mW/°C above +70°C)	174mW
3-Pin SOT23 (derate 4.01mW/°C above +70°C)	320mW
Operating Temperature Range	
LM4050/LM4051_E_ _ _	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

## II. Manufacturing Information

- A. Description/Function: 50ppm/°C Precision Micropower Shunt Voltage References with Multiple Reverse Breakdown Voltages
- B. Process: B12 (Standard 1.2 micron silicon gate CMOS)
- C. Number of Device Transistors: 60
- D. Fabrication Location: California or Oregon, USA
- E. Assembly Location: Malaysia, Philippines or USA
- F. Date of Initial Production: July, 2002

## III. Packaging Information

- |   |                            |                                |
|---|----------------------------|--------------------------------|
| A. Package Type:  | <b>3-Pin SOT23-3</b>       | <b>8-Pin SC70-3</b>            |
| B. Lead Frame:  | Copper                     | Alloy 42                       |
| C. Lead Finish:   | Solder Plate or 100% Matte | Solder Plate or 100% Matte Tin |
| D. Die Attach:  | Non-Conductive Epoxy       | Non-Conductive Epoxy           |
| E. Bondwire:  | Gold (1 mil dia.)          | Gold (1 mil dia.)              |
| F. Mold Material:   | Epoxy with silica filler   | Epoxy with silica filler       |
| G. Assembly Diagram:  | # 05-0901-0187             | # 05-0901-0188                 |
| H. Flammability Rating:   | Class UL94-V0              | Class UL94-V0                  |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: | Level 1                    | Level 1                        |

## IV. Die Information

- A. Dimensions: 30 x 31 mils
- B. Passivation:  $\text{Si}_3\text{N}_4/\text{SiO}_2$  (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Aluminum/Si (Si = 1%)
- D. Backside Metallization: None
- E. Minimum Metal Width: 1.2 microns (as drawn)
- F. Minimum Metal Spacing: 1.2 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric:  $\text{SiO}_2$
- I. Die Separation Method: Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)  
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 155 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

△ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 7.09 \times 10^{-9}$$

$$\lambda = 7.09 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Attached Burn-In Schematic (Spec. # 06-5502) shows the static Burn-In circuit. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the B12/S12 Process results in a FIT rate of 0.10 @ 25°C and 1.78 @ 55°C (eV = 0.8, UCL = 60%).

### B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

### C. E.S.D. and Latch-Up Testing

The RF25-1 die type has been found to have all pins able to withstand a transient pulse of  $\pm 1000\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**LM4050xxxx**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test (Note 1)</b>					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		155	0
<b>Moisture Testing (Note 2)</b>					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SC70	77	0
			SOT	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress (Note 2)</b>					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ <u>3/</u>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

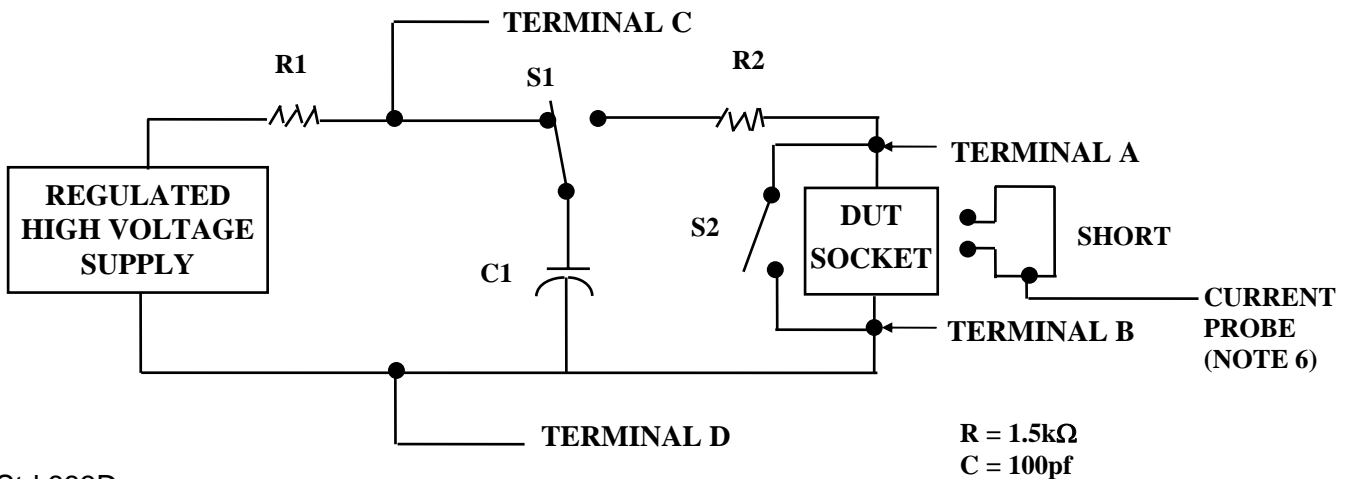
2/ No connects are not to be tested.

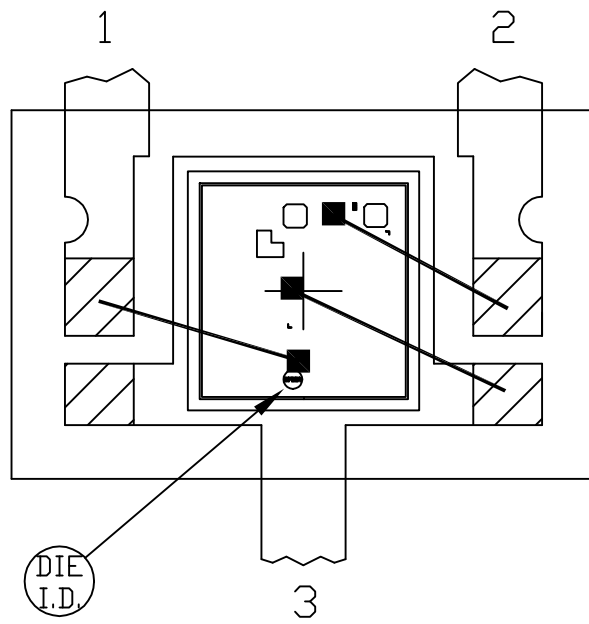
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

3.4 Pin combinations to be tested.

- Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





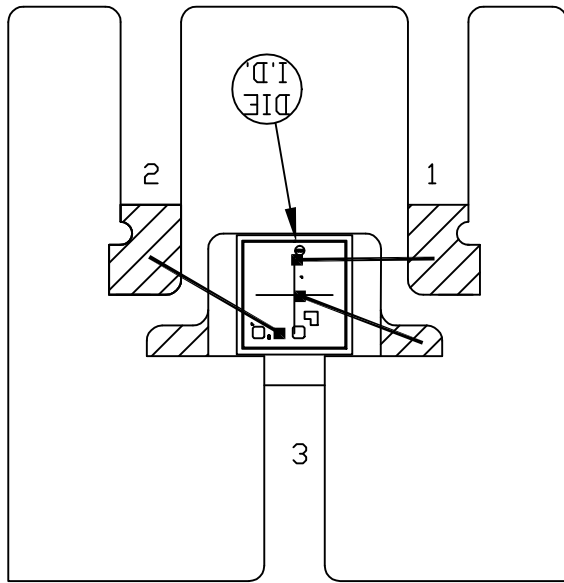
USE NON-CONDUCTIVE EPOXY

SCALE: 40x

CAVITY DOWN

 BONDABLE AREA

PKG. CODE: X3-2		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 34x35	PKG. DESIGN			BOND DIAGRAM #: 05-0901-0188	REV: A



USE NON-CONDUCTIVE EPOXY



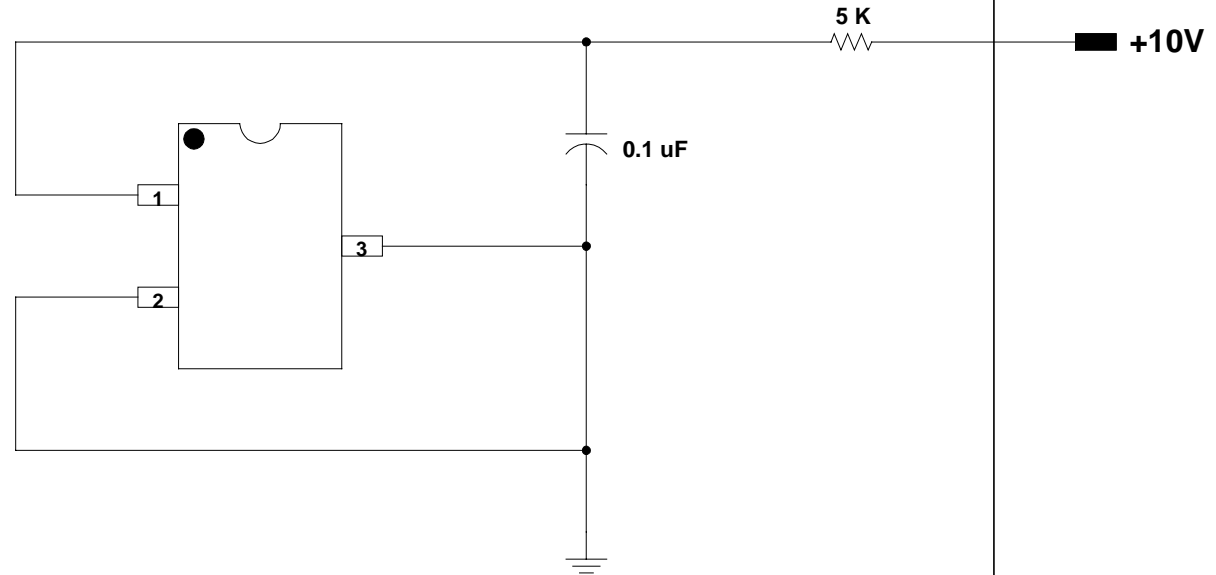
BONDING AREA

PKG. CODE: U3-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 45x32	PKG. DESIGN			BOND DIAGRAM #: 05-0901-0187	REV: A



ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX6006-9, LM4050/51, LM4040/41  
PACKAGE: 3-SOT23  
MAX. EXPECTED CURRENT = 1.75mA

NOTES: LM4040-1.2 = 1.75mA  
LM4040-2.1 = 1.59mA  
LM4040-2.5 = 1.50mA  
LM4040-3.0 = 1.40mA  
LM4040-4.1 = 1.18mA  
LM4040-5.0 = 1.00mA