RELIABILITY REPORT

FOR

DS28E07+T

PLASTIC ENCAPSULATED DEVICES

December 6, 2016

**MAXIM INTEGRATED**

160 RIO ROBLES

SAN JOSE, CA 95134

| **Approved by** |
| --- |
| Eric Wright |
| Quality Assurance |
| Reliability Engineer |

Maxim Integrated. All rights reserved.

## Conclusion

The DS28E07+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

## Table of Contents



## I. Device Description

A. General

The DS28E07 is a 1024-bit, 1-Wire® EEPROM chip organized as four memory pages of 256 bits each. Data is written to an 8-byte scratchpad, verified, and then copied to the EEPROM memory. As a special feature, the four user memory pages can individually be write protected or put in EPROM-emulation mode, where bits can only be changed from a 1 to a 0 state. Each device has its own guaranteed unique 64-bit ROM identification number (ROM ID) that is factory programmed into the chip. The communication follows the 1-Wire protocol with the ROM ID acting as node address in the case of a multiple-device 1-Wire network.

Maxim Integrated. All rights reserved.

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | 1024-Bit, 1-Wire EEPROM |
| B. Process: | GS18 |
| C. Fabrication Location: | USA |
| D. Assembly Location: | Philippines |
| E. Date of Initial Production: | September 25, 2015 |

## III. Packaging Information

| | |
|---|---|
| A. Package Type: | 3-pin TSOC |
| B. Lead Frame: | Copper |
| C. Lead Finish: | 100% Matte Tin |
| D. Die Attach: | Conductive |
| E. Bondwire: | Au (1 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | #05-0637 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Single Layer Theta Ja: | 160°C/W |
| J. Single Layer Theta Jc: | 4°C/W |
| K. Multi Layer Theta Ja: | 131.9°C/W |
| L. Multi Layer Theta Jc: | 4°C/W |

## IV. Quality Assurance Information

| | |
|---|---|
| A. Quality Assurance Contacts: | Eric Wright (Reliability Engineering)<br>Bryan Preeshl (Vice President of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet.<br>0.1% for all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

## V. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 160 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 6.87 \times 10^{-9}$

$\lambda = 6.87$ F.I.T. (60% confidence level @ 25°C)

B. E.S.D. and Latch-Up Testing

The ES02-0 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM: +/- 2500V per JEDEC JESD22-A114
ESD-CDM: +/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands overvoltage testing (1.5Vcc) per JEDEC JESD78.

Maxim Integrated. All rights reserved.

**Table 1**

Reliability Evaluation Test Results

**DS28E07+T**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 135C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | 160 | 0 | |

Note 1: Life Test Data may represent plastic DIP qualification lots.

Maxim Integrated. All rights reserved.