RELIABILITY REPORT

FOR

DG441CY+

PLASTIC ENCAPSULATED DEVICES

March 2, 2016

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
Reliability Engineer

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Conclusion

The DG441CY+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

Maxim's redesigned DG441/DG442 analog switches now feature on-resistance matching (4Ω max) between switches and guaranteed on-resistance flatness over the signal range (9Ω max). These low on-resistance switches conduct equally well in either direction. They guarantee low charge injection (10pC max), low power consumption (1.65mW), and an ESD tolerance of 2000V minimum per Method 3015.7. The new design offers lower off-leakage current over temperature (less than 5nA at +85°C). The DG441/DG442 are quad, single-pole/single-throw (SPST) analog switches. The DG441 has four normally closed switches, and the DG442 has four normally open switches. Switching times are less than 250ns for tON and less than 170ns for tOFF. These devices operate from a single +10V to +30V supply, or bipolar ±4.5V to ±20V supplies. Maxim's improved DG441/DG442 continue to be fabricated with a 44V silicon-gate process.

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II. Manufacturing Information

A. Description/Function:	Improved, Quad, SPST Analog Switches
B. Process:	S5
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	Pre 1997

III. Packaging Information

A. Package Type:	16-pin SOIC (N)
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0301-0588
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	115°C/W
K. Single Layer Theta Jc:	32°C/W
L. Multi Layer Theta Ja:	82.2°C/W
M. Multi Layer Theta Jc:	32°C/W

IV. Die Information

A. Dimensions:	71X91 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	5.0 microns (as drawn)
F. Minimum Metal Spacing:	5.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 400 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 2.75 \times 10^{-9}$

λ = 2.75 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S5 Process results in a FIT Rate of 0.08 @ 25C and 1.38 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot XRZARX005Q, D/C 9240)

The AG52 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000V per Mil-Std 883 Method 3015. Latch-Up testing has shown that this device withstands a current of +/-50mA.

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Table 1
Reliability Evaluation Test Results

DG441CY+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	80	0	NRZCDU003F, D/C 9921
	Biased	& functionality	80	0	XRZACB007D, D/C 9435
	Time = 192 hrs.		80	0	XRZABQ001B, D/C 9331
			80	0	XRZARX005Q, D/C 9240
			80	0	XRZCBQ001A, D/C 9326

Note 1: Life Test Data may represent plastic DIP qualification lots.

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