DG406xxx
Rev. A

RELIABILITY REPORT

FOR

DG406xxx

PLASTIC ENCAPSULATED DEVICES

March 30, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The DG406 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

Maxim's redesigned DG406 CMOS analog multiplexer now features guaranteed matching between channels (80max) and flatness over the specified signal range (90 max). This low on-resistance mux (1000 max) conducts equally well in either direction and features guaranteed low charge injection (15pC max). In addition, this new mux offers low input off-leakage current over temperature—less than 5nA at +85°C.

The DG406 is a 1 of 16 multiplexer/demultiplexer and operates with a +4.5V to +30V single supply and with ±4.5V to ±20V dual supplies. This improved mux is a pin-compatible plug-in upgrade for the industry standard DG406.

B. Absolute Maximum Ratings

Item	Rating
Voltage Referenced to V-	
V+	-0.3V, 44V
GND	-0.3V, 25V
Digital Inputs, S, D (Note 1)	(V- - 2V) to (V+ + 2V) or 30mA (whichever occurs first)
Continuous Current (any terminal)	30mA
Peak Current, S or D (pulsed at 1ms, 10% duty cycle max)	100mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature Ranges	
DG406C	0°C to +70°C
DG406D	-40°C to +85°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
28-Pin PDIP	727mW
28-Pin PLCC	842mW
28-Pin WSO	1000mW
Derates above +70°C	
28-Pin PDIP	9.09mW/°C
28-Pin PLCC	10.53mW/°C
28-Pin WSO	12.5mW/°C

Note 1: Signals on S_, D_, A0, A1, A2, A3, or EN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

II. Manufacturing Information

A. Description/Function:	Improved, 16-Channel, CMOS Analog Multiplexer
B. Process:	SG5 - Standard 5 micron silicon gate CMOS
C. Number of Device Transistors:	269
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines or Malaysia,
F. Date of Initial Production:	December, 1993

III. Packaging Information

A. Package Type:	**28-Lead WSO**	**28-Lead PDIP**	**28-Lead PLCC**
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0301-0641	# 05-0301-0640	# 05-0301-0642
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020A:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	98 x 184 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	5 microns (as drawn)
F. Minimum Metal Spacing:	5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 725 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 1.50 \times 10^{-9}$ $\lambda = 1.50$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-0485) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AG60 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

DG406xxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		725	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	PDIP WSO PLCC	77 77 77	0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

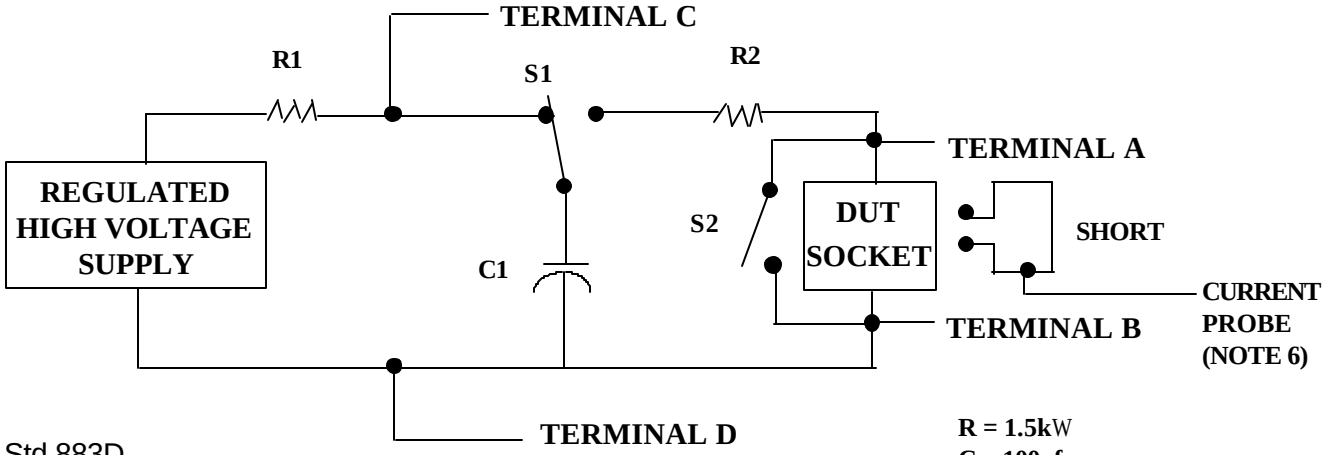
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

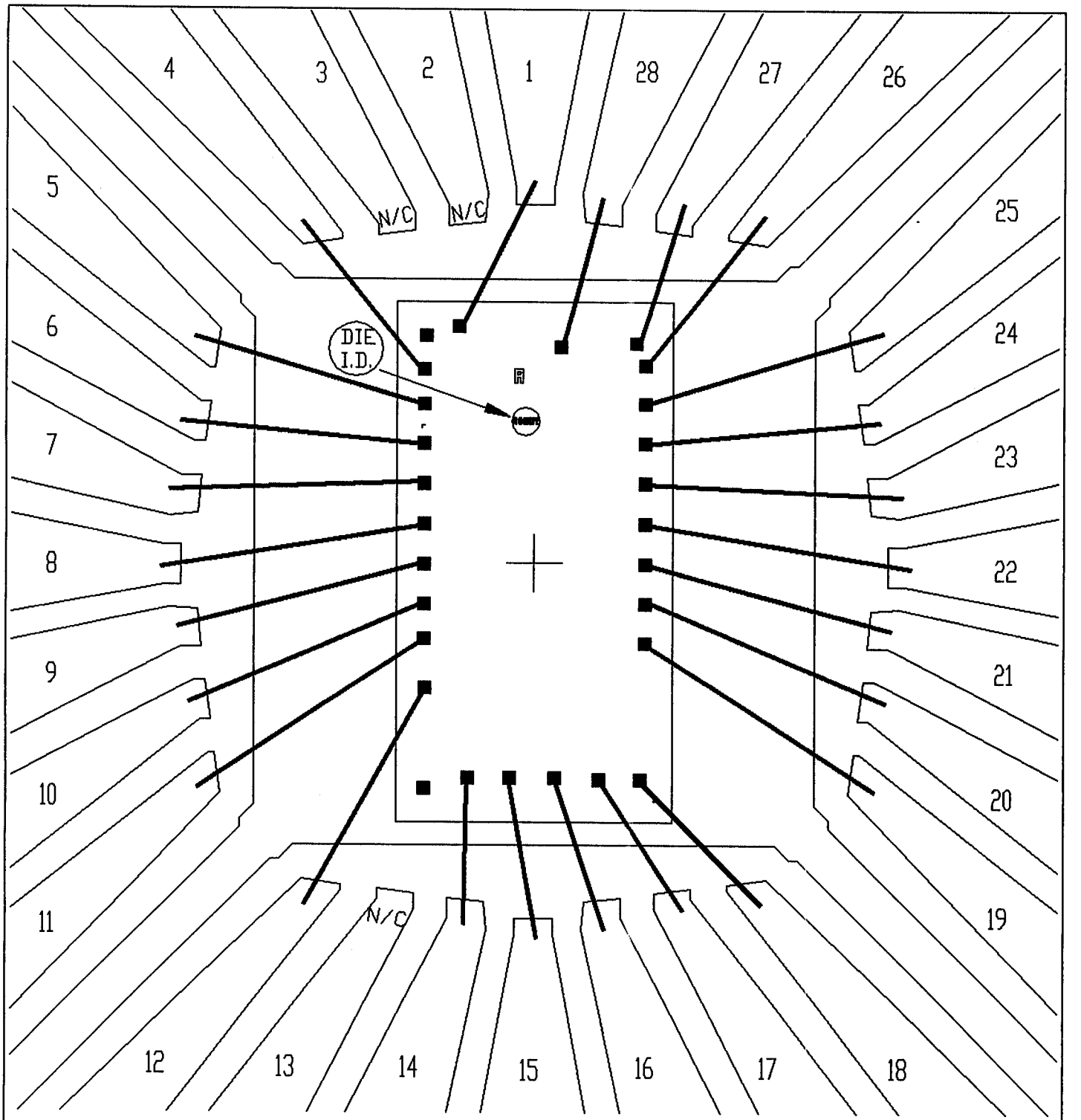
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

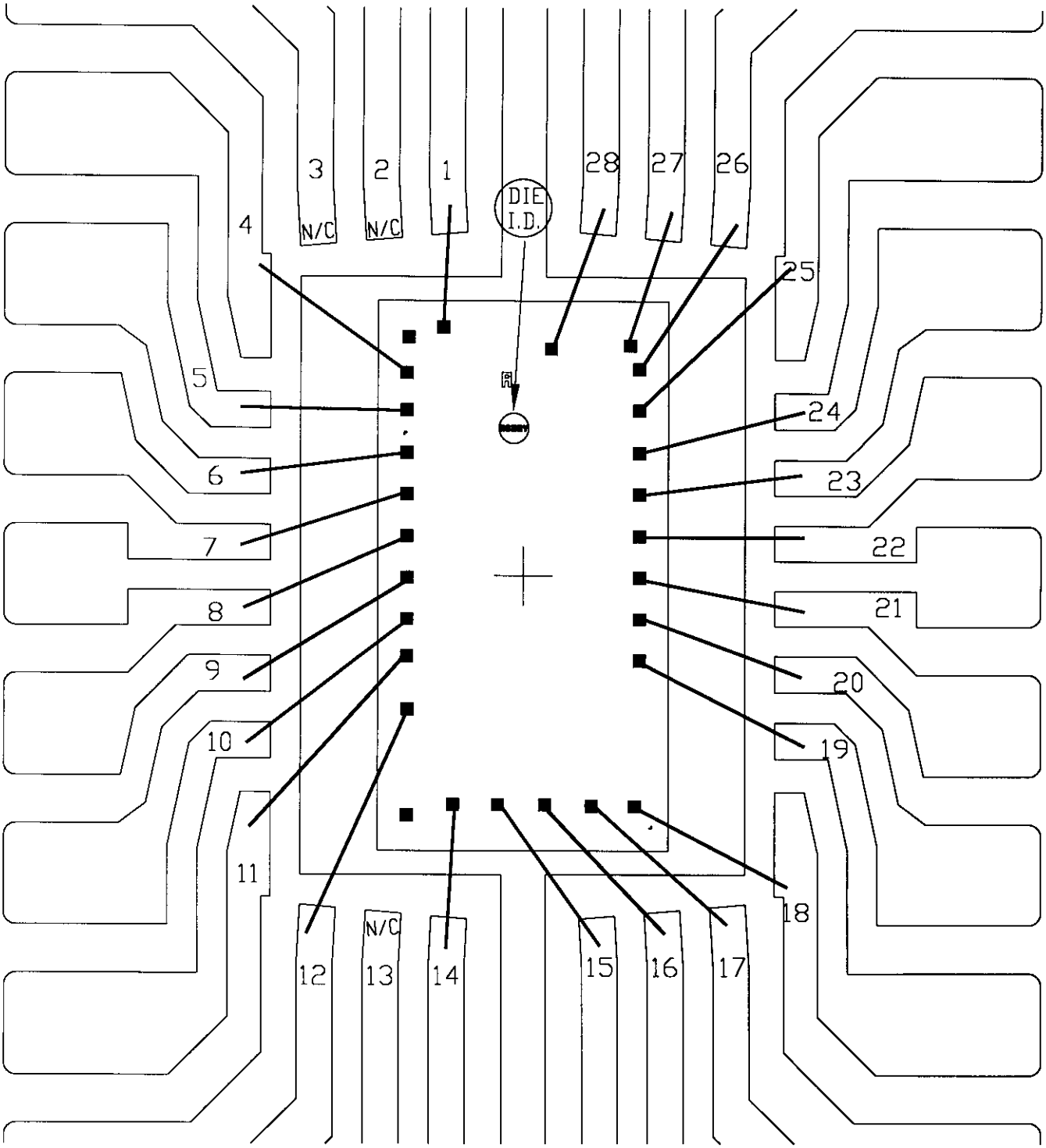
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



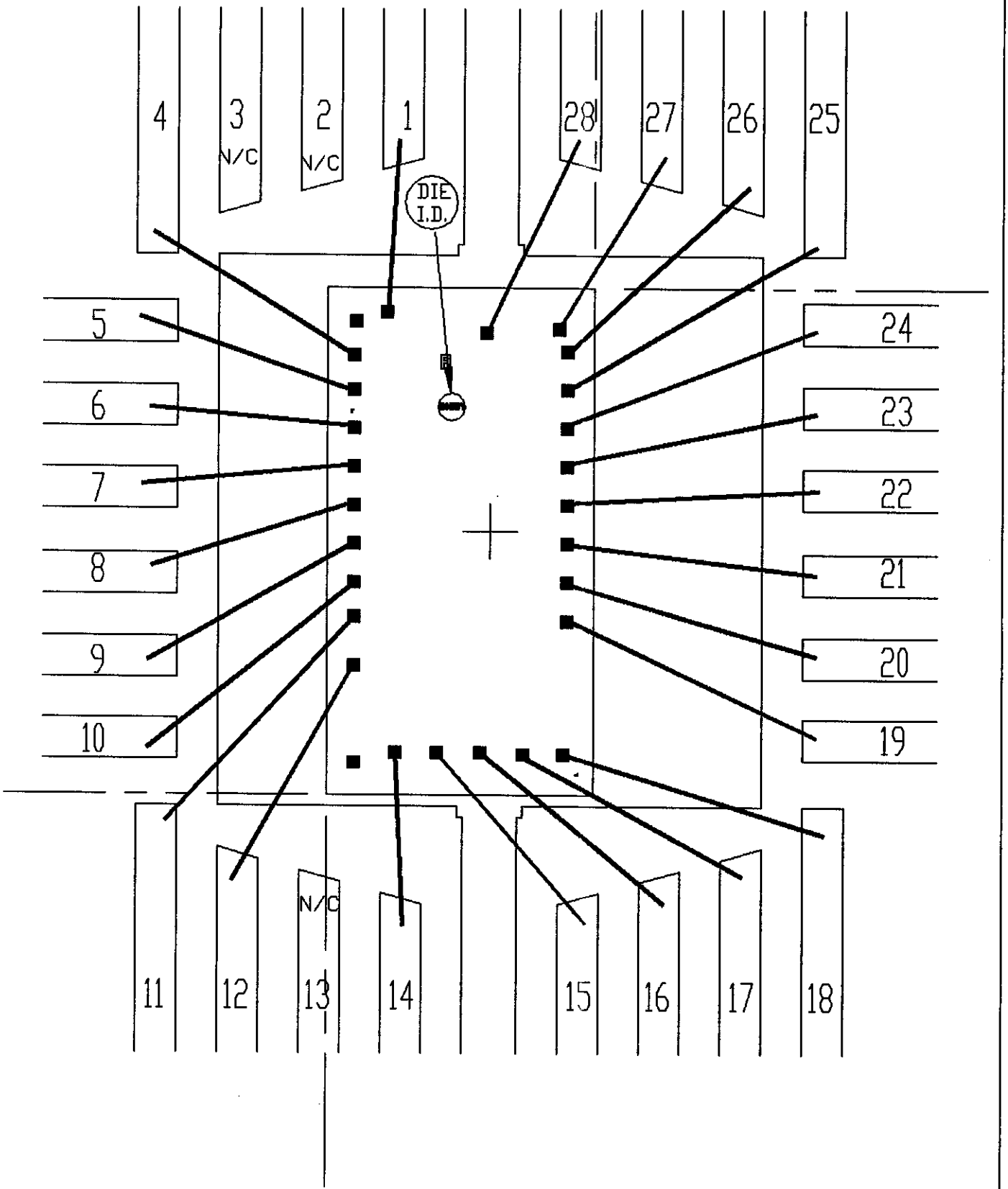
Mil Std 883D
Method 3015.7
Notice 8



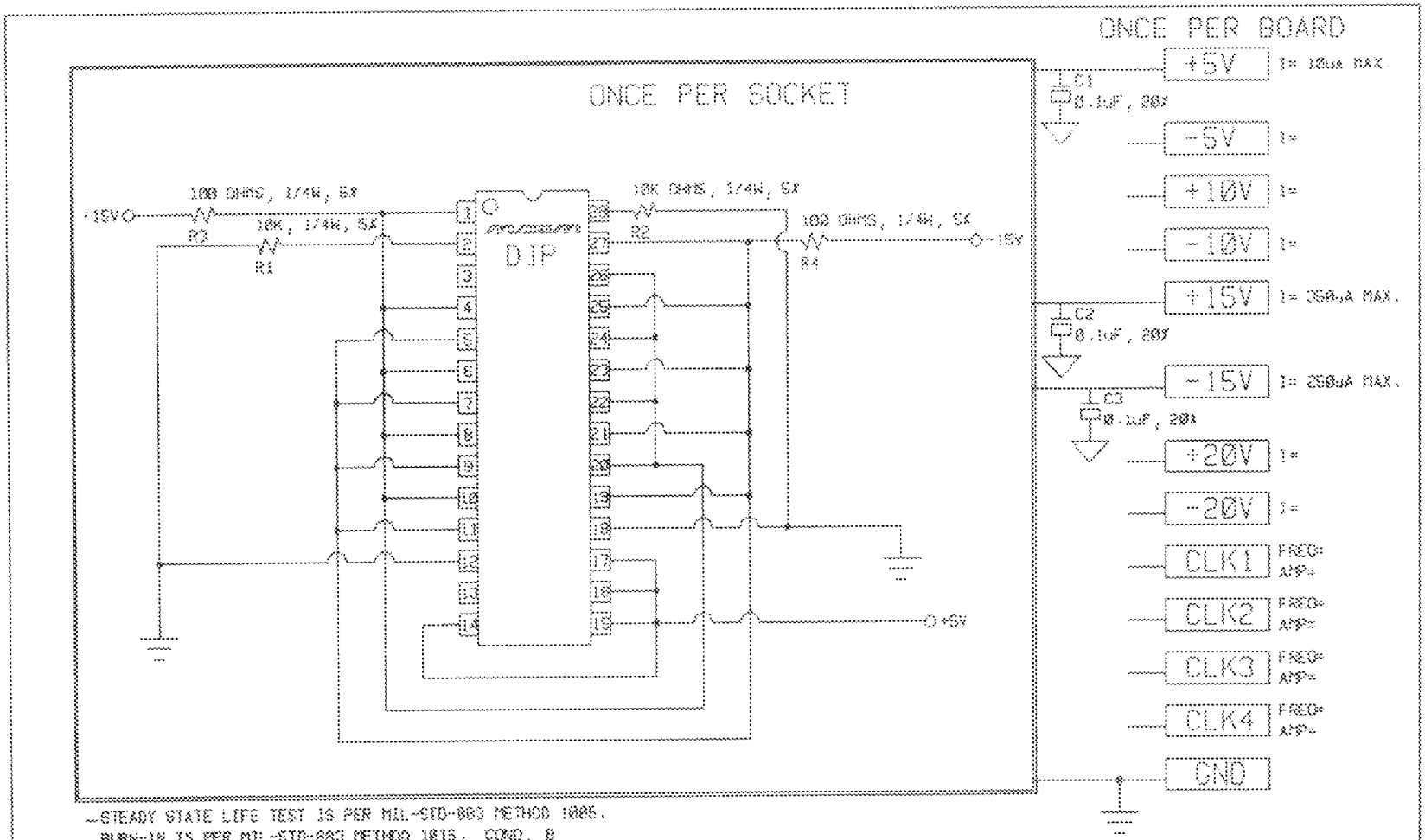
PKG.CODE: Q28-4		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 200 X 200	PKG. DESIGN			BUILDSHEET NUMBER: 05-0301-0642	REV.: A



PKG.CODE: W28-6		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 150X200	PKG. DESIGN			BUILDSHEET NUMBER: 05-0301-0641 / REV.: B



PKG.CODE: P28-3		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 200 X 200	PKG. DESIGN			BUILDSHEET NUMBER: 05-0301-0640 / REV.: A



NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR (X) COMMERCIAL
   (X) MR/883

SPEC. NO. 06-485 REV. C

DATE: 8/1/94

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE: MAX306/MAX307
DG406/407/506/507
ICL7506/7507