



78M6612 – Quality & Reliability Summary Report

Project #	Silicon Rev.	Doc Rev	Date
6612	A01	1	November 15, 2009

Introduction

This report summarizes the reliability data that have been collected by Teridian Semiconductor Corp for the 78M6612 product.

Process Information

The 78M6612 device is manufactured in a standard 0.25u Embedded Flash CMOS process at TSMC.

Process Characteristics:

- 2.5V/3.3V, 5V Tolerant
- 2 Poly Layers
- 4 Metal Layers
- Special ESD implant for I/O devices (3.3 V)

Process Technology Reliability Results:

Test Description	Total Parts	Read Points	Results
EFR JESD22-A108	790	48 hours	All Passed
HTOL JESD22-A108	1690	168 hours	All Passed
		500 hours	All Passed
		1000 hours	All Passed
85/85 JESD22-A101B	120x2	168 hours	All Passed
		500 hours	All Passed
		1000 hours	All Passed
Temp Cycling JESD22-A104	120x2	500 cycles	All Passed
Auto Clave JESD22-A102-C	120x2	168 hours	All Passed
High Temperature Storage JESD22-A103	120x2	1000 hours	All Passed

Product Biased Life Test:

Teridian has collected HTOL data from the 0.25u CMOS process at TSMC for a total sample size of 1690 units (7 different lots). A corresponding **FIT rate of 7** was calculated using 0.7eV activation energy, 60% confidence, and normal use of 55°C. Data collected for the 6612C is summarized below.

Test Description	Total Parts	Read Points	Results
EFR JESD22-A108	790	48hrs	All Passed
HTOL JESD22-A108	1690	500hrs	All Passed
	1690	1000hrs	All Passed

*Burn-in at 150°C Junction Temp, 1.1X Bias



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Package Information – 68 MLF

Package Type: 68MLF/QFN
 Lead Count: 68
 Body Size: 8x8x0.85mm
 Lead Pitch: 0.40mm
 JEDEC Outline: M0 220
 Assembly Sites: Unisem China

Bill of Materials:

	MLF (lead-free)
Lead frame	Copper Etched
Lead Finish	100% Matte Tin
Wire bond	1.0 mil: 99.99% Au/Be doped
Mold Compound	G770HCD
Die Attach Material	Ablestik 8920

Package Marking:

Line 1	Line 2	Line 3
Marketing Number	B(AC)(DC)P3	Lot Number

B = Wafer Foundry TSMC
 (AC) = Assembly Code (Unisem=C)
 (DC) = Date Code (YY, WW)


Moisture Sensitivity Classification:

MSL Level 3 (260°C IR Reflow, J-STD-020B)

Package Reliability:

Test Description	Total Parts	Read Points	Comments
Temp Cycling JESD22-A104	77x 3	500 cycles	ALL PASSED
High Temp Storage JESD22-A103	77x 3	500 hrs	ALL PASSED
		1000 hrs	ALL PASSED
85/85 JESD22-A101B	77x 3	500 hrs	ALL PASSED
		1000 hrs	ALL PASSED
HAST JESD22-A110-C	77x 3	168 hrs	ALL PASSED

Solder-ability Test J-STD-22-B102D Sn-3Ag-0.5Cu (SAC) Solder	40°C/85% RH Whisker Test J-STD-201A
0/9	0/135

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Package Information – 64 LQFP

Package Type: LQFP
 Lead Count: 64
 Body Size: 10x10x1.4mm
 Lead Pitch: 0.50mm
 JEDEC Outline: MS-026BCD
 Assembly Sites: Amkor Philippines and Unisem China

Amkor Philippines	
Lead frame	Copper Etched
Lead Finish	100% Matte Sn
Wire bond	1.0 mil: 99.99% Au/Be doped
Mold Compound	G700L
Die Attach Material	Ablestik 3230
Unisem China	
Lead frame	Copper Etched
Lead Finish	100% Matte Sn
Wire bond	1.0 mil: 99.99% Au/Be doped
Mold Compound	G600FB
Die Attach Material	Ablestik 8290

Package Marking:

Line 1	Line 2	Line 3
Marketing Number	B(AC)(DC)P6	Lot Num.

B = Wafer Foundry TSMC
 (AC) = Assembly Code (Amkor = P, Unisem = C)
 (DC) = Date Code (YY, WW)

Moisture Sensitivity Classification:
 MSL Level 3 (260°C IR Reflow, J-STD-020B)
 Package Reliability:

Test Description	Total Parts	Read Points	Comments
Temp Cycling JESD22-A104	77x 3	500 cycles	ALL PASSED
High Temp Storage JESD22-A103	77x 3	500 hrs	ALL PASSED
		1000 hrs	ALL PASSED
85/85 JESD22-A101B	77x 3	500 hrs	ALL PASSED
		1000 hrs	ALL PASSED
HAST JESD22-A110-C	77x 3	168 hrs	ALL PASSED

Solder-ability Test J-STD-22-B102D Sn-3Ag-0.5Cu (SAC) Solder	40°C/85% RH Whisker Test J-STD-201A
0/9	0/135

Recommended Reflow Soldering Profile:

(Per IPC/JEDEC J-STD-020C)

Reflow Parameter	Pb-Free Assembly
Average Ramp-Up Rate (T _{Smax} to T _p)	3 ^o C/second max.
Preheat	
- Temperature Min (T _{Smin})	150 ^o C
- Temperature Max (T _{Smax})	200 ^o C
- Time (t _{Smin} to t _{Smax})	60-180 seconds
Time maintained above:	
- Temperature (T _L)	217 ^o C
- Time (t _L)	60-150 seconds
Peak Temperature (T _p)	See Table 1 below
Time within 5 ^o C of actual Peak Temperature (t _p)	20-40 seconds
Ramp-Down Rate	6 ^o C/second max.
Time 25 ^o C to Peak Temperature	8 minutes max.

Note: All temperatures refer to topside of the package, measured on the package body surface.

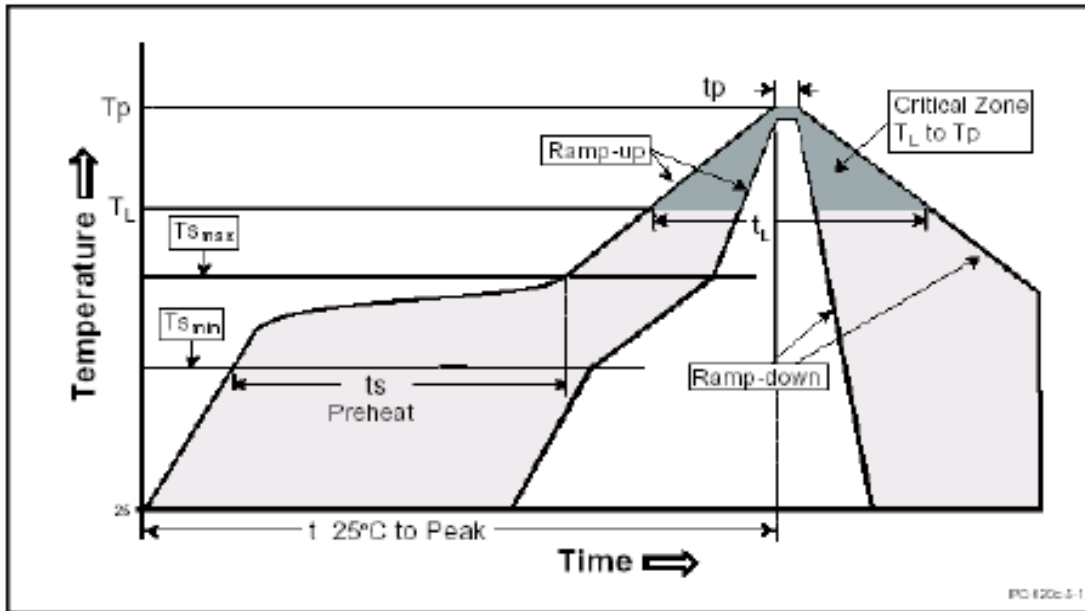


Table 1 Pb-Free Process – Peak Reflow Temperature (T_p)

Package Thickness	Volume mm ³ < 350	Volume mm ³ 350 - 2000	Volume mm ³ > 2000
<1.6 mm	280 +0 ^o C	280 +0 ^o C	280 +0 ^o C
1.6mm – 2.5 mm	280 +0 ^o C	250 +0 ^o C	245 +0 ^o C
≥2.5 mm	250 +0 ^o C	245 +0 ^o C	245 +0 ^o C



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Electrostatic Discharge:

The 6612 device has been tested for ESD immunity in accordance with JEDEC JESD22-A114.

Package	ESD (HBM) Rating	ESD (MM) Rating
64 pin	Max 5KV	Max 250V
68 pin	Max 5.5KV	Max 250V

Latch-Up:

Samples were tested in accordance to EIA/JEDEC 78 using a Keytek automatic test system. For all tests the failure criteria is specified as: 1.4X Inom or Inom+10mA, whichever is greater. Each pin was tested at the Trigger Duration of 1 second, which is the maximum limit per EIA/JEDEC 78.

Package	LU results
64 pin	All Pins >200 mA
68 pin	All Pins >200 mA

ATE Characterization

Method:

Revision 3 of the 6612 IC was processed over a corner-split lot and characterized over supply and temperature. Channel length (Poly) and thresholds (Vtn, Vtp) and were varied in the process corner lot for a total of five (5) splits. Fifteen units from each split (total of 75 units) were tested on ATE with estimated 99% test coverage over 5 corners of supply and temperature.

Results:

The production ATE limits have been guard-banded and bench correlated to ensure compliance to specification over stated operating conditions and maintain an AQL level of 0.65.