Introduction

The succeeding pages compile reliability data that have been collected by Teridian Semiconductor Corp on product number 71M6515/H.

Process Information

The 71M6515/H device is manufactured in a standard 0.25u Embedded Flash CMOS process at TSMC.
Process Characteristics:

- 2.5V/3.3, 5V Tolerant
- 2 Poly Layers
- 4 Metal Layers
- Special ESD implant for I/O devices (3.3 V)

Teridian Semiconductor (TSC) qualified this process using the reliability tests below:

Process Reliability:

Test Description	Total Parts	Read Points	Results
EFR JESD22-A108	200x3	48 hours	All Passed
HTOL JESD22-A108	1690	168 hours	All Passed
		500 hours	All Passed
		1000 hours	All Passed
85/85 JESD22-A101B	120x2	168 hours	All Passed
		500 hours	All Passed
		1000 hours	All Passed
Temp Cycling JESD22-A104	120x2	500 cycles	All Passed
Auto Clave JESD22-A102-C	120x2	168 hours	All Passed
High Temperature Storage JESD22-A103	120x2	1000 hours	All Passed

Biased Life Test

Teridian has collected HTOL data from the 0.25u CMOS process at TSMC for a total sample size of 1690 units (7 different lots). A corresponding **FIT rate of 7.0** was calculated using 0.7eV activation energy, 60% confidence, and normal use of 55°C. Data collected for the 6513 is summarized below.

Test Description	Total Parts	Read Points	Results
EFR JESD22-A108	200x3	48hrs	All Passed
HTOL JESD22-A108	1690	500hrs	All Passed
	1690	1000hrs	All Passed

*Burn-in at 125°C Junction Temp, 1.1X Bias

Package Information – 64 LQFP (Amkor)

Package Type: LQFP
Lead Count: 64
Body Size: 10x10x1.4mm
Lead Pitch: 0.50mm
JEDEC Outline: MS-026BCD
Assembly Sites: Amkor Philippines

Bill of Materials:

	LQFP (lead-free)
Lead frame	Copper Etched
Lead Finish	100% Matte Tin
Wire bond	1.0 mil: 99.99% Au/Be doped
Mold Compound	G700
Die Attach Material	Ablestik 3230

Package Marking:

Line 1	Line 2	Line 3
Marketing Number	B(AC)(DC)P3	Lot Number

B = Wafer Foundry TSMC
(AC) = Assembly Code (Amkor Philippines = P)
(DC) = Date Code (YY, WW)

Moisture Sensitivity Classification:

MRT Level 3 (260^{o}C IR Reflow, J-STD-020B)

Package Reliability:

Test Description	Total Parts	Read Points	Comments
Temp Cycling JESD22-A104	77x 3	500 cycles	ALL PASSED
High Temp Storage JESD22-A103	77x 3	500 hrs	ALL PASSED
		1000 hrs	ALL PASSED
85/85 JESD22-A101B	77x 3	500 hrs	ALL PASSED
		1000 hrs	ALL PASSED
Autoclave JESD22-A102-C	77x 3	168 hrs	ALL PASSED

Solder-ability Test Sn-3Ag-0.5Cu (SAC) Solder	Solder Heat Resistant	40^{o}C/85% RH Whisker Test
0/9	0/22	0/135

Package Information – 64 LQFP (Unisem)

Package Type: LQFP
Lead Count: 64
Body Size: 10x10x1.4mm
Lead Pitch: 0.50mm
JEDEC Outline: MS-026BCD
Assembly Sites: Unisem, China

Bill of Materials:

	LQFP (lead-free)
Lead frame	Copper Etched
Lead Finish	100% Matte Tin
Wire bond	1.0 mil: 99.99% Au/Be doped
Mold Compound	G700
Die Attach Material	Ablestik 8290

Package Marking:

Line 1	Line 2	Line 3
Marketing Number	B(AC)(DC)P3	Lot Number

B = Wafer Foundry TSMC
(AC) = Assembly Code (Unisem China = C)
(DC) = Date Code (YY, WW)

Moisture Sensitivity Classification:

MRT Level 3 (260^{o}C IR Reflow, J-STD-020B)

Package Reliability:

Test Description	Total Parts	Read Points	Comments
Temp Cycling JESD22-A104	77x 3	500 cycles	ALL PASSED
High Temp Storage JESD22-A103	77x 3	500 hrs	ALL PASSED
		1000 hrs	ALL PASSED
85/85 JESD22-A101B	77x 3	500 hrs	ALL PASSED
		1000 hrs	ALL PASSED
Autoclave JESD22-A102-C	77x 3	168 hrs	ALL PASSED

Solder-ability Test Sn-3Ag-0.5Cu (SAC) Solder	Solder Heat Resistant	40^{O}C/85% RH Whisker Test
0/9	0/22	0/135

Electrostatic Discharge:

The 6515H device has been tested for ESD immunity in accordance with JEDEC JESD22-A114.

Package	**ESD (HBM) Rating**
64 pins	Max 8000V

Latch-Up:

Samples were tested in accordance to EIA/JEDEC 78 using a Keytek automatic test system. For all tests the failure criteria is specified as: 1.4X Inom or Inom+10mA, whichever is greater. Each pin will be tested at the Trigger Duration of 1 second, which is the maximum limit per EIA/JEDEC 78.

The following latch-up measurements were taken in the TSC FA lab:

Package	**LU results**
64 pins	All Pins >200 mA

ATE Characterization

The 6515 IC was processed over a corner-split lot and characterized over supply and temperature. Channel length (Poly) and thresholds (Vtn, Vtp) and were varied in the process corner lot for a total of five (5) splits. Fifteen (x15) units from each split (total of 75 units) were tested on ATE with estimated 99% test coverage over 5 corners of supply and temperature.

Results:

The production ATE limits have been guard-banded and bench correlated to ensure compliance to specification over stated operating conditions and maintain an **AQL level of 0.65**. Optimized fuse trim targets for internal band gaps have also been implemented to achieve < 0.1% Wh accuracy over 2000:1 range for the 71M6515H.