With less than $20\text{fs}_{\text{RMS}}$ additive jitter over the 12kHz to 20MHz bandwidth, the LTC®6954 is ideal for distributing the low jitter clocks necessary to achieve the best SNR when driving high resolution data converters. Besides minimizing jitter, the LTC6954 features EZSync™ synchronization method that guarantees repeatable edge-synchronized outputs from one or multiple chips.

Features

- Three Independent, Low Noise Outputs
- Additive Jitter < $20\text{fs}_{\text{RMS}}$ (12kHz to 20MHz)
- Additive Jitter < $85\text{fs}_{\text{RMS}}$ (10Hz to Nyquist)
- Up to 1.8GHz Maximum Input Frequency
- EZSync Clock Synchronization Compatible
- Clock Dividers Covering All Integers from 1 to 63
- Phase Delays Covering All Integers from 0 to 63
- −40°C to 105°C Junction Temperature Range

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
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<tr>
<td>LTC6954-1</td>
<td>3 LVPECL Outputs</td>
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<td>LTC6954-2</td>
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<td>LTC6954-3</td>
<td>1 LVPECL and 2 LVDS/CMOS Outputs</td>
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<tr>
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</table>
EZSync Multichip Synchronization Simplifies the Generation of Repeatable Edge-Synchronized Outputs

With EZSync Enabled and the PECL0 Output of the LTC6950 Driving the LTC6954 Input, All Seven Outputs of the Two Devices Are Rising-Edge Synchronized

EZSync Disabled: Random Phase Relationship Between the Outputs of the LTC6950 and LTC6954 Clock Dividers

EZSync Enabled: Repeatable Rising-Edge Aligned Outputs of the LTC6950 and LTC6954 Clock Dividers

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