



ADV202 Session 3

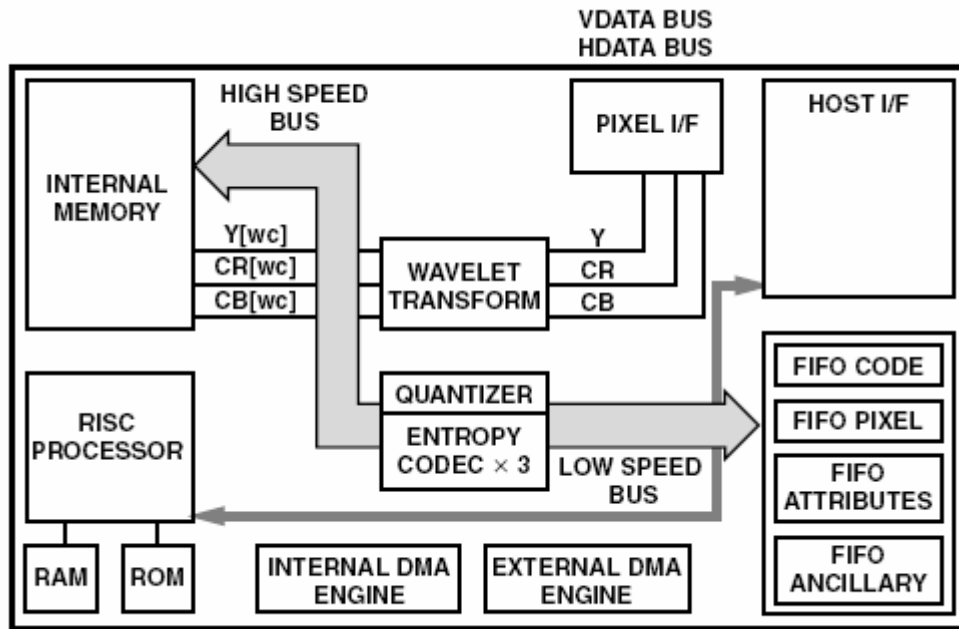
General Architecture

Encoding and Decoding Process

Interfacing the ADV202

Host Modes and Video Modes

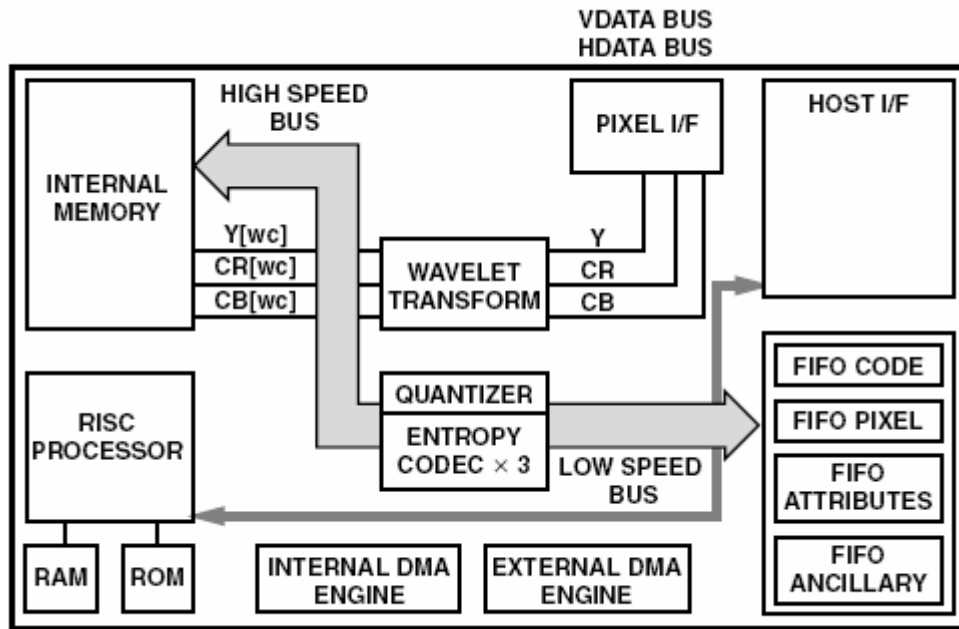
ADV202 Architecture



The ADV202 contains the following main functional blocks:

1. Risc processor. This embedded 32-bit RISC processor serves as a system controller. The RISC processor includes its own ROM and RAM for both program and data memory.
2. Wavelet transform engine with 5/3 and 9/7 wavelet filters giving up to 6 transform levels.
3. Three Entropy Codecs to generate JPEG2000 code-stream: using quantization, Rate Distortion Optimization and context modeling, organize data into packets and layers throughput of up to 65 Msamples/s.
4. Host Interface can be configured for 32-bit or 16-bit control and 8-, 16- or 32-bit data. Controls data transfers between FIFOs and controls 2 external DMA channels. Controls access to indirect and direct register.

ADV202 Architecture



5. Pixel Interface is used to process video or pixel data transfers from/to VDATA or HDATA bus.

6. Internal DMA engine. Is used to facilitate fast internal memory-to-memory data transfers.

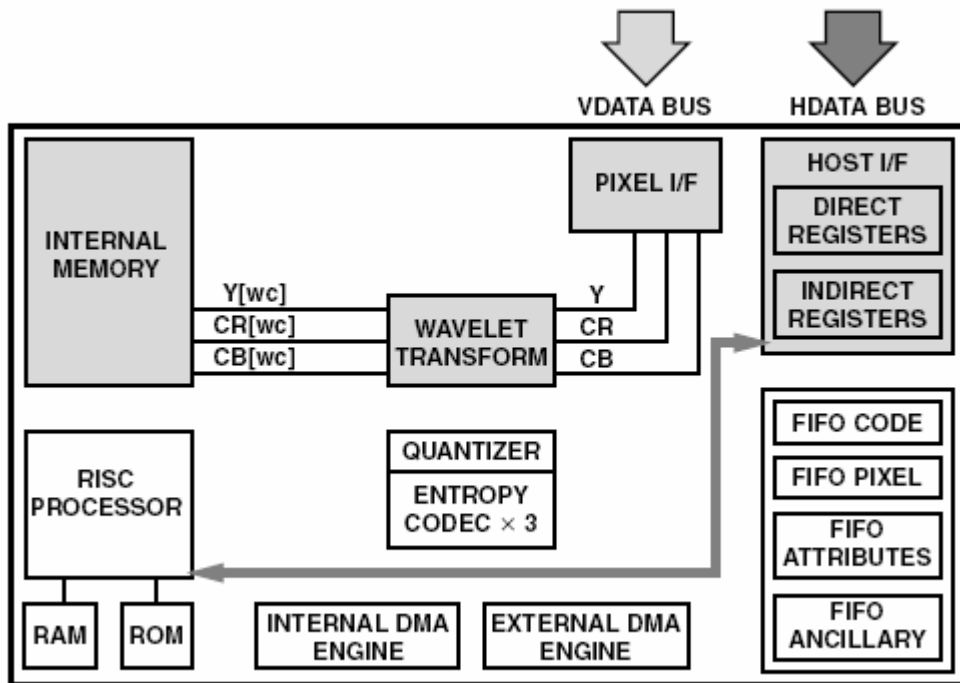
7. FIFOs

PIXEL – Uncompressed data (Host Mode) (0x0)

CODE – Compressed data (0x1)

ATTR – Attribute data (rarely used) (0x2)

ADV202 – Encode process I



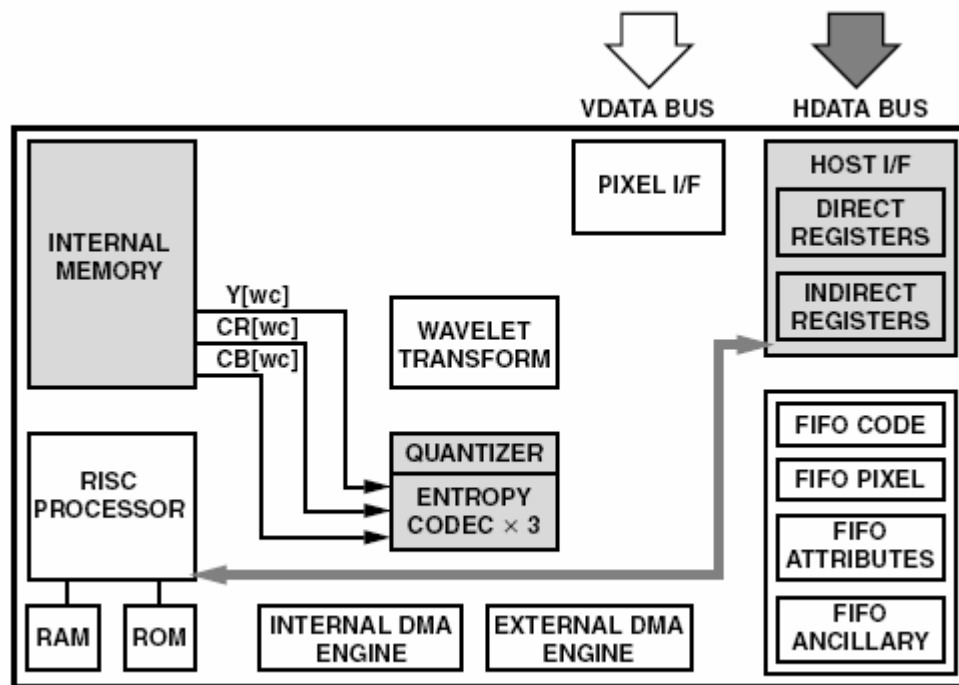
Video or pixel data can be input over the VDATA bus or alternatively pixel data can be input over the HDATA bus. In either case the video/pixel data is passed to the Pixel Interface.

The data is then de-interleaved and passed to the wavelet transform engine. The input data, organized in tiles or frames, is then decomposed into subbands using 5/3 or 9/7 wavelet filters.

The WT can perform up to 6 wavelet decomposition levels on a tile/frame.

The resultant wavelet coefficients are then written to internal memory.

ADV202 – Encode process II

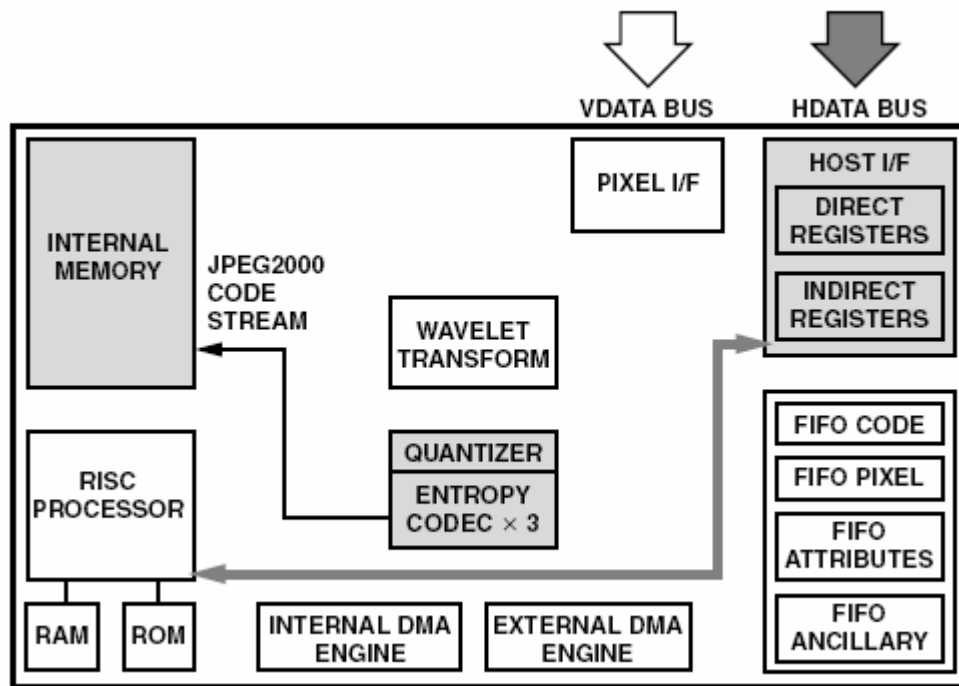


The wavelet coefficients are passed to 3 entropy codecs.

Wavelet coefficients are arranged into units of code-blocks, a code-block being essentially a bit stream of data.

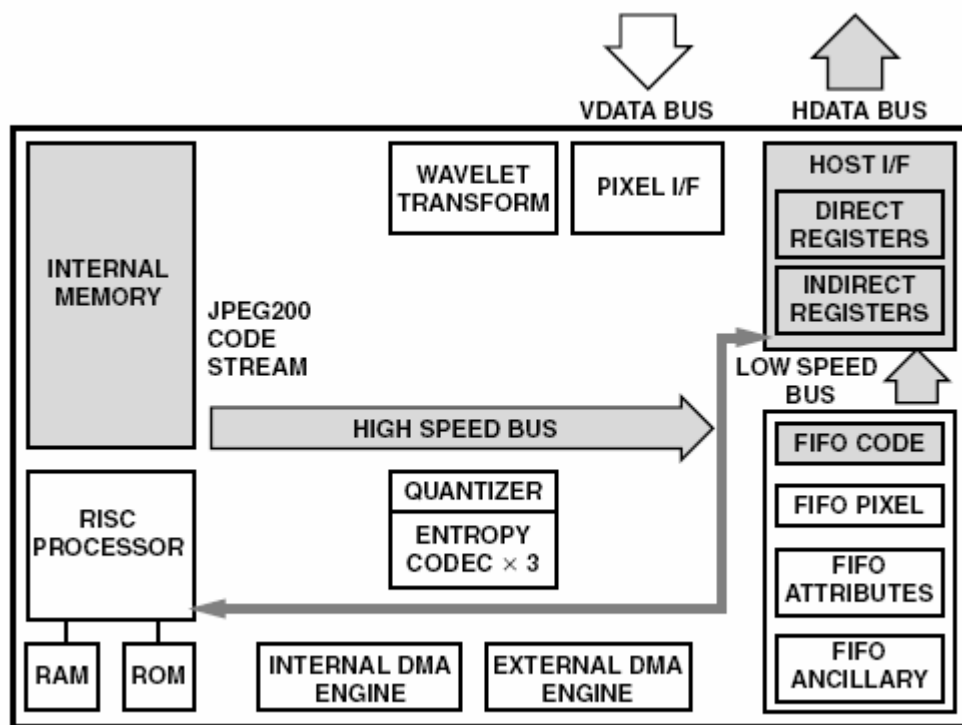
Processing is done on a code-block by code-block basis.

ADV202 Encode process III



After processing the data is arranged into packets and layers defining the JPEG2000 code stream and send back to internal memory.

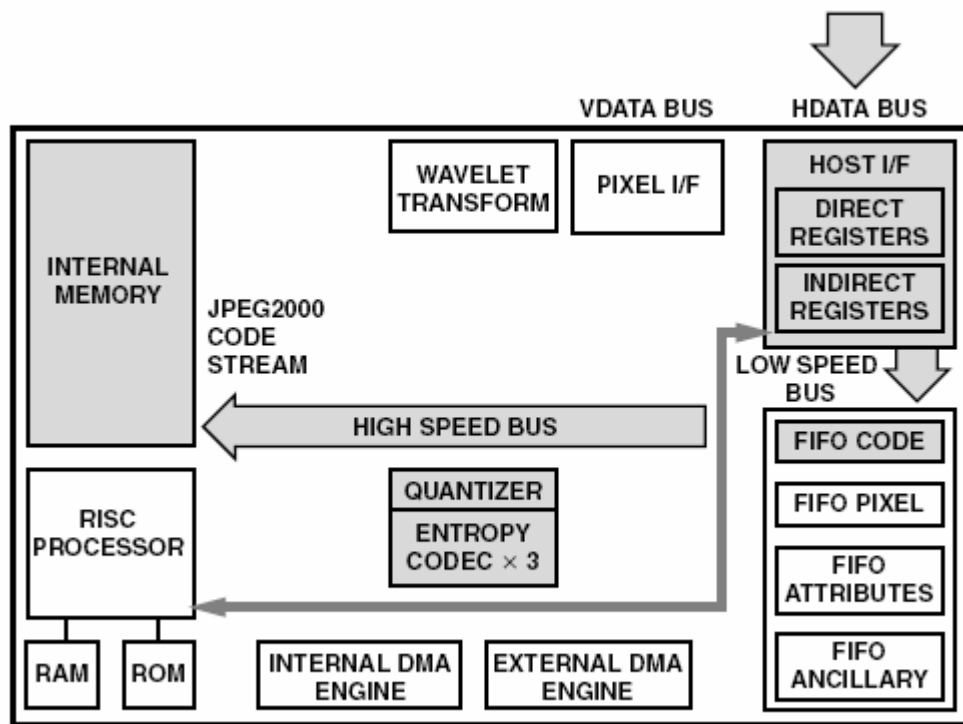
ADV202 Encode process IV



The JPEG2000 code-stream is send over a high speed bus to the Code FIFO in order to buffer internal high speed bus and low speed host interface.

The data can then be output over the host interface using a common read/write access protocol [CS/, RD/, WR/, ACK/, ADDR] or over the external DMA engine in conjunction with an external DMA controller using a DREQ/DACK protocol.

ADV202 Decode process I



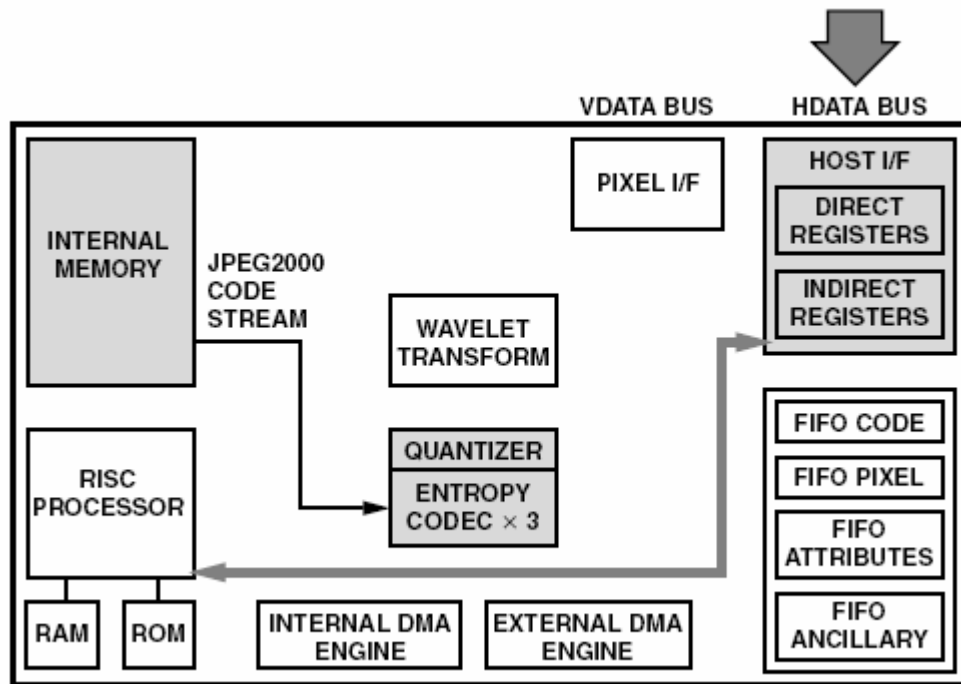
Compressed data is input over the host interface using the same protocols as in Encode mode and passed on to the CODE FIFO from which it is sent to the internal memory.

500KB are available for internal storage of wavelet data [uncompressed NTSC field = 345KB].

Depending on the compression ratio, the ADV202 can store 1 or more fields of wavelet transformed data.

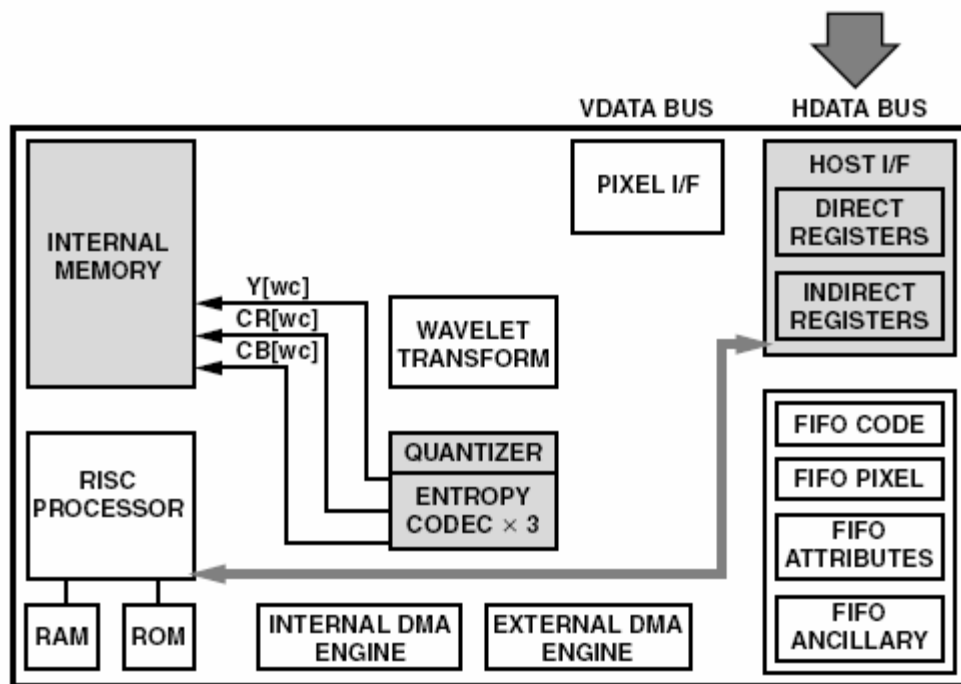
In decode, the ADV202 works 'ahead': It waits until information of 1+ field is present before starting to decode.

ADV202 Decode process II



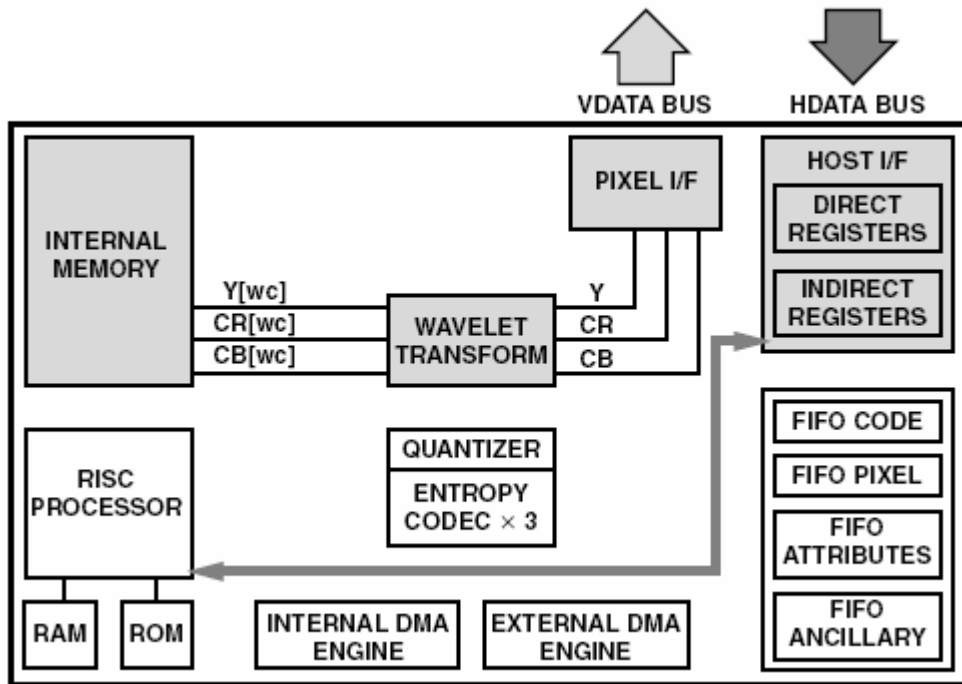
The JPEG2000 code-stream is passed to the entropy codecs which decompose the code-stream back into wavelet coefficients.

ADV202 Decode process III



The wavelet coefficients are passed back into internal memory.

ADV202 Decode process IV



The wavelet coefficients are read from internal memory and are recomposed into uncompressed component samples and are passed to the pixel interface where the components are interleaved into a video stream and output over the VDATA or HDATA bus.

ADV202 interface

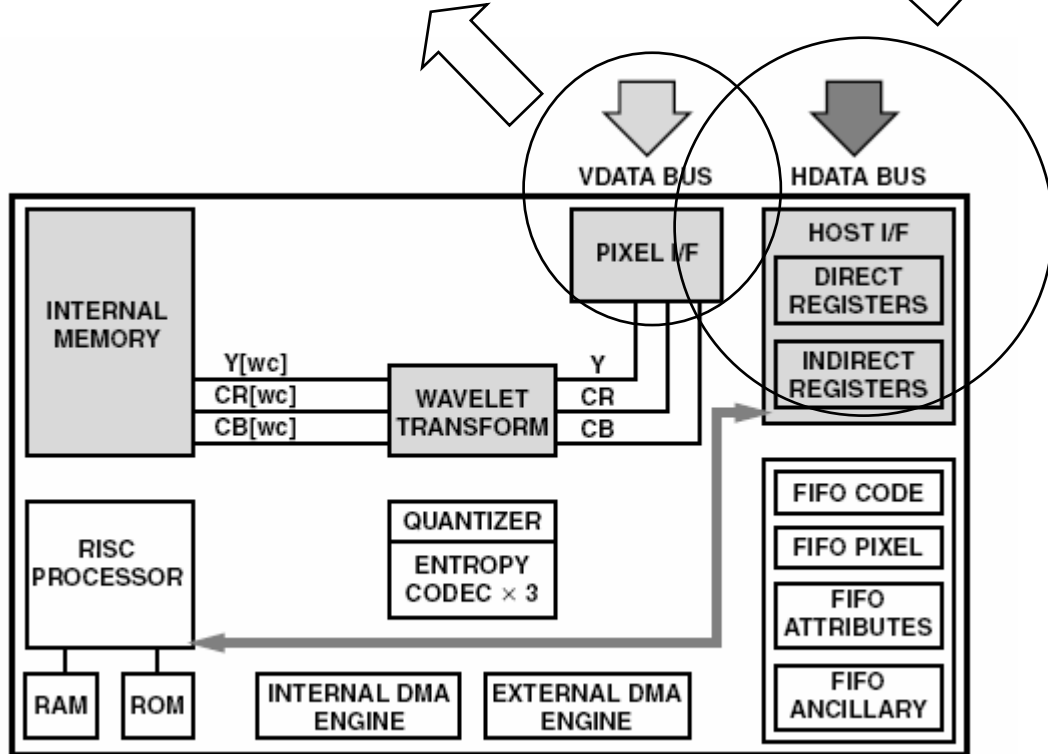
VIDEO INTERFACE:

During encode process

To input video or pixel data.

During decode process

To output de-compressed video or pixel data.



HOST INTERFACE:

Start of application

- 1) Write to Direct Registers to configure ADV202 for application.
- 2) Load firmware for specific application
- 3) Load programmable parameters for specific application
- 4) Configure Host Interface for specific data transfer mode

During encode process

To output compressed data.

During decode process

To input compressed data.

ADV202 interface

VDATA - VIDEO INTERFACE:

During encode process

To input video or pixel data.

During decode process

To output de-compressed video or pixel data.

HDATA - HOST INTERFACE:

Start of application

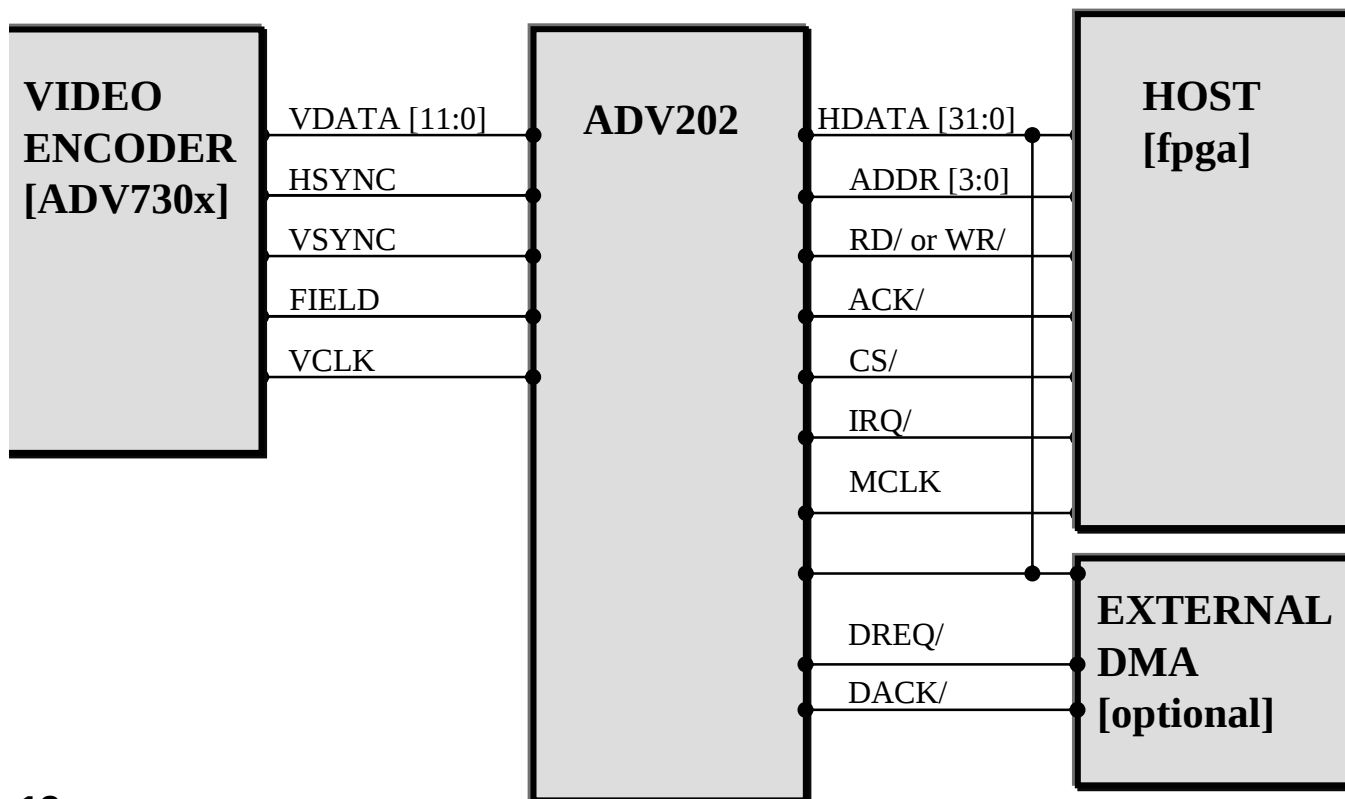
- 1) Write to Direct Registers to configure ADV202 for application.
- 2) Load firmware for specific application
- 3) Load programmable parameters for specific application
- 4) Configure Host Interface for specific data transfer mode

During encode process

To output compressed data.

During decode process

To input compressed data.





ADV202 HDATA – Host interface

- ◆ SRAM Style Parallel interface – Normal Host Mode
 - 16-bit
 - 32-bit
 - CS/, RD/ or WR/, ACK/, ADDR
- ◆ DMA Modes
 - 2 channels
 - DREQ/DACK Burst & Single
 - DCS Mode
- ◆ JDATA Mode
 - 8 bit synchronous
 - Must use 16-bit host interface



ADV202 HDATA – Host interface

The ADV202 allows several modes to interface to the compressed data:

Normal Host Mode

- a. Must be used regardless of what interface mode is used to initialize the part.
- b. Can be used to input compressed data in decode mode or output compressed data in encode mode using the Threshold registers while using VDATA for video input [encode] or video output [decode].

JDATA Mode

- a. JDATA mode can be used to input compressed data in decode mode, or output compressed data in encode mode.
- b. JDATA is a synchronous interface where HDATA is sync-ed to MCLK.
- c. This mode is for real-time applications where video data is input over VDATA while compressed data is output over JDATA [encode] or vice versa in decode.
- d. JDATA is configured for an 8-bit wide data bus with host being 16-bit.

DMA Modes :

Any ADV202 DMA mode is making use of the ADV202 DMA interface.

The ADV202 has 2 DMA channels.

In most applications, one DMA channel is used to output compressed data [encode] or input compressed data [decode] while the VDATA interface is used for pixel data interface.

- a. DREQ/DACK in single access mode
- b. DREQ/DACK in burst access mode
- c. Dedicated Chip Select mode



ADV202 HDATA – Host interface

Host Interface Pixel Interface Mode

HIPI mode is making use of the 2 DMA channels the ADV202 provides.

During encode mode, one DMA channel is used to input raw pixel data, while channel 2 is used to output compressed data. In decode, this process is reversed.

In this mode, VDATA is not used.

Configuration, uncompressed data input and compressed data output all make use of the same HDATA interface.



ADV202 HDATA – Host interface

	Normal Host Mode	JDATA	DMA	HIPI
Data width	16-bit, 32-bit	8-bit	16-bit or 32-bit	16-bit or 32-bit
Control width	16-bit, 32-bit	16-bit	16-bit, 32-bit	16-bit, 32-bit
Compressed Data Output Rate	25 Mbytes/sec	25 Mbytes/sec	25 Mbytes/sec	25 Mbytes/sec
Max. uncompressed data input rate	45 Msamples/sec	37 Msamples/sec	45 Msamples/sec	45 Msamples/sec
Interface	Asynchronous host mode	Synchronous to Mclk	Asynchronous DREQ/DACK	Asynchronous DREQ/DACK
Number of pins required	ADDR [3:0] CS/ ACK/ WR/ and RD/ IRQ/ [optional] HDATA [16 or 32]	JDATA [7:0] Mclk HOLD VALID + Normal Host Mode	DREQ0/ DACK0/ + Normal Host Mode	DREQ0/ DACK0/ DREQ1/ DACK1/ + Normal Host Mode



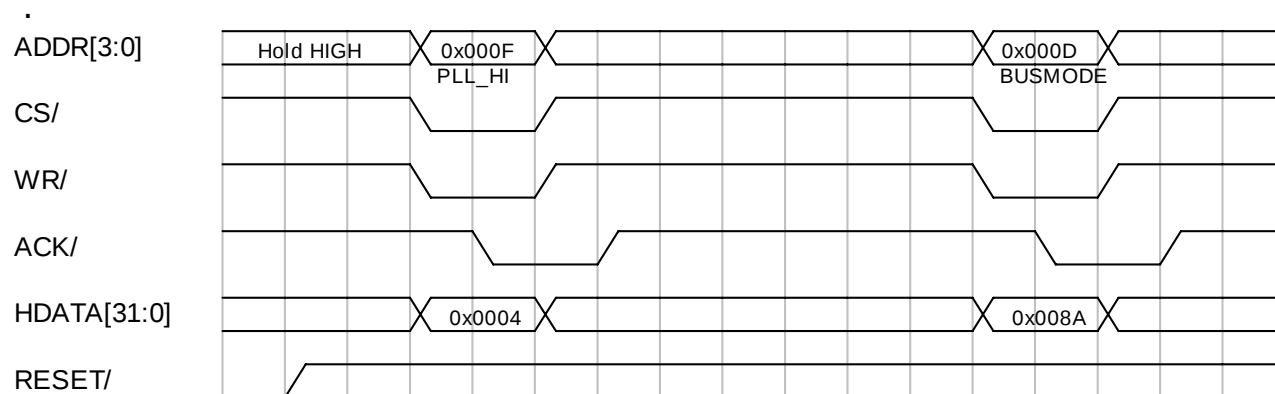
ADV202 VDATA – Video interface

- ◆ Consists of VDATA pins with HVF pins [optional].
- ◆ Video Interface can be configured in different modes:
 1. Custom Specific mode in EAV/SAV mode: Expecting YCbCr or single component data with embedded syncs on VDATA[11:0].
 2. Custom Specific mode in HVF mode : Expecting video accompanied by separate HVF syncs on VDATA[11:0].
 3. Video Raw mode : Expecting raw video data without any blanking on VDATA[15:0]
- ◆ For 1080i, 720p, NTSC, PAL dimension registers are programmed by the firmware.
- ◆ For all other formats dimension registers must be programmed using Custom Specific Mode.



ADV202 Configuration – Normal Host Mode

Writing to direct and indirect registers to configure the ADV202 uses a simple ADDR/CS/RD/WR/ACK protocol found on most processors or fpgas. This is Normal Host Mode.



Direct Registers : 16 direct registers available.
Configure ADV202 bus width, PLL settings and set Interrupts.
Provides access to indirect registers.

Indirect Registers: Are accessed over 2 direct registers.
Load firmware.
Load parameters.
Program Dimension Registers [optional].
Program DMA registers [optional].

After configuring direct and indirect registers, loading firmware and parameters, the ADV202 is ready to be run in an encode or decode application without further user interference.



ADV202 Configuration - Direct Registers

5 Fifos

PIXEL – Uncompressed data (Host Mode) (0x0)

CODE – Compressed data (0x1)

ATTR – Attribute data (rarely used) (0x2)

ANCL – Ancillary data (never used) (0x3)

CMDSTA – Command Stack (never used) (0x4)

3 Interrupt Registers

EIRQIE – Interrupt enables (0x5)

EIRQFLG – Interrupt flags (0x6)

SWFLAG – Application ID, other info from firmware (0x7)

2 Bus Control Registers

BMODE – Sets width and mode of bus (0x8)

MMODE – Sets options for the bus (0x9)

3 Indirect Access registers

STAGE – Used to “stage” upper part of 32-bit values for 16-bit bus (0xA)

IADDR – Internal address for indirect register (0xB)

IDATA – Data for indirect register (0xC)

Boot Mode

BOOT – used to set mode for set up procedure (0xD)

2 PLL Registers

PLL_HI – used to set multiplier for internal ARM vs JCLK

PLL_LO – sets internal clock rate (JCLK) vs. MCLK



ADV202 Configuration – User Control

The ADV202 is a very flexible device. It allows the user a lot of control how the ADV202 is configured or used.

◆ User Control over:

1. Firmware version

2. Video data input format :

- 8-bit to 24-bit pixel data
- single, two or 3 component
- EAV/SAV, HVF or no blanking
- Input at any rate as long as < data input rate limits

3. HDATA

- 16-bit or 32-bit control
- 8-bit, 16-bit or 32-bit data
- HDATA modes and external DMA

4. Input frequency and
Operating frequency

Vclk 20MHz-74.25MHz
Mclk 10MHz – 74.25MHz



ADV202 Configuration – User Control

◆ User Control over:

5. JPEG2000 parameters

Non Jpeg2000 specific:

- Video format [PAL, NTSC, 1080i etc]
- Bit precision
- Frame drop [select input frame rate]

Jpeg2000 specific:

- Code-block size
- Number of transform levels
- 9/7 or 5/3 wavelet transform
- Reversible or irreversible compression
- Compression ratio = variable bit rate output
- Fixed bit rate output = variable compression rate
- Progression order
- Quantization factor
- File format output [j2c, jp2, Raw-ADV202]
- Visual weighting

◆ No User Control over :

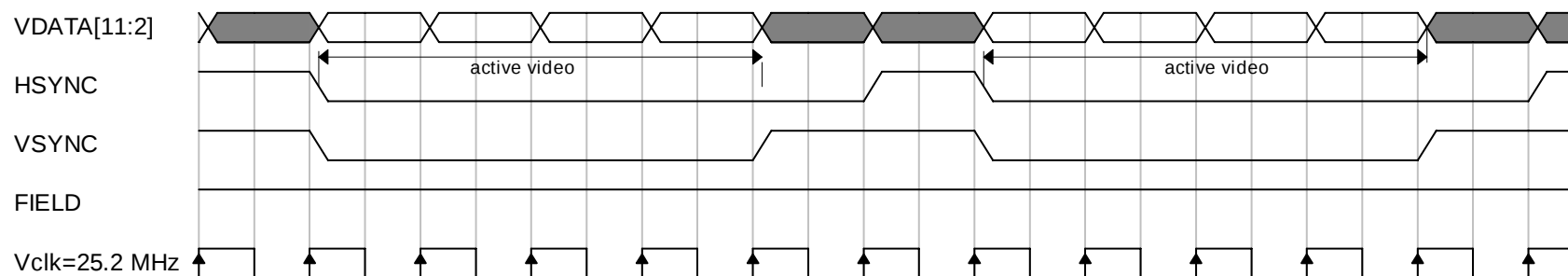
1. Encode process and decode process as outlined above.
2. Firmware edits.



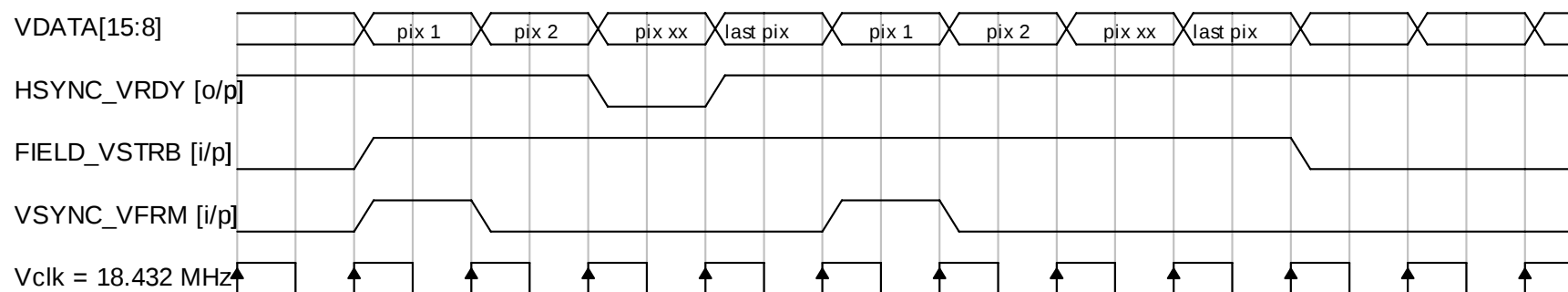
ADV202 Custom Specific Mode/Video Raw Mode/HIPI mode

Custom Specific mode, Video Raw mode and HIPI mode are all modes that can be used to input any format that does not comply to Standard PAL/NTSC/1080i or 720p.

Custom Specific mode



Video Raw Mode

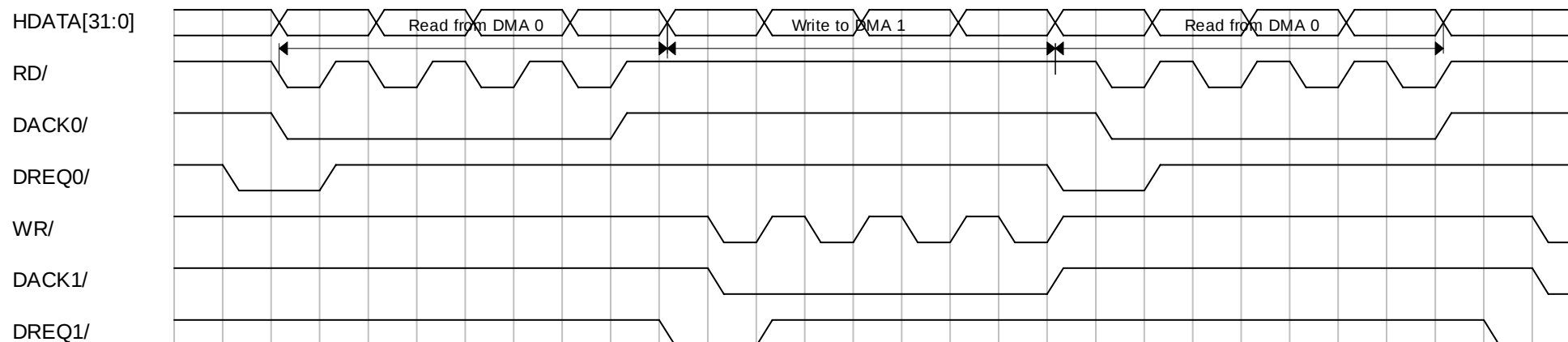




ADV202 Custom Specific Mode/Video Raw Mode/HIPI mode

Custom Specific mode, Video Raw mode and HIPI mode are all modes that can be used to input any format that does not comply to Standard PAL/NTSC/1080i or 720p.

HIPI mode





ADV202 Custom Specific Mode/Video Raw Mode/HIPI mode

	Custom Specific	Video Raw	HIPI Mode
Input rate	65Msamples/sec	65 Msamples/sec	45 Msamples/sec
Input Interface	VDATA[11:0] with optional HVF +VCLK	VDATA[15:8] + VCLK	HDATA[31:0]
Format	YCbCr in 4:2:2 with blanking regions if not NTSC, PAL, 1080i or 720p	YCbCr in 4:2:2 without blanking	YCbYCr 4:2:2 without blanking regions Other formats: YYCbCr, CbCr,
	Single component with blanking regions if not NTSC, PAL, 1080i or 720p	Single component without blanking regions	Single component without blanking regions
	Either EAV/SAV or HVF	No timing information	No timing information
	Interlaced or non-interlaced	Non-interlaced	Non-interlaced
To be captured dimensions defined by	EAV/SAV or HVF input and dimension register settings	Contol input signals and dimension register settings	Dimension register settings
Programming	All dimension registers	XTOT, YTOT only	XTOT, YTOT only
Programming reference	<i>Getting Started with ADV202 – page 31</i>	<i>Getting Started with ADV202 – page 38</i>	<i>ftp://ftp.analog.com/pub/Digital Imaging/ADV202_ApplicationNotes/ADV202_HIPImode_Still_Image_Application/</i>



ADV202 # - How many ADV202s ?

The ADV202 has a limit on how much input data it can process at any one time.

There are four limiting factors that determine how many ADV202s are required for a particular application:

1. **Data input rate.**

Data input rate = active vertical resolution x active horizontal resolution x field rate x components per pixel [Msamples/sec

If VDATA is used as the pixel input interface then the max. number of samples/sec can be up to 65Msamples/sec.

For HDATA interface this is 45 Msamples/sec when using the ADV202 150-MHz version .

2. **Tile width of the input image.**

Depending on the compression mode used, the max. allowable tile width can be 4096 pixels.

3. **Samples per image.**

Samples per image are limited to 1.048 Msamples.

This refers to the number of active samples of the input image/frame or field.

Note that YCbCr in 4:2:2 format contains 2 samples per pixel.

For example, standard definition NTSC contains 720x240x2 samples/field.

4. **Number of codeblocks per image.**

Is limited to 610 codeblocks per image/frame or field.

With the largest programmable codeblock size of 128x32 an active resolution of 1024x1024 is supported.

For standard definition resolutions all available codeblock sizes are supported.

For high definition resolutions the codeblock size must be 64x32, 64x64 or 128x32.



ADV202 # - How many ADV202s ?

	Msamples/sec	Tile width	Compression Mode	Samples/image	Number of code blocks	Number of ADV202s required
NTSC	20.7	720	any	345.6K	~ 228 [64x32]	1
PAL	20.7	720	any	414.7K	~ 297 [64x32]	1
1080i	124.4	1920	9/7i or 5/3i	1.036M	~ 1149 [128x32]	2
1Kx1K monochrome @ 60 frames/sec	62.9	1024	any	1.048M	~ 417 [128x32]	1
ADV202 limits [see datasheet, tables 23 and 24]	ADV202 max. allowable input rate on VDATA in Msamples/sec	Max. allowable tile width for YCbCr	Compression Mode	Samples/image	Number of code blocks	
	65	2048	5/3 irreversible	1.048 M	610	

ADV202 support documentation

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ADV202 - JPEG 2000 Video CODEC

Data Sheets

Rev B, 01/2005 (pdf, 863K)

Email PDF

Application Notes

Evaluation Boards

Price, Packaging,
and Availability

Lead(Pb) - Free Data

(Data Sheet Help)

Product Description

The ADV202 is a single-chip JPEG2000 codec targeted for video and high bandwidth image compression applications that can benefit from the enhanced quality and feature set provided by the JPEG2000...[More](#)

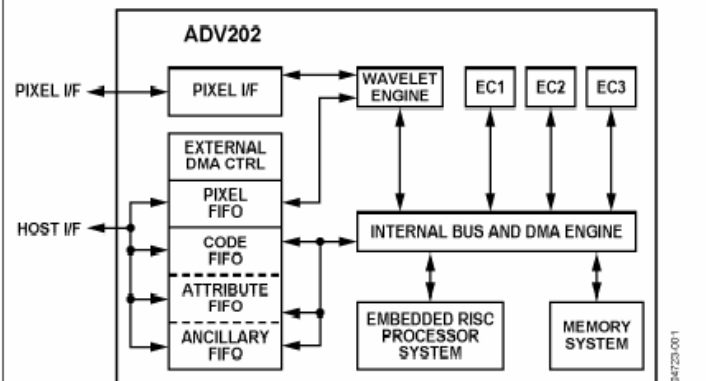
Visit the [ADV202 Third Party Developer page](#) where you'll find links to companies that provide products and services in conjunction with JPEG2000, from software CODECs to hardware and software design.

For questions or more information on the ADV202, please contact the [JPEG2000 Development Group](#).

Specifications

Bits per Component	16
Compression Format	JPEG2000
Microcontroller Interface	16 or 32-bits
External Memory Necessary	No - Internal
On-board Rate Control	Yes
HD Encode Capability	Yes
Pixel interface	10, 12, 14, 16, 8
Max. Tile Width	4096 Pixels
Development Kits	Evaluation Board , Video Pipe (3rd Party)
Target Applications	CCTV, Consumer, Industrial, Professional
Temp Range (°C)	-40 to 85

Functional Block Diagram



[Symbols and Footprints](#)

Design Tools

[Evaluation Boards/Tools](#)

Related Tech Info

[Application Notes](#)

[Technical Documentation](#)

[Analog Dialogue](#)

[More...](#)

Resources

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Signal Chains

[Interactive Signal Chains](#)

Access to :

- ◆ Datasheet
- ◆ Firmware
- ◆ User Guides
- ◆ Application notes
- ◆ Evaluation board support do and software
- ◆ Errata sheets etc.



ADV202 support documentation

Application Notes and Tech Notes

1. [Getting Started with the ADV202](#)

Before starting out with the ADV202, it is recommended to consult the following three Application Notes:

[AN-790: How to use the ADV202 Application Note](#) (pdf, 361,958 bytes) gives a brief overview of the ADV202 including a general description, the data flow for both coding processes, a review of interfaces and modes, as well as a recommendation of how to determine the number of ADV202s required for a particular application.

[Getting Started with the ADV202](#), (pdf, 375,166 bytes) contains detailed instructions for implementing specific applications by describing the procedures necessary for programming the ADV202 as well as an explanation of JPEG2000 parameters.

[AN-799: ADV202 Test Modes](#), (pdf, 174,968 bytes) provides instructions on confirming correct hardware configurations for register accesses, JDATA mode or DREQ/DACK modes.

2. [Multi-chip Applications](#)

Application notes for using multiple ADV202s. These notes contain sample codes and recommended methods for merging Y and CbCr streams during the encoding process.

3. [HIPI Mode and Still Image Applications](#)

Generally used in still image applications, this application note is an introduction to HIPI mode [Host Interface - Pixel Interface]. Configuration procedures as well as code examples can be found here.

4. [ADV202 Output format and Attribute Data Format](#)

This document contains information about the ADV202's compressed output data formats that are programmable with the Encode JPEG2000 parameter COD_STYLE and the Attribute data formats that are programmable with the Encode JPEG2000 parameter ATTRTYPE.

ADV202 Datasheet and User Guide

1. [ADV202 Data Sheet](#), (pdf, 319,284 bytes)

Timing, electrical and mechanical specifications of the ADV202.

2. [ADV202 User Guide](#), Rev.3.03 (pdf, 780,094 bytes)

A 180+ page reference guide for the ADV202, the User Guide contains detailed description of the ADV202 from functional and register descriptions, an overview of application examples, firmware parameters, as well as software and hardware configurations.

Design Tools

[Evaluation Boards/Tools](#)

Related Tech Info

[Application Notes](#)

[Technical Documentation](#)

[Analog Dialogue](#)

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Resources

[Overview](#)

[Press Releases](#)

[Product Highlights](#) (pdf, 488,543 bytes)

[More...](#)



ADV202 support documentation

ADV202 Firmware

[Latest ADV202 firmware](#) can be downloaded from this location. The ADV202 requires encode or decode firmware to be downloaded onto the on-chip memory to initiate compression or decompression. Both encode and decode firmware is periodically updated with new features and improvements to increase functionality, though older versions of the firmware can be used in applications.

Evaluation Boards

There are 3 evaluation systems available for the ADV202:

1. ADV202 PCI HD card
2. ADV202 P160 FPGA system

The ADV202-HD PCI card supports in-/output of 1080i in SDI format. The card is compatible with 32/64-bit 2.2-PCI WinXP systems.

Schematics for the ADV202-HD PCI card and evaluation notes can be downloaded at [ADV202 Evaluation Documents](#).

All information about the P160 FPGA system are located at [ADV202 P160 FPGA Evaluation System](#).

The ADV202 FPGA Evaluation System contains a ADV202 daughter card on a Xilinx platform. It allows the user to evaluate the ADV202 for parameters and performance when used in a stand-alone application via switch settings on the board.

Evaluation Board Software

ADI has developed Windows Application software for the ADV202 HD PCI card complete with drivers. The software and drivers for the ADV202 HD PCI card can be downloaded without charge at [ADV202 PCI Evaluation Software](#). This location also contains installation instructions and sample demo files.

There are two versions of Windows application software available for the PCI cards:

1. ADV202 Toolkit Version
2. ADV202 Alberio Version

The ADV202 Toolkit version - recommended for evaluating the performance of the ADV202 only. The Toolkit allows the user to change the parameters of the ADV202 in regard to both compression and decompression.

ADV202 Alberio Version - suitable as a basis for software application development using the ADV202. Alberio enables the implementation of JPEG2000 over a network environment for both still and moving images as well as incorporating other development features.

Note that the P160 FPGA board is fundamentally a stand-alone board, though register values can be changed through software that is located in the P160 folder.

ADV202 PCNs and Errata sheets

[ADV202 PCN and Errata sheets](#)

General JPEG2000 and ADV202 information