ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±13 V (+26 V)
Power Dissipation	See Figure 3
Storage Temperature	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
LFCSP-32 (CP)	27.27	°C/W
TSSOP-28/EP (RE)	35.33	°C/W

Maximum Power Dissipation

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming that the load (R_L) is midsupply, the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$).

RMS output voltages should be considered. If R_L is referenced to V_{S-} as in single-supply operation, the total power is $V_S \times I_{OUT}$.

In single supply with R_L to V_{S-}, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package versus the ambient temperature for the LFCSP-32 and TSSOP-28/EP packages on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

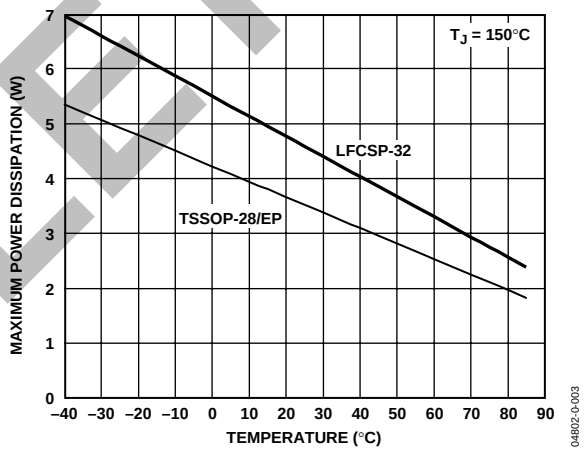

Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

See the Thermal Considerations section for additional thermal design guidance.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

THERMAL CONSIDERATIONS

When using a quad, high output current amplifier, such as the AD8392, special consideration should be given to system level thermal design. In applications such as ADSL/ADSL2+, the AD8392 could be required to dissipate as much as 1.4 W or more on chip. Under these conditions, particular attention should be paid to the thermal design in order to maintain safe operating temperatures on the die. To aid in the thermal design, the thermal information in the Thermal Resistance section can be combined with what follows here.

The information in Table 4 and Figure 3 is based on a standard JEDEC 4-layer board and a maximum die temperature of 150°C. To provide additional guidance and design suggestions, a thermal study was performed under a set of conditions more closely aligned with an actual ADSL/ADSL2+ application.

In a typical ADSL/ADSL2+ line card, component density usually dictates that most of the copper plane used for thermal dissipation be internal. Additionally, each ADSL/ADSL2+ port may be allotted only 1 square inch, or even less, of board space. For these reasons, a special thermal test board was constructed for this study. The 4-layer board measured approximately 4 inches × 4 inches and contained two internal 1 oz copper ground planes, each measuring 2 inches × 3 inches. The top layer contained signal traces and an exposed copper strip ¼ inch × 3 inches to accommodate heat sinking, with no other copper on the top or bottom of the board.

Three 28-lead TSSOPs were placed on the board representing six ADSL channels, or one channel per square inch of copper, with each channel dissipating 700 mW on-chip (1.4 W per package). The die temperature is then measured in still air and in a wind tunnel with calibrated airflow of 100 LFM, 200 LFM, and 400 LFM. Figure 36 shows the power dissipation versus the ambient temperature for each airflow condition. The figure assumes a maximum die temperature of 135°C. No heat sink was used.

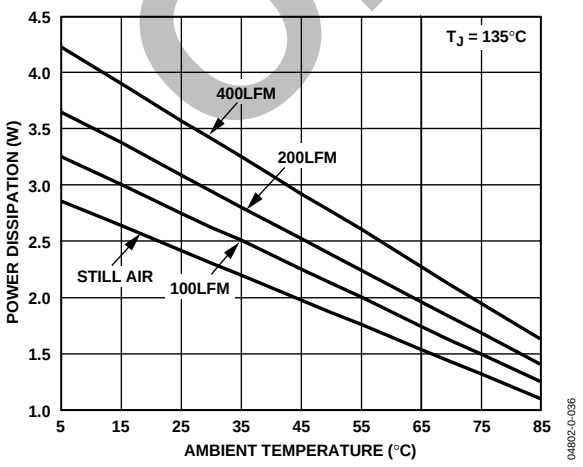

Figure 36. Power Dissipation vs. Ambient Temperature and Air Flow 28-Lead TSSOP/EP

This data is only provided as guidance to assist in the thermal design process. Due diligence should be performed with regards to power dissipation because there are many factors that can affect thermal performance.

TYPICAL ADSL/ADSL2+ APPLICATION

In a typical ADSL/ADSL2+ application, a differential line driver is used to take the signal from the analog front end (AFE) and drive it onto the twisted pair telephone line. Referring to the typical circuit representation in Figure 37, the differential input appears at V_{IN+} and V_{IN-} from the AFE, while the differential output is transformer coupled to the telephone line at tip and ring. The common-mode operating point, generally midway between the supplies, is set through V_{COM}.

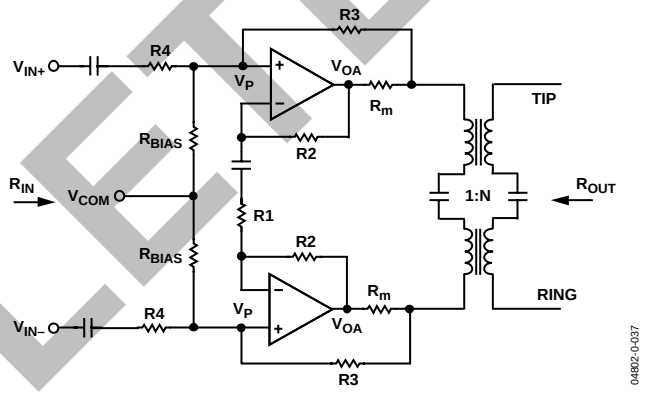

Figure 37. Typical ADSL/ADSL2+ Application Circuit

In ADSL/ADSL2+ applications, it is common practice to conserve power by using positive feedback to synthesize the output resistance, thereby lowering the required ohmic value of the line matching resistors, R_m. The circuit in Figure 37 is somewhat unique in that the positive feedback introduced via R3 has the effect of synthesizing the input resistance as well. The following definitions and equations can be used to calculate the resistor values necessary to obtain the desired gain, input resistance, and output resistance for a given application. For simplicity the following calculations assume a lossless transformer.

The following values are used in the design equations and are assumed already known or chosen by the designer.

- V_{IN} Differential input voltage
- R_{IN} Desired differential input resistance
- N Transformer turns ratio
- V_{LINE} Differential output voltage at tip and ring
- R_m Each is typically 5% to 15% of the transformer reflected line impedance
- $R2$ Recommended in the amplifier data sheet
- V_P Voltage at the + inputs to the amplifier, approximately ½ V_{IN} (must be less than V_{IN} for positive input resistance)
- R_L Transformer reflected line impedance

Additional definitions for calculating resistor values include:

V_{OA}	Voltage at the amplifier outputs
k	Matching resistance reduction factor
A_V	Gain from V_{IN} to transformer primary
β	Negative feedback factor
α	Positive feedback factor

Note: R1 must be calculated before β and α.

$$V_{OA} = \frac{V_{LINE}(1+k)}{N} \qquad k = \frac{2\,R_m}{R_L} \qquad A_V = \frac{V_{LINE}}{N\,V_{IN}}$$

$$\beta = \frac{R1}{R1 + 2\,R2} \qquad \alpha = \beta(1-k)$$

With the above known quantities and definitions, the remaining resistors can readily be calculated.

$$R1 = \frac{2\,V_P\,R2}{V_{OA} - V_P}$$

$$R4 = \frac{R_{IN}\,(V_{IN} - V_P)}{2\,V_{IN}}$$

$$R3 = \frac{A_V\,R4\left(2\,R1R_m + R1R_L - \alpha\,R1R_L - 2\alpha\,R2\,R_L\right)}{\alpha\,R_L\left(R1 + 2\,R2\right)}$$

$$R_{BIAS} = \frac{\alpha\,R3\,R4}{R4 - \alpha\,(R3 + R4)}$$

After building the circuit with the closest 1% resistor values, the actual gain, input resistance, and output resistance can be verified with the following equations.

$$GAIN_{(V_{IN}\ to\ LINE)} = \frac{N}{\beta(k+1)\left(1 + \frac{R4}{R3} + \frac{R4}{R_{BIAS}}\right) - \frac{R4}{R3}}$$

$$R_{IN} = \frac{2}{\frac{1}{R4} - A_V\,\beta\left(\frac{2\,R_m + R_L}{R4\,R_L}\right)}$$

$$R_{OUT} = \frac{2\,R_m\,N^2}{1 - \left(\frac{R4\,R_{BIAS}}{R1\left(R4 + R_{BIAS}\right)}\right)\left(\frac{R1 + 2R2}{R3 + \frac{R4\,R_{BIAS}}{R4 + R_{BIAS}}}\right)}$$

MULTITONE POWER RATIO

The DMT signal used in ADSL/ADSL2+ systems carries data in discrete tones or bins, which appear in the frequency domain in evenly spaced 4.3125 kHz intervals. In applications using this type of waveform, multitone power ratio (MTPR) is a commonly used measure of linearity. Generally, there are two types of MTPR that designers are typically concerned with: in-band and out-of-band MTPR. In-band MTPR is defined as the measured difference from the peak of one tone that is loaded with data to the peak of an adjacent tone that is intentionally left empty. Out-of-band MTPR is more loosely defined as the spurious emissions that occur in the receive band located between 25.875 kHz and the first downstream tone at 138 kHz. Figure 38 and Figure 39 show the AD8392 in-band MTPR for a 5.5 crest factor waveform for empty bins in the ADSL and extended ADSL2+ bandwidths. Figure 40 shows the AD8392 out-of-band MTPR for the same waveform.

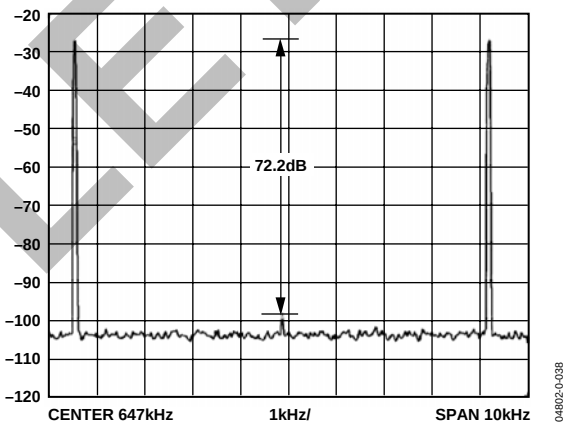

Figure 38. In-Band MTPR at 647 kHz

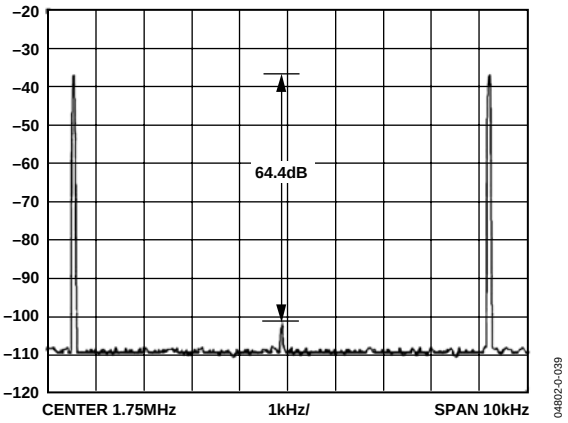

Figure 39. In-Band MTPR at 1.751 MHz

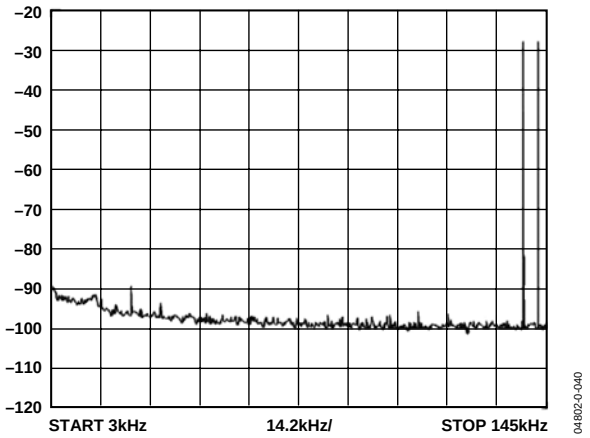

Figure 40. Out-of-Band MTPR

LIGHTNING AND AC POWER FAULT

The AD8392 can be used is as an ADSL/ADSL2+ line driver. In this application, the line driver is transformer-coupled to the twisted pair telephone line and could be subjected to large line transients resulting from events such as lightning strikes or downed power lines. In this type of environment, additional circuitry may be required to protect the AD8392 from damage that may occur as a result of these events. Using a minimal amount of external protection, the AD8392 has successfully passed overvoltage and overcurrent compliance testing per the ITU K-20 specification. For details on the external protection circuitry, contact the high current driver product line at high_current_drivers.com@analog.com.

OUTLINE DIMENSIONS

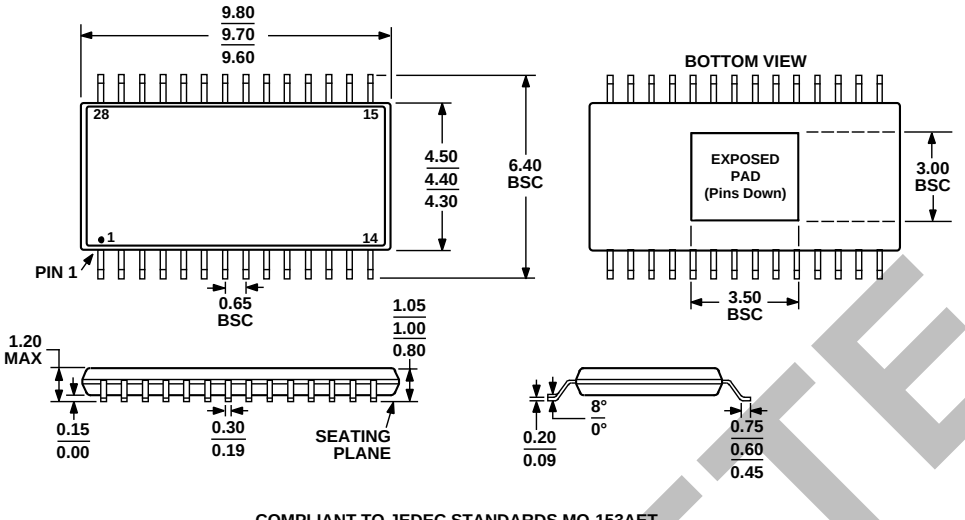

Figure 41. 28-Lead Thin Shrink Small Outline with Exposed Pad [TSSOP/EP], (RE-28-1), Dimensions shown in millimeters

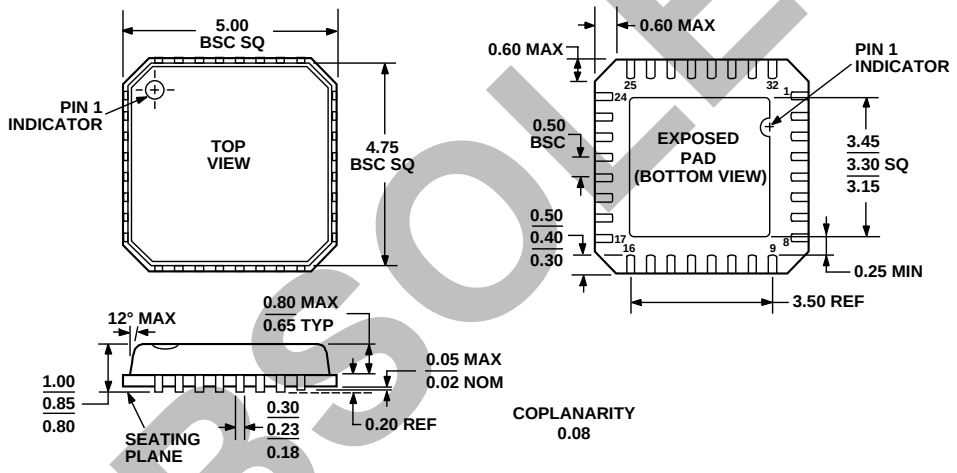

Figure 42. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ], 5 mm × 5 mm Body, Very Thin Quad (CP-32-3)—Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Outline
AD8392ARE	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP/EP)	RE-28-1
AD8392ARE-REEL	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP/EP)	RE-28-1
AD8392ARE-REEL7	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP/EP)	RE-28-1
AD8392AREZ[1]	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP/EP)	RE-28-1
AD8392AREZ-REEL[1]	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP/EP)	RE-28-1
AD8392AREZ-REEL7[1]	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP/EP)	RE-28-1
AD8392ACP-R2	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-32-3
AD8392ACP-REEL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-32-3
AD8392ACP-REEL7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-32-3

[1] Z = Pb-free part.