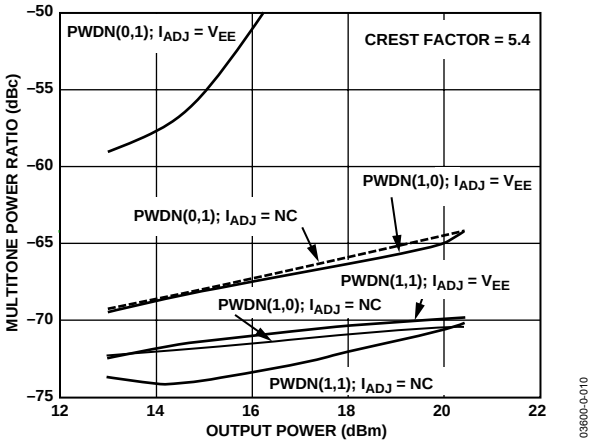

Figure 10. MTPR vs. Output Power; 970 kHz Empty Bin (26 kHz to 1.1 MHz)

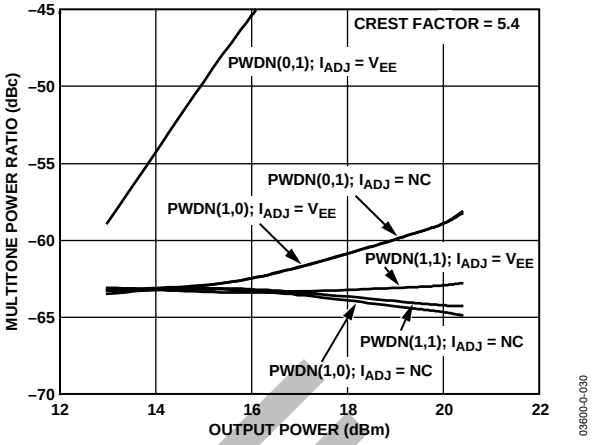

Figure 13. MTPR vs. Output Power; 1.75 MHz Empty Bin (26 kHz to 2.2 MHz)

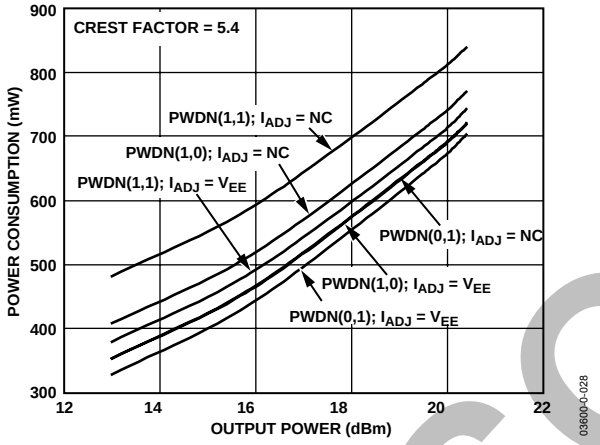

Figure 11. Power Consumption vs. Output Power (Includes Output Power Delivered to Load)

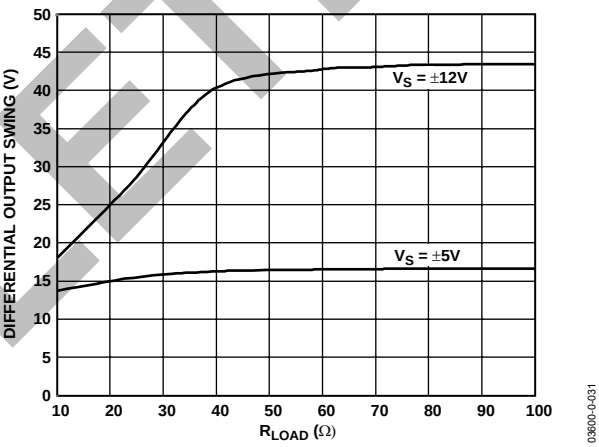

Figure 14. Differential Output Swing vs. R_{LOAD}

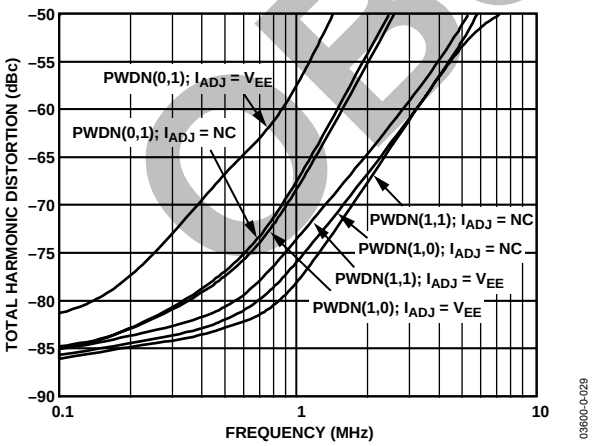

Figure 12. Total Harmonic Distortion vs. Frequency; V_S = ±12 V, V_{OUT} = 2 V p-p

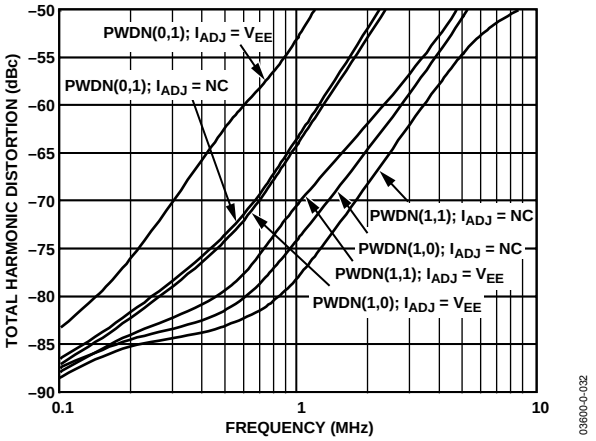

Figure 15. Total Harmonic Distortion vs. Frequency; V_S = ±5 V, V_{OUT} = 2 V p-p

LAYOUT, GROUNDING, AND BYPASSING

The first layout requirement is for a good solid ground plane that covers as much of the board area around the AD8390 as possible. The only exception to this is that the two input pins should be kept a few millimeters from the ground plane, and ground should be removed from inner layers and the opposite side of the board under the input traces. This minimizes the stray capacitance on these nodes and helps preserve the gain flatness versus frequency.

The power supply pins should be bypassed as close as possible to the device on a ground plane common with signal ground. Good high frequency, ceramic chip capacitors should be used. This bypassing should be done with a capacitance value of 0.01 µF to 0.1 µF for each supply. Low frequency bypassing should be provided with 10 µF tantalum capacitors from each supply to signal ground. The signal routing should be short and direct to avoid parasitic effects, particularly on traces connected to the amplifier inputs. Wherever there are complementary signals, a symmetrical layout should be provided to the extent possible to maximize the balance performance. When running differential signals over a long distance, the traces on the PCB should be close together.

POWER DISSIPATION AND THERMAL MANAGEMENT

The AD8390 was designed to be the most efficient class AB ADSL/ADSL2+ line driver available. Figure 11 shows the total power consumption (delivered line power and power consumed) of the AD8390 driving ADSL signals at varying output powers and power modes. To accurately determine the amount of power dissipated by the AD8390, it is necessary to subtract the power delivered to the load, matching losses, and transformer losses as follows:

$$P_{AD8390} = P_{supply,mW} - P_{load,mW} - P_{losses,mW} \quad (11)$$

where:

$P_{supply,mW}$ is the total supply power in mW drawn by the AD8390.

$P_{load,mW}$ is the power delivered into a 100 Ω twisted-pair line in mW.

$P_{losses,mW}$ is the power dissipated by the matching resistors and the transformer in mW.

While this discussion focuses mainly on ADSL applications, the same premise can be applied to determining the power dissipation of the AD8390 in any application.

To obtain optimum thermal performance from the AD8390 in either package, it is essential that the thermal pad be soldered to a ground plane with minimal thermal resistance. This is particularly true for dense circuit designs with multiple integrated circuits. Furthermore, the PCB should be designed in such a manner as to draw the heat away from the ICs. Figure 26 illustrates the relationship between thermal resistance (°C/W) and the copper area (mm^2) for the AD8390ACP soldered down to a 4-layer board with a given copper area.

Figure 26 can be used to help determine the copper board area required for proper thermal management of the AD8390. The power dissipation of the AD8390 can be computed using Equation 11. This number can then be inserted into the following equation to yield the required θ_{JA}:

$$\theta_{JA} = \frac{T_{RISE}}{P_{AD8390}} = \frac{^\circ C}{W} \quad (12)$$

where T_{RISE} is the delta from the maximum expected ambient temperature to the highest allowable die temperature. It is generally recommended that the maximum die temperature be limited to 125°C, and in no case should it be allowed to exceed 150°C.

Using the θ_{JA} computed in Equation 12, Figure 26 can be used to determine the minimum copper area required for proper thermal dissipation of the AD8390.

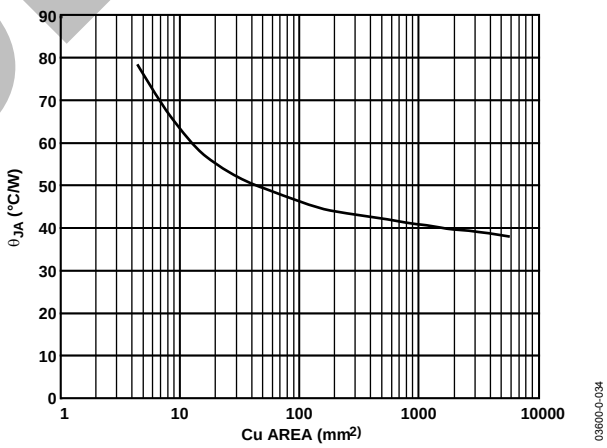

Figure 26. Thermal Resistance vs. Copper Area

OUTLINE DIMENSIONS

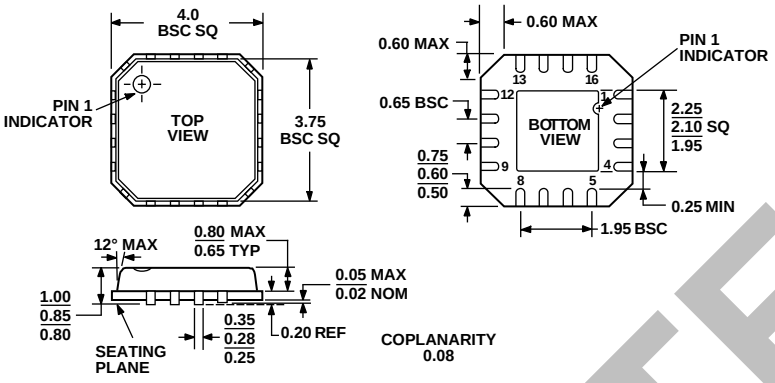

Figure 27. 4 × 4 mm 16-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-16)
Dimensions shown in millimeters

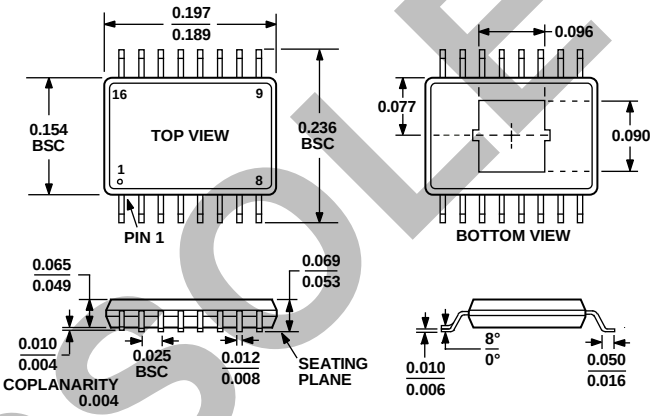

Figure 28. 16-Lead Shrink Small Outline Package, Exposed Pad [QSOP/EP]
(RC-16)
Dimensions shown in inches

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8390ACP-R2	–40°C to +85°C	16-Lead LFCSP	CP-16, 250 Piece Reel
AD8390ACP-REEL	–40°C to +85°C	16-Lead LFCSP	CP-16, 13" Tape and Reel
AD8390ACP-REEL7	–40°C to +85°C	16-Lead LFCSP	CP-16, 7" Tape and Reel
AD8390ACP-EVAL		Evaluation Board	LFCSP
AD8390ARC	–40°C to +85°C	16-Lead QSOP/EP	RC-16
AD8390ARC-REEL	–40°C to +85°C	16-Lead QSOP/EP	RC-16, 13" Tape and Reel
AD8390ARC-REEL7	–40°C to +85°C	16-Lead QSOP/EP	RC-16, 7" Tape and Reel
AD8390ARC-EVAL		Evaluation Board	QSOP/EP

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