SPECIFICATIONS

Test conditions, unless otherwise specified.

Table 1.

Parameter	Ratings
SUPPLY VOLTAGES	
AV_{DD}	5 V
DV_{DD}	5 V
PV_{DD}	12 V
AMBIENT TEMPERATURE	25°C
LOAD IMPEDANCE	6 Ω
CLOCK FREQUENCY	12.288 MHz
PGA GAIN	0 dB
MEASUREMENT BANDWIDTH	20 Hz to 20 kHz

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
R_{DS-ON}					
Per High-Side Transistor		260	355	mΩ	T = 25°C
Per Low-Side Transistor		210	265	mΩ	T = 25°C
MAXIMUM CURRENT THROUGH OUTx		5		A	Peak
THERMAL WARNING ACTIVE		135		°C	Die temperature
THERMAL SHUTDOWN ACTIVE		150		°C	Die temperature
RESTORE TEMPERATURE AFTER THERMAL SHUTDOWN		120		°C	Die temperature

Table 3. Performance Specifications

Parameter	Typ	Unit	Test Conditions/Comments
TOTAL HARMONIC DISTORTION AND NOISE (THD + N)	0.003	%	PGA = 0 dB, P_O = 1 W, 1 kHz
	0.006	%	PGA = 6 dB, P_O = 1 W, 1 kHz
	0.01	%	PGA = 12 dB, P_O = 1 W, 1 kHz
	0.02	%	PGA = 18 dB, P_O = 1 W, 1 kHz
SIGNAL-TO-NOISE RATIO (SNR)	105	dB	1 kHz, A-weighted, 0 dB referred to 1% THD + N output
DYNAMIC RANGE (DNR)	105	dB	1 kHz, A-weighted, –60 dB referred to 1% THD + N output
CROSSTALK (LEFT-TO-RIGHT OR RIGHT-TO-LEFT)	–100	dB	PGA = 0 dB, P_O = 5 W, 1 kHz

Table 4. DC Specifications

Parameter	Typ	Unit	Test Conditions/Comments
INPUT IMPEDANCE	20	kΩ	AINL, AINR input pins
OUTPUT DC OFFSET	±4	mV	Independent of PGA setting

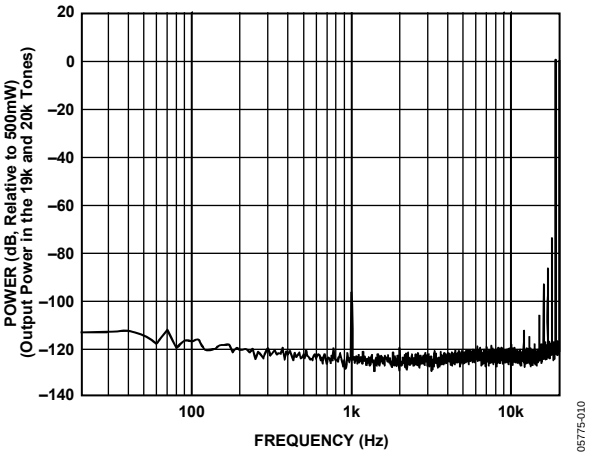

Figure 10. IMD for 19 kHz/20 kHz Twin-Tone Stimulus with 1 W Total Output Power

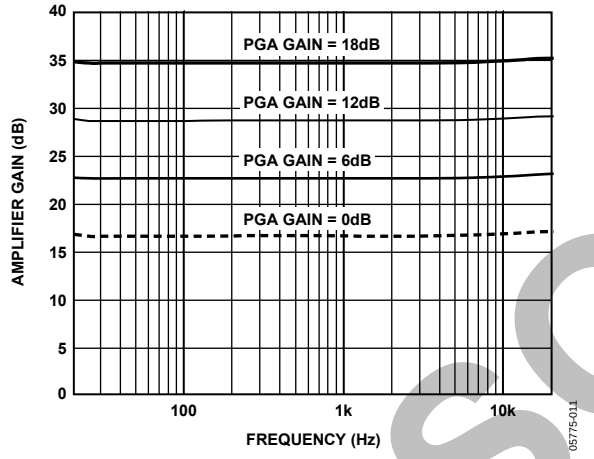

Figure 11. Amplifier Gain vs. Frequency, 6 Ω Load, PVDD = 12 V

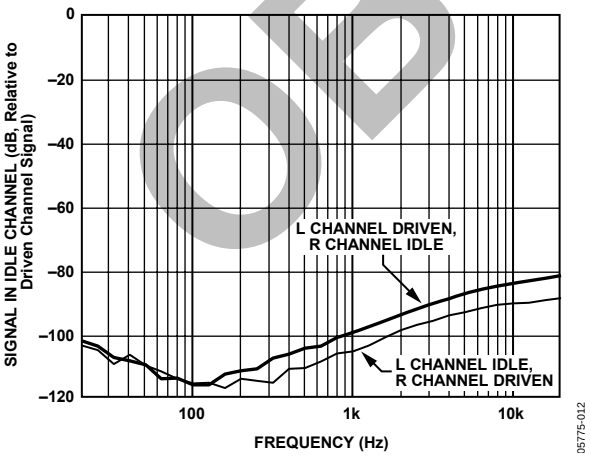

Figure 12. Channel Separation vs. Frequency, Driven Channel Has 1 W Output Power into 6 Ω Load

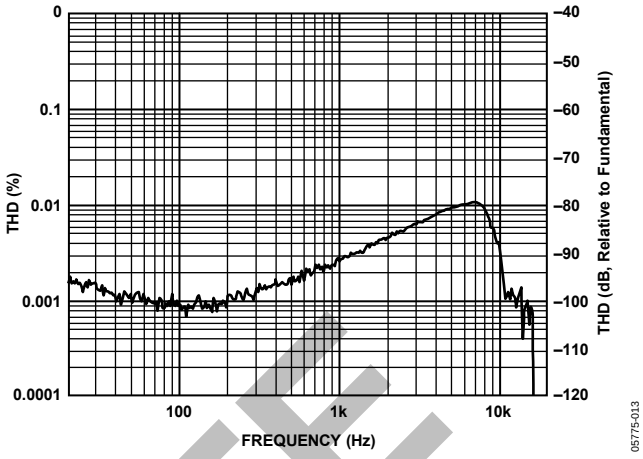

Figure 13. THD vs. Frequency, 1 W Output Power into 4 Ω Load, PVDD = 12 V

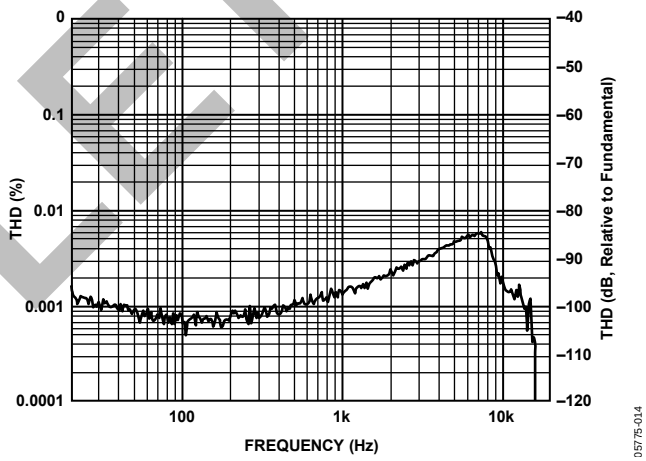

Figure 14. THD vs. Frequency, 1 W Output Power into 6 Ω Load, PVDD = 12 V

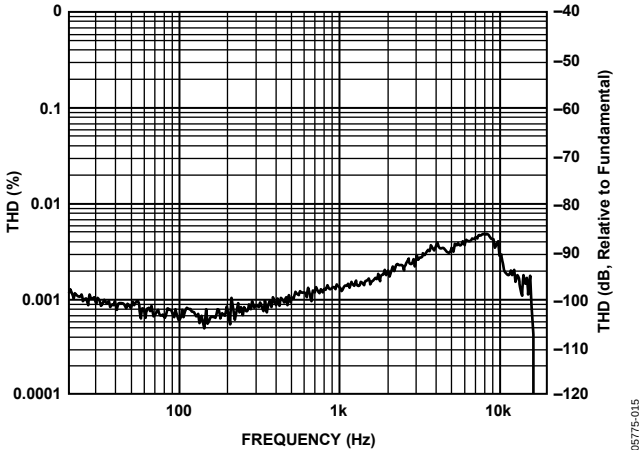

Figure 15. THD vs. Frequency, 1 W Output Power into 8 Ω Load, PVDD = 12 V

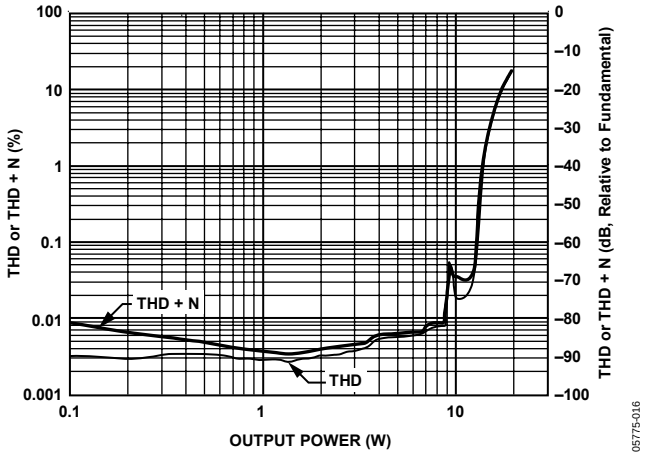

Figure 16. THD and THD + N vs. Output Power, 1 kHz Sine, 4 Ω Load, PVDD = 12 V

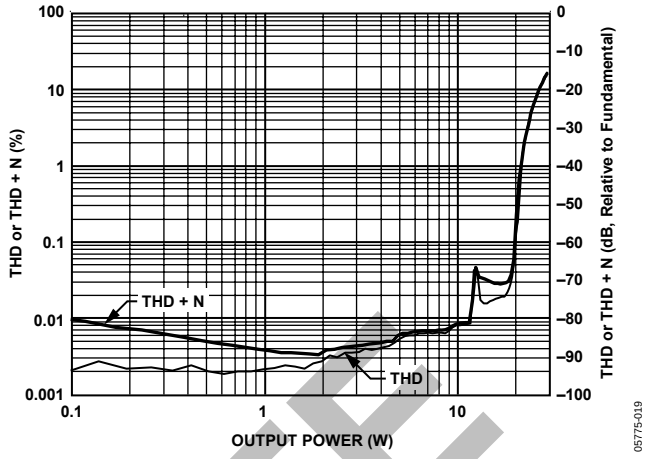

Figure 19. THD and THD + N vs. Output Power, 1 kHz Sine, 4 Ω Load, PVDD = 15 V

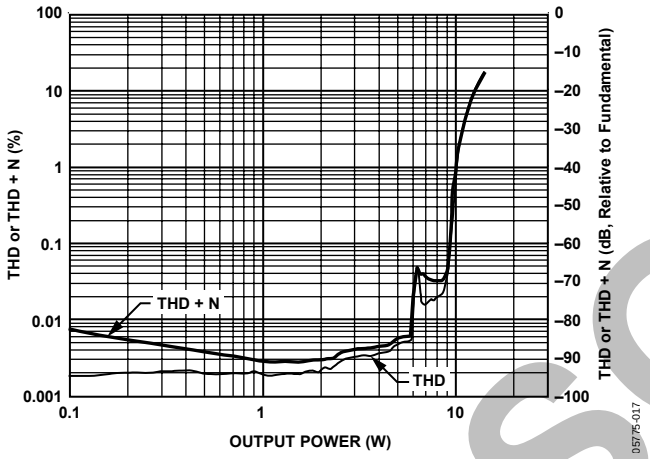

Figure 17. THD and THD + N vs. Output Power, 1 kHz Sine, 6 Ω Load, PVDD = 12 V

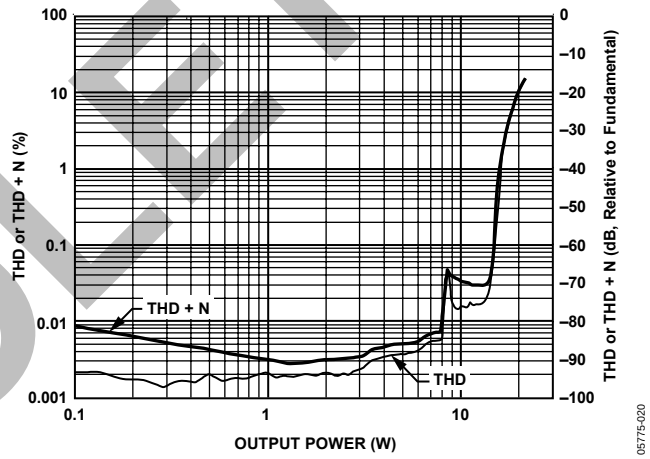

Figure 20. THD and THD + N vs. Output Power, 1 kHz Sine, 6 Ω Load, PVDD = 15 V

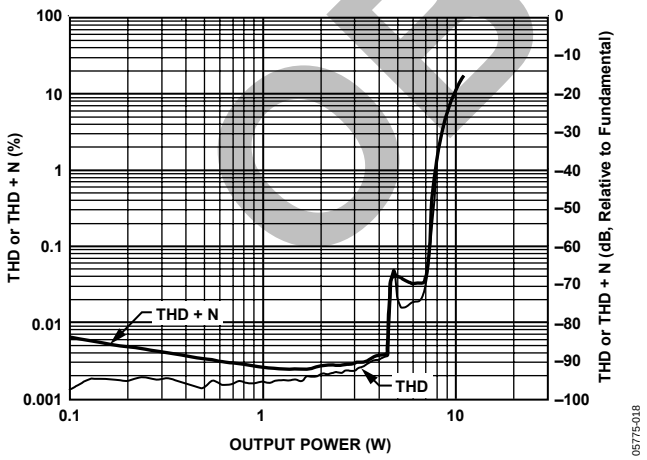

Figure 18. THD and THD + N vs. Output Power, 1 kHz Sine, 8 Ω Load, PVDD = 12 V

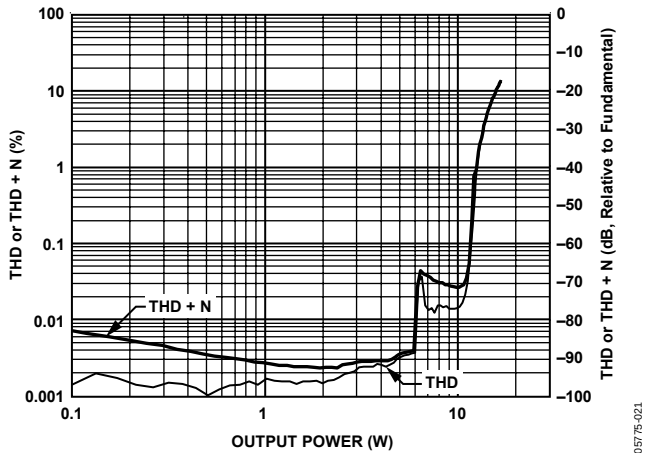

Figure 21. THD and THD + N vs. Output Power, 1 kHz Sine, 8 Ω Load, PVDD = 15 V

Output Transistor Nonoverlap Time

The AD1994 allows the user to select from one of eight different nonoverlap times, as shown in Figure 46. Nonoverlap time prevents or minimizes the period during which both the high-side and low-side devices are on simultaneously due to propagation delays and nonzero rise and fall times. If both the upper and lower portions of a half-bridge conduct simultaneously, there is a path directly from the power supply to ground and an induced current flow known as shoot-through. However, introducing this delay increases distortion by pushing the switching pattern further from an ideal two-state waveform. Selecting the nonoverlap delay requires a compromise between distortion and efficiency. The logic levels on the three delay control pins, DCTRL2, DCTRL1, and DCTRL0, set the nonoverlap time according to Table 12. The state of DCTRL[2:0] is read on the rising edge of $\overline{\text{RESET}}$ and should not be changed while $\overline{\text{RESET}}$ is logic high.

Table 12. Nonoverlap Time Settings

DCTRL2	DCTRL1	DCTRL0	Nonoverlap Time (ns)[1]
0	0	0	62
0	0	1	49
0	1	0	37
0	1	1	24
1	0	0	15
1	0	1	13.5
1	1	0	12
1	1	1	9

[1] Values are typical and are not production tested.

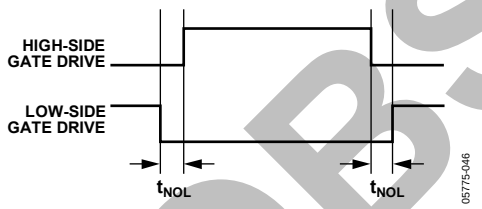

Figure 46. Half-Bridge Nonoverlap Delay Timing

The shortest setting (DCTRL[2:0] = 111) or the second shortest setting (DCTRL[2:0] = 111) is recommended for most applications. These two settings allow a small trade-off between efficiency and distortion. Longer nonoverlap times generally increase distortion while providing little or no decrease in shoot-through current.

CLOCKING

The AD1994 Σ-Δ modulator requires an external clock source with a nominal frequency of 12.288 MHz. This clock can come from a crystal or from an existing clock signal in the application circuit. The discrete time portions of the modulator run internally at 6.144 MHz, corresponding to 128 × f_S, where f_S = 48 kHz.

As mentioned in the Σ-Δ Modulator section, the modulator has a noise-shaping effect such that SNR is increased within the audio band by shifting modulator quantization noise upward in frequency. For external clock frequency of 12.288 MHz, the modulator's noise-shaping works in a manner that results in a flat noise floor at the amplifier output for frequencies 20 kHz and below. Above 20 kHz, the amplifier noise rises due to the spectral shaping of the modulator quantization noise. At very high frequencies, the noise floor levels off and decreases due to poles in the modulator noise-transfer function and in the external LC filter.

The clock frequency does not have to be exactly equal to 12.288 kHz and can vary by up to ±10%. For other rates, the noise corner scales linearly with frequency. When the modulator runs at a rate lower than nominal, the average power stage switching frequency decreases, the efficiency increases slightly, and the noise floor begins to rise at a slightly lower frequency. Likewise, a faster clock gives slightly increased bandwidth and slightly lower efficiency.

Using a Crystal Oscillator

The AD1994 can use a crystal connected to the CLKI and CLKO pins as a master clock source, as shown in Figure 47. The CLKI and CLKO pins connect to an internal inverter to create a full resonator. The typical values shown work in many applications, but the crystal manufacturer should provide the exact type and value of the capacitors and the resistor.

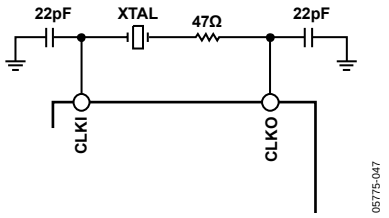

Figure 47. Crystal Connection

Using an External Clock Source

If a clock signal of the appropriate frequency already exists in the application circuit, connect it directly to CLKI and leave CLKO floating. The logic levels of the square wave should be compatible with those defined in Specifications section.

Large amounts of jitter on the clock input degrade performance. Whenever possible, avoid passing the clock signal though programmable logic and other circuits with unknown or variable propagation delay. In general, clock signals suitable for audio ADCs or DACs are also appropriate for use with the AD1994.

Clocking Multiple Amplifiers in Parallel

If there are multiple AD199x family amplifiers connected to the same PV_{DD} supply, use the same clock source (or synchronous derivatives) for each amplifier as previously described. Avoid clocking amplifiers from similar but asynchronous clocks if they use the same power supply because this can result in beat frequencies.

PROTECTION CIRCUITS AND ERROR REPORTING

Thermal Protection

The AD1994 features thermal protection. When the die temperature exceeds approximately 135°C, the thermal warning error output ($\overline{ERR1}$) is asserted. If the die temperature exceeds approximately 150°C, the thermal shutdown error output ($\overline{ERR2}$) is asserted. If this occurs, the part shuts down to prevent damage to the part. When the die temperature drops below approximately 120°C, the part returns to normal operation automatically and negates both error outputs.

Overcurrent Protection

The AD1994 features over current or short-circuit protection. If the current through any power transistors exceeds approximately 4 A, the part enters a mute state and the overcurrent error output ($\overline{ERR0}$) is asserted. This is a latched error and does not clear automatically. Restore normal operation and clear the error condition by either asserting and then negating $\overline{RESET}$ or by asserting and then negating $\overline{MUTE}$.

APPLICATION CIRCUITS

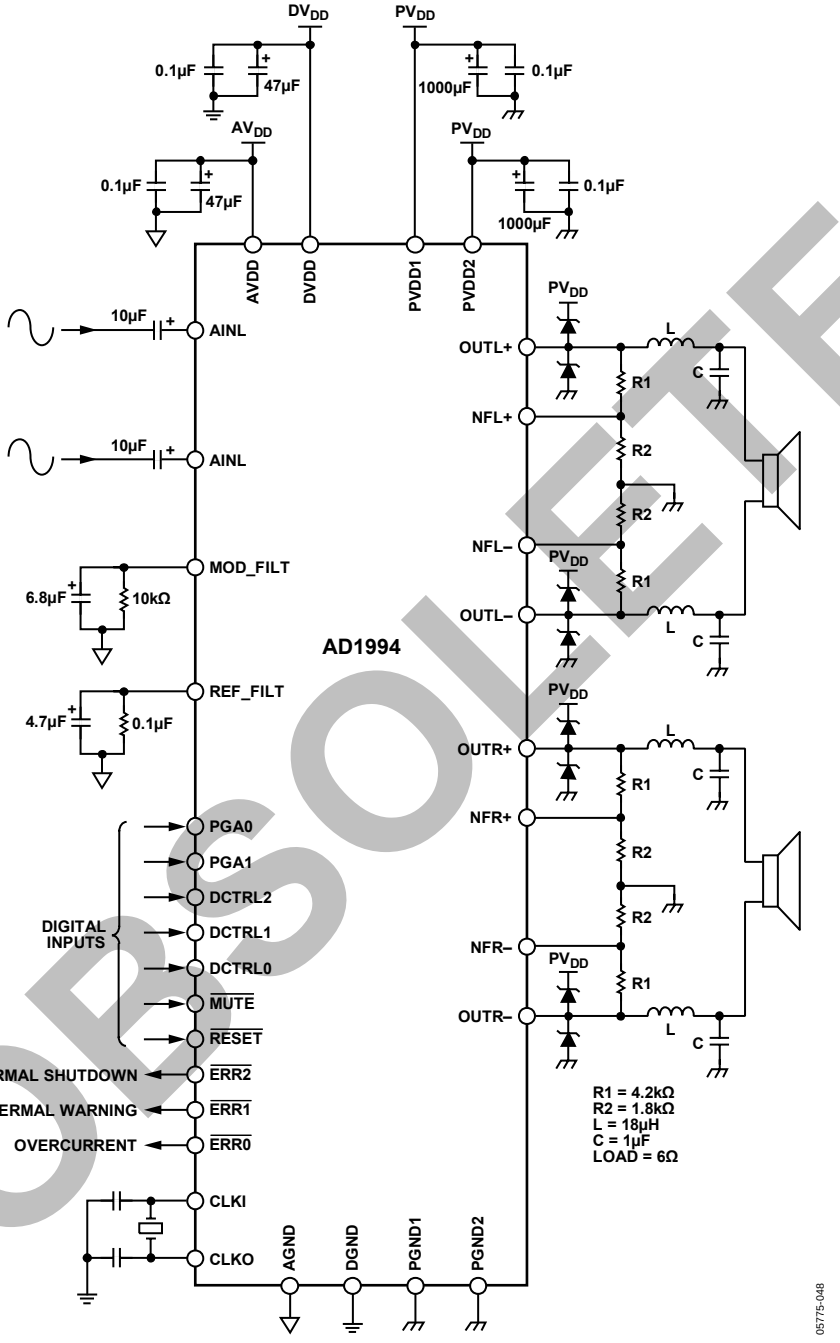

Figure 48. Typical Stereo Circuit

OUTLINE DIMENSIONS

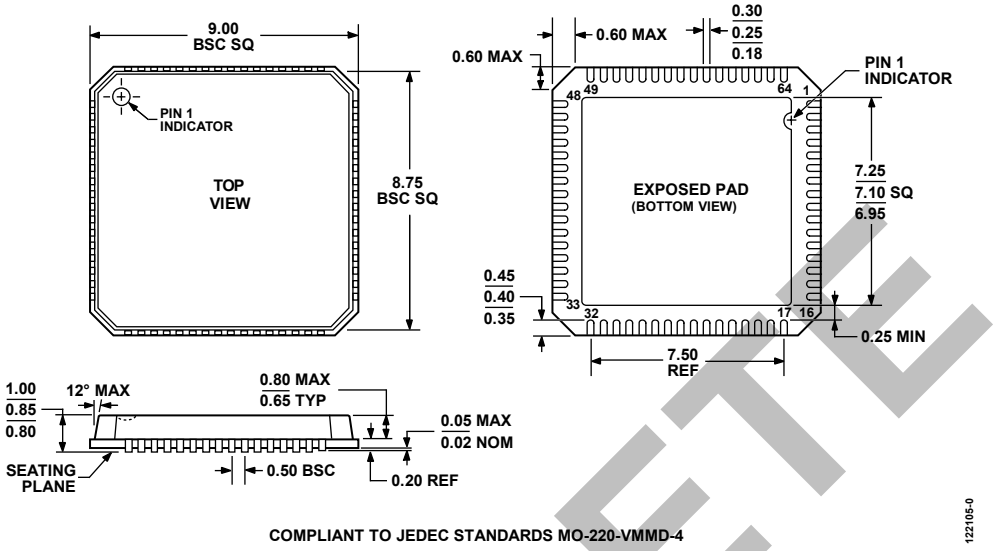

Figure 49. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-3)
Dimension shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1994ACPZ[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-3
AD1994ACPZRL[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ), 13″ Tape and Reel	CP-64-3
AD1994ACPZRL7[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ), 7″ Tape and Reel	CP-64-3
EVAL-AD1994EB		Evaluation Board	

[1] Z = Pb-free part.

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