ANALOG DEVICES

Low Cost 16-Bit Analog to Digital Converter

ADC1140

FEATURES
Guaranteed Nonlinearity: ±0.003% FSR max
35μs Maximum Conversion Time
Small Size 2" x 2" x 0.4"
Wide Power Supply Operation: ±12V to ±17V
Low Cost $149 (100s)

APPLICATIONS
Process Control Data Acquisition
Seismic Data Acquisition
Nuclear Instrumentation
Medical Instrumentation
Pulse Code Modulation Telemetry
Industrial Scales
Robotics

GENERAL DESCRIPTION
The ADC1140 is a low cost 16-bit successive-approximation analog-to-digital converter having a 35μs maximum conversion time. This converter provides high accuracy, high stability and low power consumption all in a 2" x 2" x 0.4" module.

High accuracy performance such as integral and differential nonlinearity of ±0.003% FSR max are both guaranteed. Guaranteed stability such as differential nonlinearity TC of ±2ppm/°C maximum, offset TC of ±30μV/°C maximum, gain TC of ±12ppm/°C maximum and power supply sensitivity of ±0.002% of FSR/°C are also provided by the ADC1140.

The ADC1140 makes extensive use of both integrated circuit and thin-film components to obtain excellent performance, small size and low cost. The internal 16-bit DAC incorporates Analog Devices' proprietary thin-film resistor technology and proprietary CMOS current-steering switches. A low noise reference, low power comparator and low power successive-approximation register are also used to optimize the ADC1140's design (shown in Figure 1).

The ADC1140 can operate with power supplies ranging from ±12V to ±17V and has provisions for a user supplied external reference. Four analog input voltage ranges are selectable via pin programming: ±5V, ±10V, 0 to +5V and 0 to +10V. Bipolar coding is provided in the offset binary and two's complement formats with unipolar coding displayed in true binary.

Figure 1. ADC1140 Functional Block Diagram

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## SPECIFICATIONS

(typical @ $+25^\circ C \pm V_S = \pm 15V$, $V_{CC} = +5V$, $V_{REF} = +10.0V$ unless otherwise specified)

<table>
<thead>
<tr>
<th>Model</th>
<th>ADC1140</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESOLUTION</td>
<td>16 Bits</td>
</tr>
<tr>
<td>CONVERSION TIME</td>
<td>$35\mu s$ max</td>
</tr>
</tbody>
</table>

### ACCURACY

- **Nonlinearity Error**
  - $\pm 0.003\%$ FSR$^2$ max
- **Differential Nonlinearity Error**
  - $\pm 0.003\%$ FSR$^2$ max

### STABILITY

- **Differential Nonlinearity**
  - $\pm 2ppm/\degree C$ max
- **Gain (with internal reference)**
  - $\pm 12ppm/\degree C$ max
- **(without internal reference)**
  - $\pm 4ppm/\degree C$ max
- **Unipolar Offset**
  - $\pm 30uV/\degree C$ max
- **Bipolar Offset**
  - $\pm 7ppm/\degree C$ max

### POWER SUPPLY SENSITIVITY

- $\pm 0.002\%$ FSR/$\% V_S$

### ANALOG INPUT

- **Voltage Ranges**
  - Bipolar: $\pm 10V$
  - Unipolar: $0$ to $+5V$, $0$ to $+10V$
- **Input Resistance**
  - Bipolar: $2.5k\Omega$
  - Unipolar: $5.0k\Omega$
- **External Reference Input**
  - **Voltage Range**
    - $0$ to $+10V$
- **Input Resistance**
  - $2.5k\Omega$

### DIGITAL INPUT

- **Convert Command Positive Pulse**
  - $100ns$ Width min
- **Logic Loading**
  - $1TTL$ Load

### DIGITAL OUTPUT

- **Parallel Output Data**
  - **Unipolar**
  - Binary (BIN)
  - **Bipolar**
  - Offset Binary (OBIN) Two’s Complement
- **Output Drive**
  - **Status**
  - $1TTL$ Load
  - Logic “1” During Conversion
- **Output Drive**
  - $1TTL$ Load

### INTERNAL REFERENCE VOLTAGE

- **External Load Current**
  - $2mA$ max
- **Temperature Stability**
  - $\pm 8.5ppm/\degree C$ max

### POWER REQUIREMENTS

- **Voltage (Rated Performance)**
  - $\pm 15V \pm 3\%$, $+5V \pm 3\%$
- **Voltage (Operating)**
  - $\pm 12V$ to $+17V$, $+4.75V$ to $+5.25V$
  - $\pm 25mA$
- **Supply Current Drain**
  - $150mA$

### TEMPERATURE RANGE

- **Specified**
  - $0$ to $+70^\circ C$
- **Operating**
  - $-25^\circ C$ to $+85^\circ C$
- **Storage**
  - $-55^\circ C$ to $+85^\circ C$

### SIZE

- **Weight**
  - $1.2$ oz ($33g$)

### PRICE

- **(1-24)**
  - $\$199$
- **(25-99)**
  - $\$169$
- **(100+)**
  - $\$149$

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1. Offset and gain error are adjustable to zero by means of external potentiometers. See Figure 3 for proper connection.
2. FSR means Full Scale Range.
3. Rated performance is specified with $+10.0V$ reference.

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## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### MATING CONNECTORS

- **AC1577 (2 REQUIRED)**

### PIN DESIGNATIONS

### OTHER HIGH RESOLUTION PRODUCTS FROM ANALOG DEVICES:

- 14-Bit/15-Bit Sampling A/D Converters: DAS1152/53
  - $25kHz$ (14-Bit)/20kHz (15-Bit) throughput rates
  - Second Source to A/D/A/M824 and A/D/A/M825 Modules
- 14-Bit/15-Bit Low Level Data Acquisition Systems: DAS1155/56
  - $25kHz$ (14-Bit)/20kHz (15-Bit) throughput rates
  - High Performance PGA (1V/V–1000V/V), SHA and A/D Converter
- 14-Bit Sample-Hold Amplifier: SHA1144
  - Acquisition Time: $8\mu s$ max to $\pm 0.003\%$ (20V step)

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*Recommended Power Supply: Analog Devices Model 923.*

Specifications subject to change without notice.
OPERATION
For operation, the only connections necessary to the ADC1140 are the power supplies, the analog input, the convert command pulse and a connection between pins 25 and 26 in order to supply the internal precision reference voltage to the DAC (see Figure 2). For operation with an external reference see Figure 7.

ANALOG INPUT PROGRAMMING
The analog input section consists of three analog input terminals. Analog input range selection is accomplished by pin programming as shown in Table 1. In the unipolar mode, a 0 to +10V or a 0 to +5V input signal develops a 0 to +2mA current that is compared to the 0 to -2mA (shown in Figure 2) current output of the DAC. In the bipolar mode, a +1mA offset current from the reference is applied to the comparator input via pin programming connections. The ADC1140 can then accept either ±5V or ±10V inputs. These inputs again will be converted to current and compared with the DAC's 0 to -2mA current output.

Table 1. Analog Input Voltage Pin Programming

<table>
<thead>
<tr>
<th>Input Signal</th>
<th>Connect Input</th>
<th>Connect Pin 26 To Pin(s)</th>
<th>Connect Pin 30 To Pin(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>±10V</td>
<td>OBIT, Two's Comp</td>
<td>28, 27</td>
<td>29, 2</td>
</tr>
<tr>
<td>±5V</td>
<td>OBIT, Two's Comp</td>
<td>29, 27</td>
<td>28, 2</td>
</tr>
<tr>
<td>0 to +5V</td>
<td>BIN</td>
<td>27, 28, 29</td>
<td>Open 2</td>
</tr>
<tr>
<td>0 to +10V</td>
<td>BIN</td>
<td>27, 28</td>
<td>Open 29, 2</td>
</tr>
</tbody>
</table>

*If Internal Reference is used, Pins 25 and 26 must be connected together (see Figure 3 and the gain calibration section).

OPTION OFFSET & GAIN CALIBRATION
Initial offset and gain errors can be adjusted to zero by potentiometers as shown in Figure 3. Proper offset and gain calibration requires great care and the use of an accurate and stable voltage reference. The voltage standard used as a signal source must be very stable. It should be capable of being set to within 1µV of the desired value at both ends of its range. The potentiometers selected should be of the good quality Cermet type. Multi-turn potentiometers having ten to fifteen turns and 100ppm/°C temperature coefficients will be adequate. The temperature coefficients contributed by these Cermet potentiometers will be less than 0.1ppm/°C. By adjusting the offset first, gain and offset adjustments will remain independent of each other.

OFFSET CALIBRATION
For 0 to +10V range, set the input voltage precisely to +76µV; for 0 to +5V range, set it at +38µV. Adjust the zero potentiometer until the binary coded converter is just on the verge of switching from 000 . . . 00 to 000 . . . 01.

For ±5V range, set the input voltage precisely to -4.999724V; for ±10V range, set it at -9.999847V. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 000 . . . 00 to 000 . . . 01 and the two's comp. coded units are just on the verge of switching from 000 . . . 00 to 000 . . . 01.

GAIN CALIBRATION
Set the input voltage precisely at 4.99977V for 0 to +10V input range, ±4.99977V for ±5V input range, or ±4.99977V for 0 to ±5V input range, adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 111 . . . 0 to 111 . . . 1 and two's comp. coded units are just on the verge of switching from 011 . . . 10 to 011 . . . 11. Note that these values are 1 1/2 LSBs less than nominal full scale.

POWER SUPPLY AND GROUNDING CONNECTIONS
The analog power ground (pin 30) and digital ground (pin 2) are not connected internally. The connection must be made externally. The choice of an optimum "star" point is an important consideration in avoiding ground loops and to minimize coupling between the analog and digital sections. One suggested approach is shown in Figure 4.

Because the ADC1140 contains high quality tantalum capacitors on each of the power supply inputs to ground, external bypass capacitors are not required.

ADC1140 TIMING
Conversion is initiated with the negative going edge of the Convert Command pulse as shown in Figure 5. The Convert Command pulse width must be a minimum of 100ns. Once the conversion process is initiated, it cannot be retriggered until after the end of conversion.

With the negative edge of the Convert Command pulse, all internal logic is reset. The MSB is set low with the remaining digital outputs set to logic high state, and the status line is set high and remains high thru the full conversion cycle.
During conversion each bit, starting with the MSB, is sequentially switched low at the rising edge of the internal clock. The DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 16-bit conversion taking $3.5\mu s$ maximum. At this time, the STATUS line goes low signifying that the low conversion is complete.

![Figure 5. ADC1140 Timing Diagram](image)

**ANALOG INPUT/OUTPUT RELATIONSHIPS**

The ADC1140 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two’s complement output codes. The most significant bit (MSB) is displayed on pin 4 for the binary and offset binary codes or on pin 3 for the two’s complement code. Table 2 shows the unipolar analog input/digital output relationships. Table 3 shows the bipolar analog input/digital output relationships for offset binary code and two’s complement codes.

![Table 2. Unipolar Input/Output Relationships](image)

**Table 2. Unipolar Input/Output Relationships**

<table>
<thead>
<tr>
<th>Analog Input</th>
<th>Offset Binary Code</th>
<th>2’s Complement Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Range</td>
<td>Range</td>
<td></td>
</tr>
<tr>
<td>0 to +5V</td>
<td>1111 1111 1111 1111</td>
<td>1111 1111 1111 1111</td>
</tr>
<tr>
<td>+4.999924V</td>
<td>+9.99985V</td>
<td></td>
</tr>
<tr>
<td>+2.50000V</td>
<td>+5.00000V</td>
<td></td>
</tr>
<tr>
<td>+1.25000V</td>
<td>+2.50000V</td>
<td></td>
</tr>
<tr>
<td>+0.62500V</td>
<td>+1.25000V</td>
<td></td>
</tr>
<tr>
<td>+0.000076V</td>
<td>+0.000153V</td>
<td></td>
</tr>
<tr>
<td>+0.000000V</td>
<td>+0.000000V</td>
<td></td>
</tr>
</tbody>
</table>

**Table 3. Bipolar Input/Output Relationships**

<table>
<thead>
<tr>
<th>Analog Input</th>
<th>Digital Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Range</td>
<td>Offset Binary Code</td>
</tr>
<tr>
<td>0 to +5V</td>
<td>1111 1111 1111 1111</td>
</tr>
<tr>
<td>+4.999924V</td>
<td>+9.99985V</td>
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</tr>
<tr>
<td>+0.000076V</td>
<td>+0.000153V</td>
</tr>
<tr>
<td>+0.000000V</td>
<td>+0.000000V</td>
</tr>
</tbody>
</table>

**HIGH RESOLUTION DATA ACQUISITION SYSTEM**

Shown in Figure 6 is a high resolution data acquisition system. Here the SHA1144, a high resolution sample-hold amplifier, is used to drive the ADC1140. Conversion is initiated by the negative edge of the convert command pulse. At this time the STATUS pulse goes low causing the SHA1144 to go from the sample mode to the hold mode. When the conversion is complete, $3.5\mu s$ later, the STATUS pulse goes low, thus placing the SHA1144 in the sample mode.

![Figure 6. High Resolution Data Acquisition System](image)

**EXTERNAL REFERENCE**

The ADC1140 is capable of operating with an external $+10.0V$ reference. Simply disconnect the gain trim potentiometer from pin 26 and connect it to the external reference as shown in Figure 7. The external reference output must appear as a low impedance and must remain very stable during conversion to ensure that accuracy is maintained. Gain error is adjusted as previously discussed in the gain calibration section.

![Figure 7. External Reference](image)

**PIA INTERFACE**

The ADC1140 can be used with a PIA to interface directly to a microprocessor. As shown in Figure 8 the 16-bit output of the ADC1140 is split into two 8-bit bytes. Part A of the PIA is programmed to read the eight most-significant-bits while Part B reads the eight least-significant-bits. Output CB2 is used to start the ADC1140 conversion process. CB1, of the PIA, is used to sense the STATUS of the ADC1140 so that the end of conversions can be determined. The control bus, address bus, and data bus are then connected directly to the microprocessor. With the use of PIAs, control of one or more ADC1140s can be accomplished in many different configurations.

![Figure 8. ADC1140 Interface to PIA](image)