ANALOG DEVICES

High Speed Digital to Analog Converter

DAC1108

PRELIMINARY TECHNICAL DATA

FEATURES
- 12 Bit Resolution
- Fast Settling
  - to 0.05% in 60ns
  - to 0.01% in 150ns
- Adjustment Free Operation
- Linearity Error: ±½LSB Max
- Small Size: 2" x 2" x 0.4"

GENERAL DESCRIPTION

The DAC1108 is a high speed, current output digital-to-analog converter with 12-bit resolution and accuracy. The very fast settling times to 0.05% accuracy of 60ns and to 0.01% accuracy of 150ns make it ideal for use in high speed applications such as computer driven displays, automatic test equipment, and function generators. In addition to the ±½LSB maximum linearity error, the DAC1108 features temperature coefficients of 30ppm/°C for gain and 8ppm/°C for linearity.

Everything needed to perform high speed conversions is contained in the compact 2" x 2" x 0.4" package of the DAC1108. Included are a precision temperature compensated reference source, high speed current switches and a carefully trimmed network of weighting resistors. Because of the inherent stability and careful factory adjustment of this device, no external zero or gain adjustment potentiometers are required.

The digital inputs of the DAC1108 are fully DTL/TTL compatible. Binary code is used for unipolar operation and Offset Binary code is used for bipolar operation. The current output of this device can be applied directly to an external resistor to develop a voltage output or it can be applied to the input of a fast settling op amp if amplification or impedance transformation is desired.

INPUT CONSIDERATIONS

The binary weighted current sources which form the basis of the digital to analog conversion process are directly switched by their associated input bits. A change in the converter's current output will begin to occur approximately 10nsec after a new digital word is applied. Because of this extremely fast response, time skew in the digital input can result in momentary erroneous outputs or "glitches". Consider, for example, the case of a transition from 1000 . . . 0 to 0111 . . . 1, a step of only one LSB. If the MSB turns to a "0" before the rest of the bits have turned to "1"'s, the input will momentarily be 0000 . . . 0 and the converter will start to respond accordingly as shown below in Figure 1.

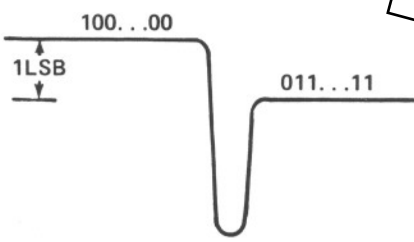


Figure 1. Switching Transient Caused by Time Skew

These switching transients will be minimized if the digital input data time skew is held to less than 5nsec.

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577
West Coast 213/595-1783
Mid-West 312/894-3300
Texas 214/231-5094

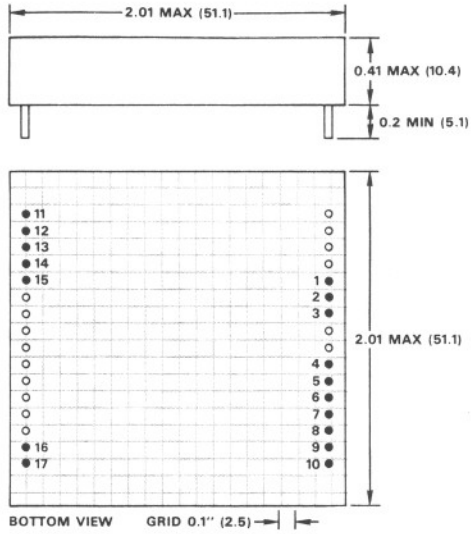
SPECIFICATIONS (typical @ +25°C and rated supply voltages, unless otherwise noted)

RESOLUTION	12 Bits
DIGITAL INPUT	TTL Compatible
0V ≤ Logic '0' ≤ 0.5V	@ -3.2mA max
2.5V ≤ Logic '1' ≤ 15V	@ 80μA max
INPUT CODES	
Unipolar	Binary
Bipolar	Offset Binary
OUTPUT RANGES	0 to +5mA ±2.5mA
OUTPUT VOLTAGE COMPLIANCE[1]	±1.2V
OUTPUT IMPEDANCE	510Ω ±2%
SETTLING TIME	
to ±0.01% Accuracy	150ns
to ±0.05% Accuracy	60ns
ABSOLUTE ACCURACY	
Full Scale	±0.1%
Offset	±20nA
LINEARITY	±½LSB max
TEMPERATURE COEFFICIENT	
Gain	±30ppm/°C
Linearity	±8ppm/°C
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55 to +125°C
POWER REQUIREMENTS	+15V ±5% @ 42mA max -15V ±5% @ 10mA max
POWER SUPPLY SENSITIVITY	
of Gain to +15V Supply	0.01%/%ΔV_S
of Gain to -15V Supply	0.01%/%ΔV_S
PRICE (1-9)	$122

[1] ±1V for rated dynamic performance.
Specifications subject to change without notice.

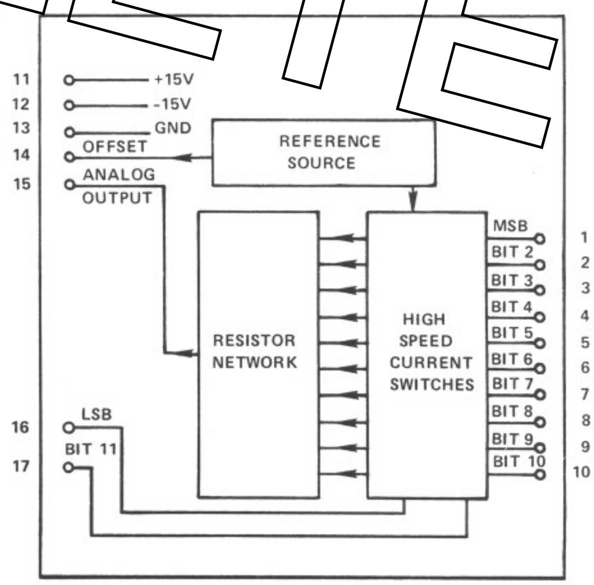
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE:
Terminal pins installed only in shaded hole locations.
All pins are gold plated half-hard brass, (MIL-G-45 204), 0.019'' ±0.001'' (0.48 ±0.03) dia.

BLOCK DIAGRAM AND PIN DESIGNATIONS



DIGITAL INPUTS

The DAC1108 is fully TTL/DTL compatible with each input bit representing two standard TTL loads. The logic levels of

$$0V \leq \text{Logic '0'} \leq 0.8V$$
$$+2V \leq \text{Logic '1'} \leq 15V \text{ (Absolute Max)}$$

are also compatible with CMOS logic systems. When using this device in a CMOS system, standard CMOS/TTL interface rules must be observed to insure that the driving gate is capable of sinking at least 3.2mA.

The simple addition of an external inverter ahead of the MSB input terminal, as shown below in Figure 2, allows the bipolar Two's Complement code to be used.

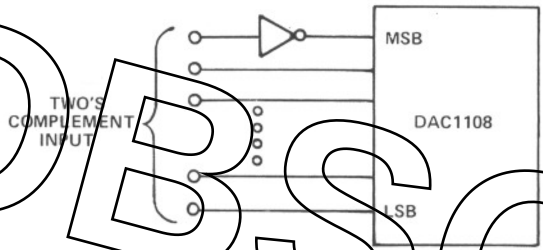


Figure 2. Two's Complement Input Connection

OUTPUT CHARACTERISTICS

The output of the DAC1108 represents the sum of the currents produced by the individual binary-weighted current sources in response to the digital input word. This current varies from 0 to +5mA. In order to produce the half scale offset needed for bipolar outputs, a current of exactly -2.5mA must be added to the output. Such a current is generated internally and is available at pin 14. The analog outputs which are produced by various digital inputs are shown in the following tables.

Digital Input	Analog Output
111. 111	+4.999mA
100. 000	+2.500mA
000. 001	+1.22μA
000. 000	0mA

UNIPOLAR

Digital Input	Analog Output
111. 111	+2.499mA
100. 000	0mA
000. 000	-2.500mA

BIPOLAR

Figures 3 and 4 illustrate the converter's output impedance characteristics for unipolar and bipolar operation.

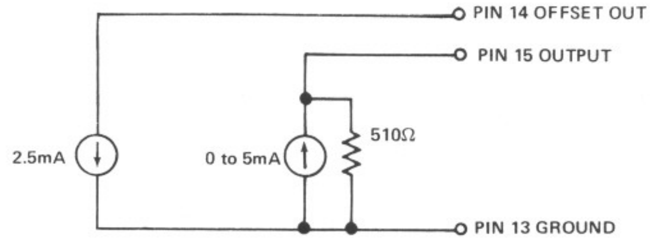


Figure 3. Equivalent Circuit DAC1108 (Unipolar)

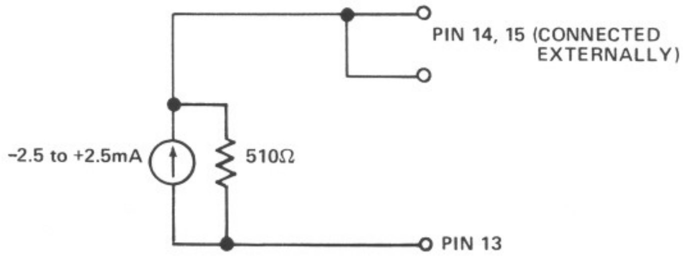


Figure 4. Equivalent Circuit DAC1108 (Bipolar)

OUTPUT CONNECTIONS

The circuits used to develop an output voltage across a resistor are shown below in Figures 5 and 6 for unipolar and bipolar operation.

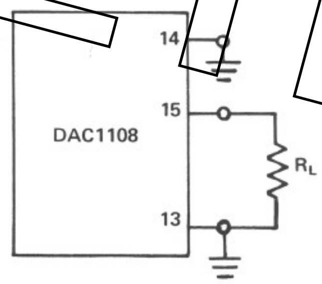


Figure 5. Voltage Output with Load Resistor (Unipolar)

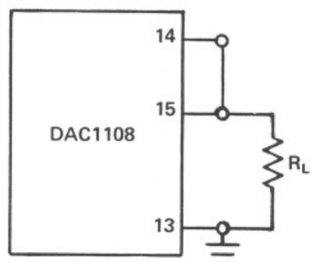


Figure 6. Voltage Output with Load Resistor (Bipolar)

In both cases, the output voltage is limited to ±1.2V max. By referring to Figures 3 and 4, the user can readily compute the value of R_L needed to produce the desired full scale voltage. For example, a 329Ω resistor will develop a 0 to +1V F.S. unipolar output and a 1.855kΩ resistor will develop a ±1V F.S. bipolar output.

The DAC1108 may be used in conjunction with a high speed external op amp when outputs greater than ±1.2V and 5mA are needed. Because current output converters such as the DAC1108 are not ideal current sources, the op amp does not operate in a unity gain configuration. Figure 7 below shows, in simplified form, a unipolar DAC1108 driving an op amp.

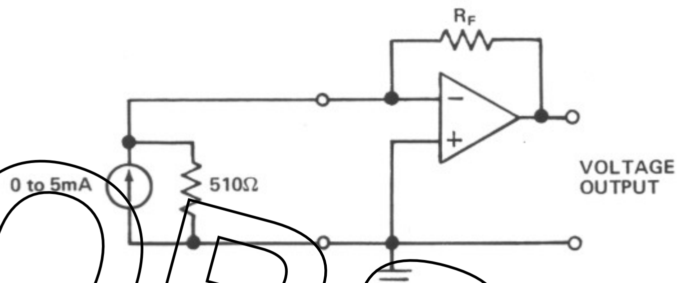


Figure 7. Voltage Output with an Op Amp Simplified Diagram

Because of the 510Ω output impedance, the closed loop gain becomes $1 + R_f/510$ instead of 1. For example with an R_f of 2kΩ the closed loop gain is 4.92.

This can complicate the job of selecting a suitable op amp since most manufacturers specify settling time at unity gain. One extremely fast op amp that performs as well at gains of 2 to 6 as it does at unity gain is the Analog Devices' model 50 differential input, FET amplifier. The model 50 will settle to 0.05% accuracy in a maximum of 200nsec. The high current output of this device (100mA) also makes it ideal for use with the DAC1108 in CRT deflection applications.

Sometimes space or budgetary considerations dictate that an IC rather than a modular op amp be used. In these cases the AD509K fast settling IC op amp is recommended. The AD509K maintains its guaranteed maximum settling time specification (500nsec to 0.1%) even at the closed loop gains encountered with the DAC1108. Furthermore, when the closed loop gain is greater than 3, no external compensating components are required.

Figures 8 and 9 below show the proper means of connecting the converter to an op amp for unipolar and bipolar operation.

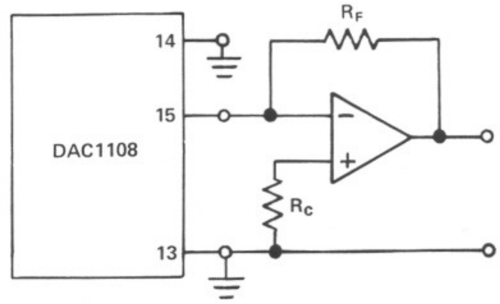


Figure 8. Connections to an External Op Amp (Unipolar)

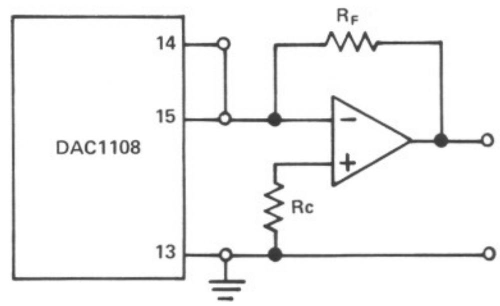


Figure 9. Connections to an External Op Amp (Bipolar)

The resistor Rc is used with the AD509K for bias current compensation. Because of the low bias currents inherent with the model 50, Rc is unnecessary and the noninverting input is connected directly to ground.

Great care must be taken in laying out the circuits of Figures 8 and 9 to assure true high speed performance. Several of the most important considerations are listed below:

1. Keep leads, especially those between the converter output and op amp summing junction, as short as possible to prevent the introduction of noise.
2. Orient components to minimize stray capacitance.
3. Carefully bypass power supplies to the op amp.
4. Select suitable components such as metal film resistors with their low capacitance and low stray inductance.
5. Design the signal and power supply ground circuits so as to prevent the introduction of extraneous voltages in ground signal path.
6. Use separate returns for analog and digital grounds. The DAC1108 and op amp power supply returns go to analog ground; any logic circuits that precede the converter go to digital ground.

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