ANALOG DEVICES

Wideband, Fast Settling Op Amp

AD840

FEATURES

Wideband AC Performance
- Gain Bandwidth Product: 400 MHz (Gain ≥ 10)
- Fast Settling: 100 ns to 0.01% for a 10 V Step
- Slew Rate: 400 V/μs
- Stable at Gains of 10 or Greater
- Full Power Bandwidth: 6.4 MHz for 20 V p-p into a 500 Ω Load

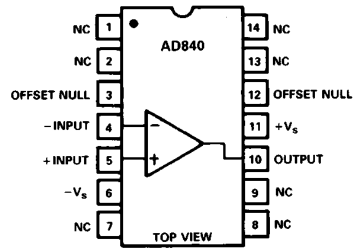
Precision DC Performance
- Input Offset Voltage: 0.3 mV max
- Input Offset Drift: 3 μV/°C typ
- Input Voltage Noise: 4 nV/√Hz
- Open-Loop Gain: 130 V/mV into a 1 kΩ Load
- Output Current: 50 mA min
- Supply Current: 12 mA max

APPLICATIONS

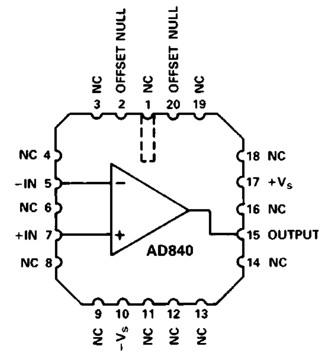
Video and Pulse Amplifiers
DAC and ADC Buffers
Line Drivers
Available in 14-Pin Plastic DIP, Hermetic Cerdip and 20-Pin LCC Packages and in Chip Form
MIL-STD-883B Processing Available

CONNECTION DIAGRAMS

Plastic DIP (N) Package and Cerdip (Q) Package



LCC (E) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD840 is a member of the Analog Devices' family of wide bandwidth operational amplifiers. This high speed/high precision family includes, among others, the AD841, which is unity-gain stable, and the AD842, which is stable at a gain of two or greater and has 100 mA minimum output current drive. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 400 MHz gain bandwidth product, the AD840 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in 100 ns for a 10 volt step.

The AD840 remains stable over its full operating temperature range at closed-loop gains of 10 or greater. It also offers a low quiescent current of 12 mA maximum, a minimum output current drive capability of 50 mA, a low input voltage noise of 4 nV/√Hz and a low input offset voltage of 0.3 mV maximum (AD840K).

The 400 V/μs slew rate of the AD840, along with its 400 MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is ideally suited for use in high frequency signal conditioning circuits and wide bandwidth active filters. The extremely rapid settling time of the AD840 makes it the preferred choice for data acquisition applications which require 12-bit accuracy. The AD840 is also appropriate for other applications such as high speed DAC and ADC buffer amplifiers and other wide bandwidth circuitry.

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD840 make it ideal for DAC and ADC buffers, line drivers and all types of video instrumentation circuitry.
2. The AD840 is truly a precision amplifier. It offers 12-bit accuracy to 0.01% or better and wide bandwidth, performance previously available only in hybrids.
3. The AD840's thermally balanced layout and the high speed of the CB process allow the AD840 to settle to 0.01% in 100 ns without the long "tails" that occur with other fast op amps.
4. Laser wafer trimming reduces the input offset voltage to 0.3 mV max on the K grade, thus eliminating the need for external offset nulling in many applications. Offset null pins are provided for additional versatility.
5. Full differential inputs provide outstanding performance in all standard high frequency op amp applications where circuit gain will be 10 or greater.
6. The AD840 is an enhanced replacement for the HA2540.

REV. C

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Tel: 617/329-4700 Fax: 617/326-8703

AD840–SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD840J Min	AD840J Typ	AD840J Max	AD840K Min	AD840K Typ	AD840K Max	AD840S Min	AD840S Typ	AD840S Max	Units
INPUT OFFSET VOLTAGE[1]			0.2	**1**		0.1	**0.3**		0.2	**1**	mV
	T_{MIN}–T_{MAX}			1.5			**0.7**			2	mV
Offset Drift			5			3			5		µV/°C
INPUT BIAS CURRENT			3.5	**8**		3.5	**5**		3.5	**8**	µA
	T_{MIN}–T_{MAX}			10			**6**			12	µA
INPUT OFFSET CURRENT			0.1	**0.4**		0.1	**0.2**		0.1	**0.4**	µA
	T_{MIN}–T_{MAX}			0.5			**0.3**			0.6	µA
INPUT CHARACTERISTICS	Differential Mode										
Input Resistance			30			30			30		kΩ
Input Capacitance			2			2			2		pF
INPUT VOLTAGE RANGE											
Common Mode		**±10**	12		**±10**	12		±10	12		V
Common-Mode Rejection	V_{CM} = ±10 V	**90**	110		**106**	115		**90**	110		dB
	T_{MIN}–T_{MAX}	85			**90**			85			dB
INPUT VOLTAGE NOISE	f = 1 kHz		4			4			4		nV/$\sqrt{Hz}$
Wideband Noise	10 Hz to 10 MHz		10			10			10		µV rms
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD} = 1 kΩ	**100**	130		**100**	130		**100**	130		V/mV
	T_{MIN}–T_{MAX}	50	80		**75**	100		**50**	80		V/mV
	R_{LOAD} = 500 Ω	75			**100**			75			V/mV
	T_{MIN}–T_{MAX}	50			**75**			50			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} ≥ 500 Ω										
	T_{MIN}–T_{MAX}	**±10**			**±10**			**±10**			V
Current	V_{OUT} = ±10 V	**50**			**50**			**50**			mA
Output Resistance	Open Loop		15			15			15		Ω
FREQUENCY RESPONSE											
Gain Bandwidth Product	V_{OUT} = 90 mV p-p										
	A_V = –10		400			400			400		MHz
Full Power Bandwidth[2]	V_O = 20 V p-p										
	R_{LOAD} = 500 Ω	5.5	6.4		5.5	6.4		5.5	6.4		MHz
Rise Time	A_V = –10		10			10			10		ns
Overshoot[3]	A_V = –10		20			20			20		%
Slew Rate[3]	A_V = –10	350	400		350	400		350	400		V/µs
Settling Time[3] – 10 V Step	A_V = –10										
	to 0.1%		80			80			80		ns
	to 0.01%		100			100			100		ns
OVERDRIVE RECOVERY	–Overdrive		190			190			190		ns
	+Overdrive		350			350			350		ns
DIFFERENTIAL GAIN	f = 4.4 MHz		0.025			0.025			0.025		%
DIFFERENTIAL PHASE	f = 4.4 MHz		0.04			0.04			0.04		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±5**		**±18**	**±5**		**±18**	**±5**		**±18**	V
Quiescent Current			12	**14**		12	**14**		12	**14**	mA
	T_{MIN}–T_{MAX}			16			**16**			**18**	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±18 V	**90**	100		**94**	100		**90**	100		dB
	T_{MIN}–T_{MAX}	80			**86**			**80**			dB
TEMPERATURE RANGE											
Rated Performance[4]		**0**		**+75**	0		**+75**	–55		**+125**	°C
TRANSISTOR COUNT	# of Transistors		72			72			72		

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.
[2]Full power bandwidth = slew rate/2 π V_{PEAK}.
[3]Refer to Figures 22 and 23.
[4]"S" grade T_{MIN}–T_{MAX} specifications are tested with automatic test equipment at T_A = –55°C and T_A = +125°C.
All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipation[2]
  Plastic (N) . . . . 1.5 W
  Cerdip (Q) . . . . 1.3 W
  LCC (E) . . . . 1.0 W
Input Voltage . . . . $\pm V_S$
Differential Input Voltage . . . . ±6 V
Storage Temperature Range
  Q, E . . . . –65°C to +150°C
  N . . . . –65°C to +125°C
Junction Temperature (T_J) . . . . +175°C
Lead Temperature Range (Soldering 60 sec) . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C.
Thermal Characteristics:

	θ_{JC}	θ_{JA}	Derate at
Cerdip Package	30°C/W	110°C/W	8.7 mW/°C
Plastic Package	30°C/W	100°C/T	10 mW/°C
LCC Package	35°C/W	150°C/W	6.7 mW/°C

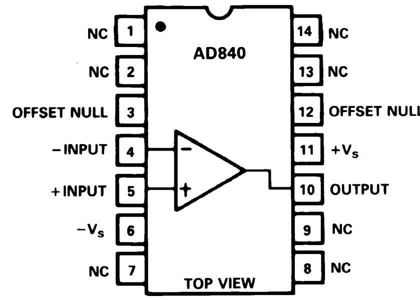
Recommended Heat Sink:
  Aavid Engineering© #602B

ORDERING GUIDE

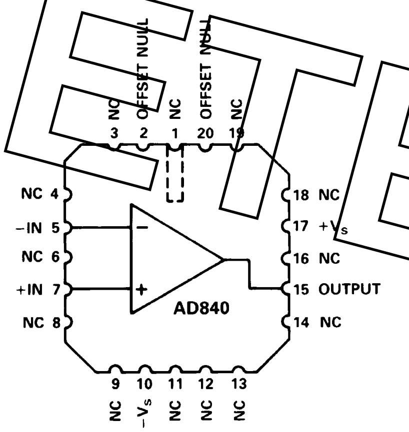
Models	Package Options[2]
AD840JN	N-14
AD840KN	N-14
AD840JQ	Q-14
AD840KQ	Q-14
AD840SQ	Q-14
AD840SQ-883B	Q-14
5962-89640012A	Q-14
AD840SE-883B	E-20A
5962-8964001CA	E-20A

NOTES
[1]J and S Grade Chips also available.
[2]N = Plastic DIP; Q = Cerdip; E = LCC (Leadless Ceramic Chip Carrier).

Plastic DIP (N) Package and Cerdip (Q) Package



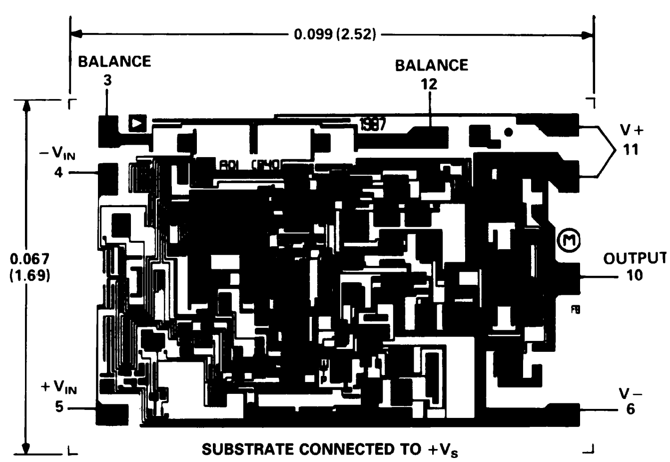
LCC (E) Package



AD840 Connection Diagrams

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD840–Typical Characteristics (at +25°C and V_S = ±15 V, unless otherwise noted)

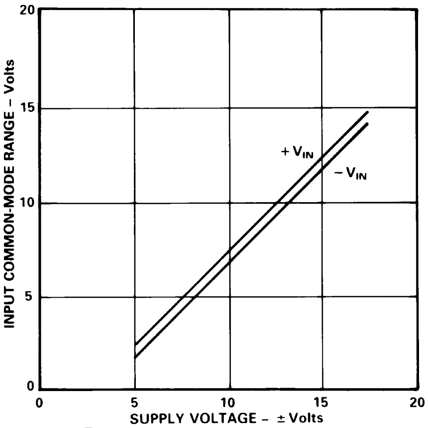


Figure 1. Input Common-Mode Range vs. Supply Voltage

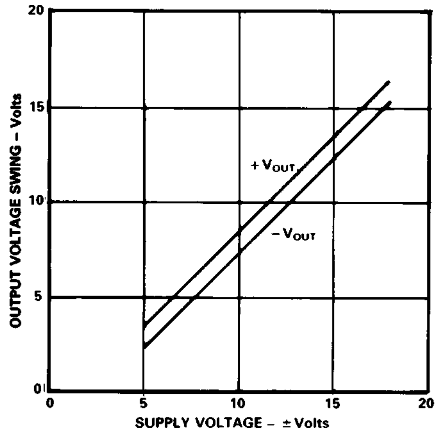


Figure 2. Output Voltage Swing vs. Supply Voltage

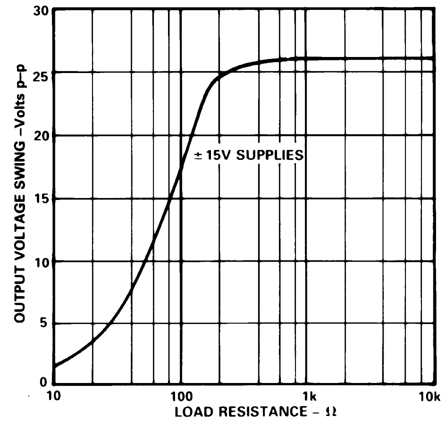


Figure 3. Output Voltage Swing vs. Load Resistance

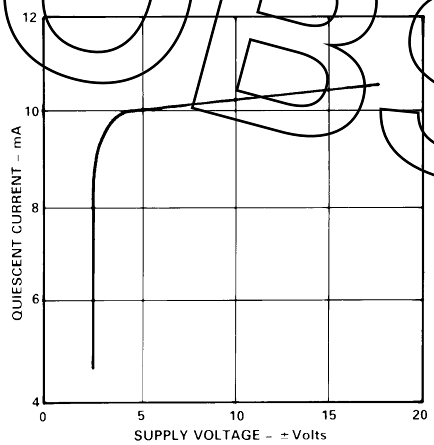


Figure 4. Quiescent Current vs. Supply Voltage

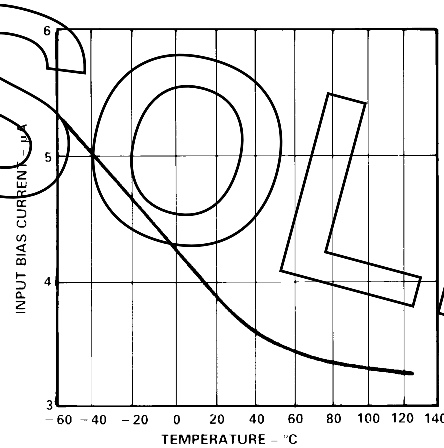


Figure 5. Input Bias Current vs. Temperature

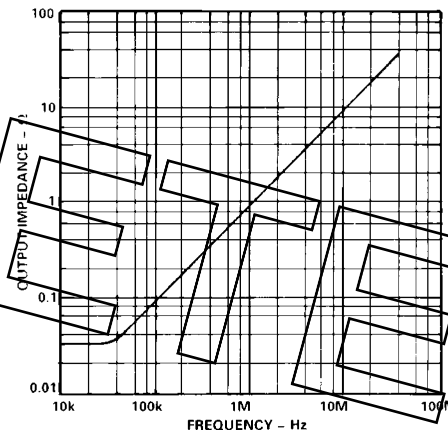


Figure 6. Output Impedance vs. Frequency

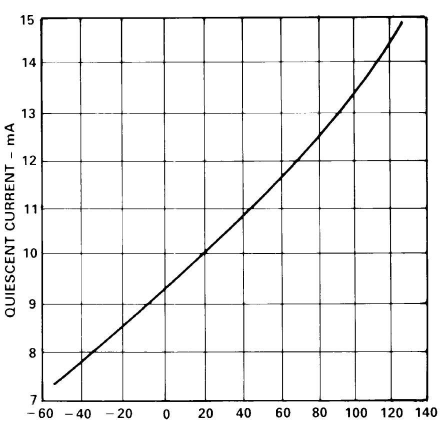


Figure 7. Quiescent Current vs. Temperature

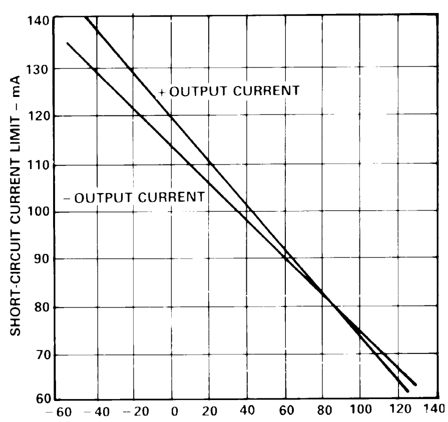


Figure 8. Short-Circuit Current Limit vs. Temperature

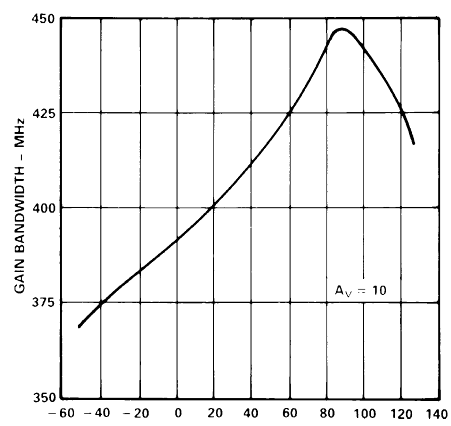


Figure 9. Gain Bandwidth Product vs. Temperature

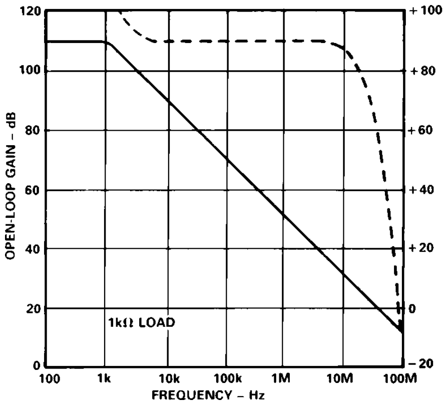


Figure 10. Open-Loop Gain and Phase Margin Phase vs. Frequency

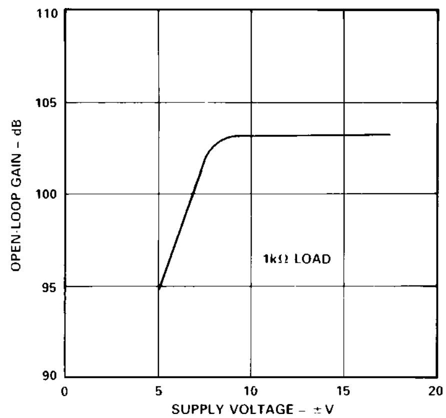


Figure 11. Open-Loop Gain vs. Supply Voltage

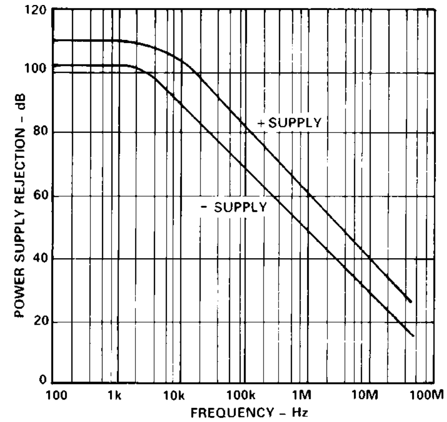


Figure 12. Power Supply Rejection vs. Frequency

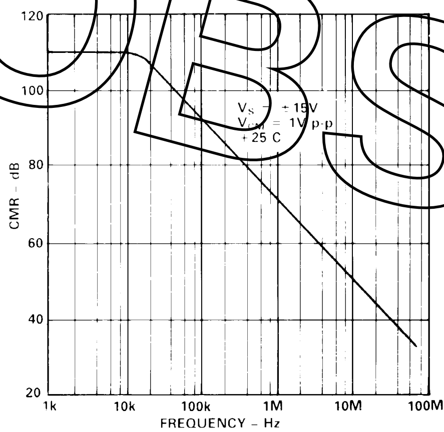


Figure 13. Common-Mode Rejection vs. Frequency

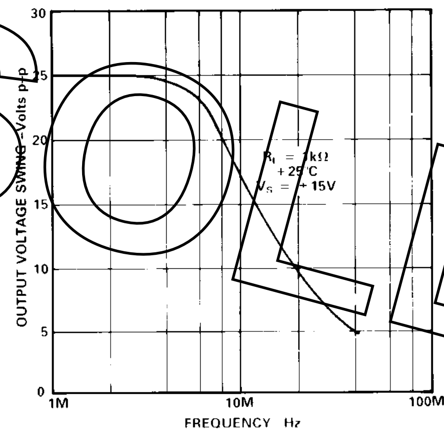


Figure 14. Large Signal Frequency Response

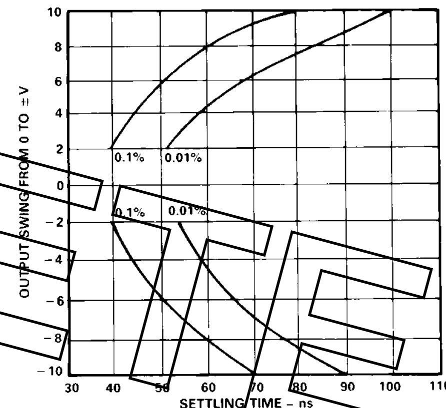


Figure 15. Output Swing and Error vs. Settling Time

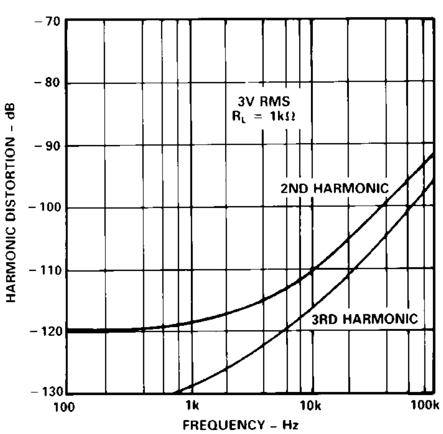


Figure 16. Harmonic Distortion vs. Frequency

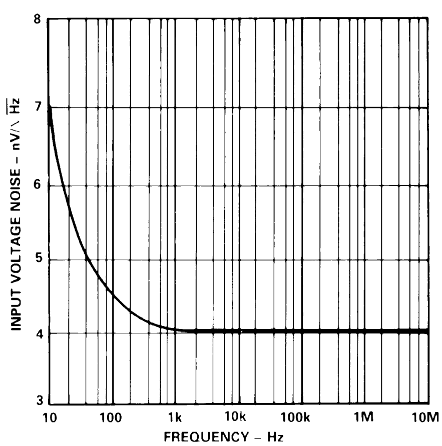


Figure 17. Input Voltage Noise Spectral Density

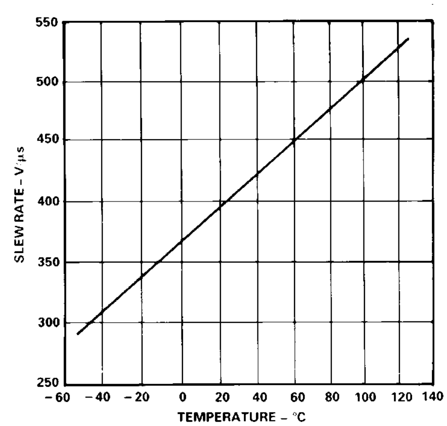


Figure 18. Slew Rate vs. Temperature

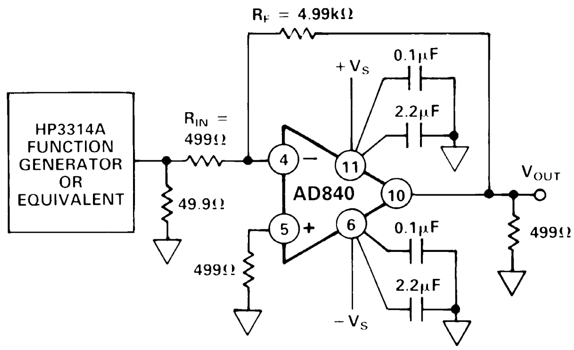


Figure 19a. Inverting Amplifier Configuration (DIP Pinout)

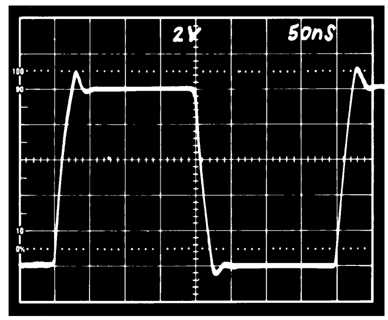


Figure 19b. Inverter Large Signal Pulse Response

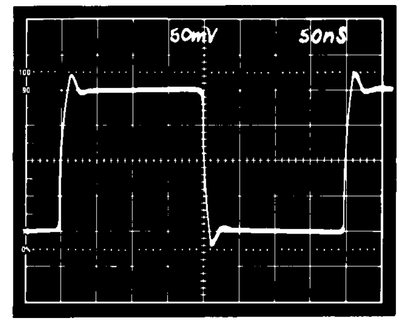


Figure 19c. Inverter Small Signal Pulse Response

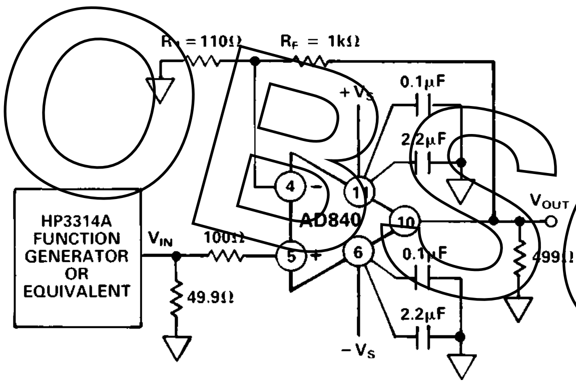


Figure 20a. Noninverting Amplifier Configuration (DIP Pinout)

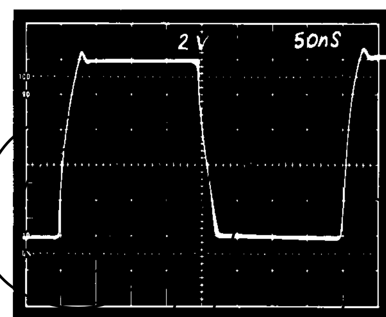


Figure 20b. Noninverting Large Signal Pulse Response

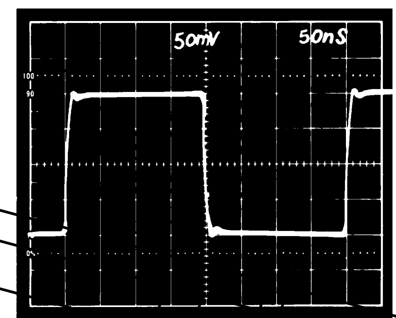


Figure 20c. Noninverting Small Signal Pulse Response

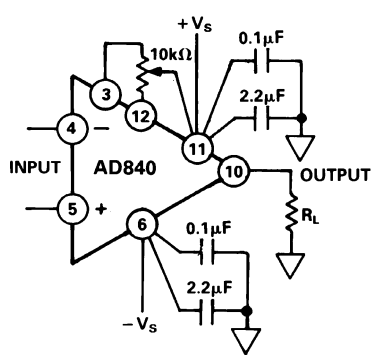


Figure 21. Offset Nulling (DIP Pinout)

OFFSET NULLING

The input offset voltage of the AD840 is very low for a high speed op amp, but if additional nulling is required, the circuit shown in Figure 21 can be used.

AD840 SETTLING TIME

Figures 22 and 24 show the settling performance of the AD840 in the test circuit shown in Figure 23.

Settling time is defined as:

> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

This definition encompasses the major components which comprise settling time. They include (1) propagation delay through the amplifier; (2) slewing time to approach the final output value; (3) the time of recovery from the overload associated with slewing; and (4) linear settling to within the specified error band.

Expressed in these terms, the measurement of settling time is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for the application.

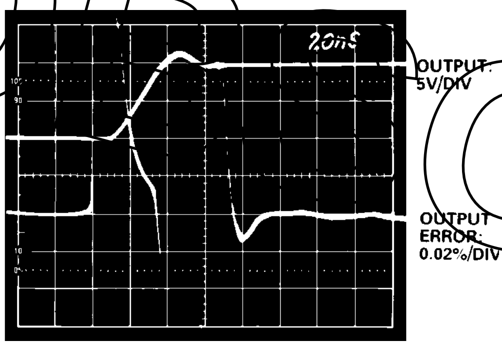


Figure 22. AD840 0.01% Settling Time

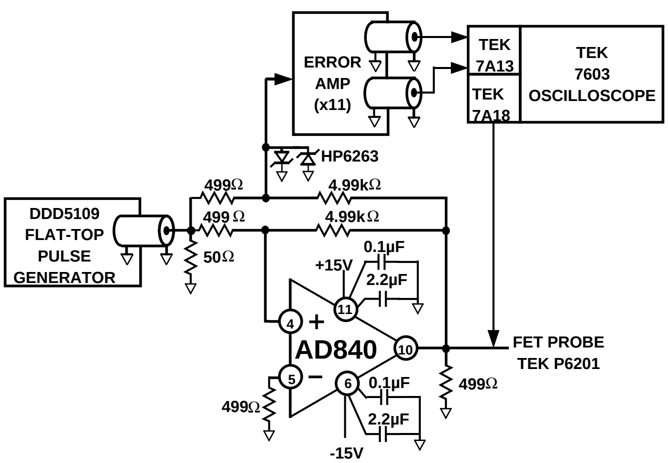


Figure 23. Settling Time Test Circuit

Figure 23 shows how measurement of the AD840's 0.01% settling in 100 ns was accomplished by amplifying the error signal from a false summing junction with a very high speed proprietary hybrid error amplifier specially designed to enable testing of small settling errors. The device under test was driving a 420 Ω load. The input to the error amp is clamped in order to avoid possible problems associated with the overdrive recovery of the oscilloscope input amplifier. The error amp amplifies the error from the false summing junction by 11, and it contains a gain vernier to fine trim the gain.

Figure 24 shows the "long-term" stability of the settling characteristics of the AD840 output after a 10 V step. There is no evidence of settling tails after the initial transient recovery time. The use of a junction isolated process, together with careful layout, avoids these problems by minimizing the effects of transistor isolation capacitance discharge and thermally induced shifts in circuit operating points. These problems do not occur even under high output current conditions.

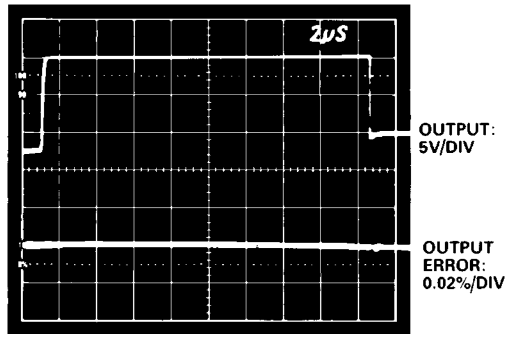


Figure 24. AD840 Settling Demonstrating No Settling Tails

GROUNDING AND BYPASSING

In designing practical circuits with the AD840, the user must remember that whenever high frequencies are involved, some special precautions are in order. Circuits must be built with short interconnect leads. Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as minimizing the effects of high frequency coupling. Sockets should be avoided, because the increased inter-lead capacitance can degrade bandwidth.

Feedback resistors should be of low enough value to assure that the time constant formed with the circuit capacitances will not limit the amplifier performance. Resistor values of less than 5 kΩ are recommended. If a larger resistor must be used, a small (±10 pF) feedback capacitor in connected parallel with the feedback resistor, R_F, may be used to compensate for these stray capacitances and optimize the dynamic performance of the amplifier in the particular application.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. A 2.2 µF capacitor in parallel with a 0.1 µF ceramic disk capacitor is recommended.

CAPACITIVE LOAD DRIVING ABILITY

Like all wideband amplifiers, the AD840 is sensitive to capacitive loading. The AD840 is designed to drive capacitive loads of up to 20 pF without degradation of its rated performance. Capacitive loads of greater than 20 pF will decrease the dynamic performance of the part although instability should not occur unless the load exceeds 100 pF. A resistor in series with the output can be used to decouple larger capacitive loads.

USING A HEAT SINK

The AD840 draws less quiescent power than most high speed amplifiers and is specified for operation without a heat sink. However, when driving low impedance loads the current to the load can be 4 to 5 times the quiescent current. This will create a noticeable temperature rise. Improved performance can be achieved by using a small heat sink such as the Aavid Engineering #602B.

HIGH SPEED DAC BUFFER CIRCUIT

The AD840's 100 ns settling time to 0.01% for a 10 V step makes it well suited as an output buffer for high speed D/A converters. Figure 25 shows the connections for producing a 0 to +10.24 V output swing from the AD568 35 ns DAC. With the AD568 in unbuffered voltage output mode, the AD840 is placed in noninverting configuration. As a result of the 1 kΩ span resistor provided internally in the AD568, the noise gain of this topology is 10. Only 5 pF is required across the feedback (span) resistor to optimize settling.

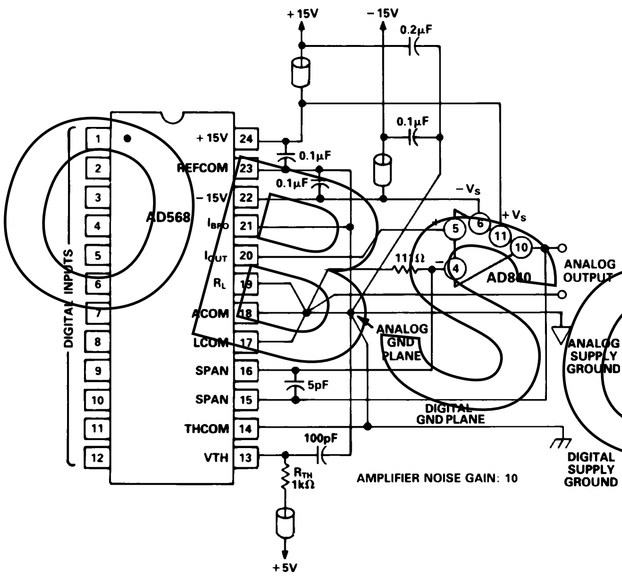


Figure 25. 0 V to +10.24 V DAC Output Buffer

OVERDRIVE RECOVERY

Figure 26 shows the overdrive recovery capability of the AD840. Typical recovery time is 190 ns from negative overdrive and 350 ns from positive overdrive.

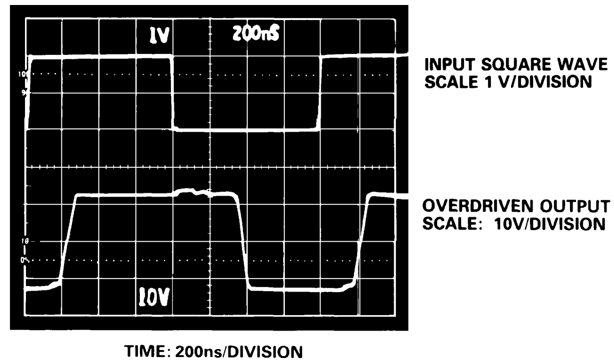


Figure 26. Overdrive Recovery

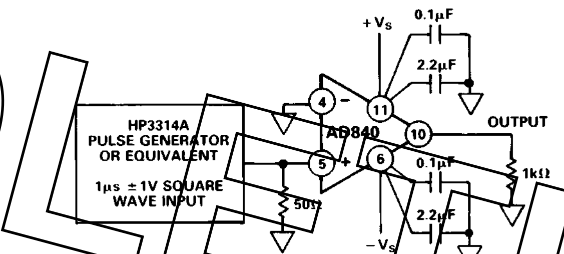
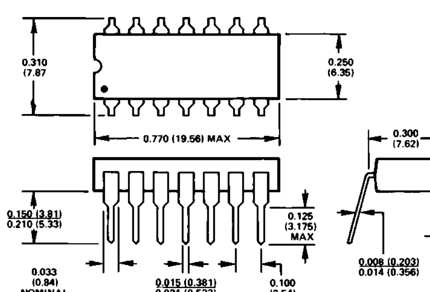


Figure 27. Overdrive Recovery Test Circuit

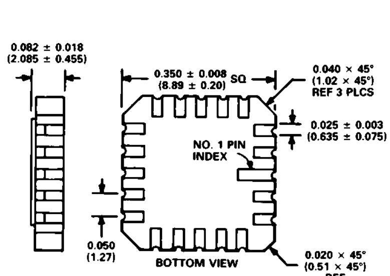
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

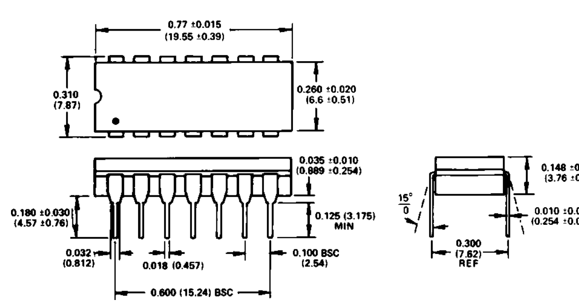
14-Pin Cerdip (Q) Package



20-Pin LCC (E) Package



14-Pin Plastic (N) Package



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