LINEAR TECHNOLOGY

OCTOBER 1992 VOLUME II NUMBER 3

IN THIS ISSUE . . .

Design Techniques for Electrostatic Discharge Protection

by Sean Gold

Since their infancy, integrated-circuit manufacturers have been concerned about circuit damage caused by electrostatic discharge (ESD). Assembly and packaging procedures often proved fatal to early stone-knife and bearskin ICs. Design and processing techniques improved, but device geometries shrank, perpetuating ESD problems. Today, interest in ESD protection goes beyond handling and assembly considerations.

Portable computers and instrumentation are often subjected to severe electrical stresses, imposing stringent demands on exposed circuitry. Digital-communication interfaces and input amplifiers must tolerate repetitive ESD pulses because cable connections frequently come in contact with humans and other charged bodies. In addition, products to be sold in European markets must conform to standards set forth by the European Committee for Electrotechnical Standardization (CENELEC). The standard for ESD, IEC-801-2, is now under review and will become mandatory in 1996.

UNDERSTANDING ESD

Even though the most modern ICs have some form of ESD protection, a basic understanding of electrostatic discharge, its causes and its remedies, is helpful when designing circuits for electrically harsh environments.

Charge Generation

Both conductors and insulators can support charge, which can build up in three ways:

1. Inductively, when a surface becomes polarized due to nearby electric fields
2. Capacitively, when the capacitance of a body at fixed potential increases
3. Triboelectrically, when two materials exchange charge as result of friction and are separated.[1]

The third generation mechanism, triboelectricity, is usually the most troublesome because the human body can acquire a substantial charge, up to 35kV in some cases, depending upon the relative humidity and electrical properties of the materials involved. Walking across a wool carpet with leather shoes on a dry winter day may generate a charge of 10kV to 15kV, whereas the same action on a humid day in the summer may produce less than 2kV.

Charge Transfer

For charge to affect circuitry, it must be transferred from the generator. Electrostatic charge may be transferred between bodies at different potentials directly, via physical contact, or inductively, via an electrostatic field.

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ESD Protection, High-Speed and Precision Op Amps, and Fast Serial ADCs Highlight this Issue

by Richard Markell

This issue, the last of the year, spotlights many different topics. ESD (electrostatic discharge) is a critical issue for most RS232 designs. Our lead article presents a careful study of the causes, cures, and prevention of electrostatic-discharge damage in RS232 circuitry. The article presents a method to virtually assure that your RS232 design is the best it can be.

LTC has expended time and resources on an intensive program to ensure that our RS232 devices are as ESD resistant as we can make them. Laboratory testing has proven that our RS232 devices can withstand multiple 10kV strikes. Line drivers and line receivers must be more resistant to ESD than other types of devices since their inputs and outputs connect directly to the outside world. Other devices are hidden inside instrumentation boxes, on PC boards, or otherwise shielded from the rigors experienced by the DB25 (RS232) connector. Making LTC's RS232 parts more rugged to the tune of 10kV is another engineering triumph from the designers at LTC.

This issue includes two articles on our high-speed operational amplifiers. The first is a collection of circuits designed around the low cost LT1190 video amplifier. The second shows temperature compensation of the LT1228 electronic gain control amplifier. Both of these components and a whole list of other video amplifiers are products from LTC's 600MHz complementary bipolar process. This proprietary process allows IC designers to combine precision DC specifications with high speed, resulting in some of the best video amplifiers in the industry. Watch for more video amplifiers and other high-speed products from LTC.

Precision operational amplifiers are also well represented in this issue with articles on the new LT1112/1114 dual and quad surface-mountable op amps. Also new in the world of op amps is a surface-mount version of the industry's lowest noise op amp, the LT1028. In addition, the new LT1128 is a unity-gain-stable version of the LT1028, which is also available in SO packages. The LT1028 and the LT1128 are featured in a short article herein. Last to be described here, but certainly not least in performance, are two new A/D converters. These converters, the LT1196/1198, challenge half-flash converters in speed, cost, power consumption, size, and ease of use.

Issue Highlights

Sean Gold leads off this issue with his article on techniques for staving off the horrors of ESD. Sean has been at LTC for four years, during which time he designed the LT1134, LT1137, LT1237, LT1330, LT1026 and the LT1116. He is an avid cyclist, urban adventurer, and alpine skier, and regularly attends the Foothill College electronics flea market. Sean's collection of mid-60's oscilloscopes and instrumentation has made him extremely popular with the ladies.

Mitchell Lee and John Wright describe a number of applications for LTC's LT1190 high-speed op amp. Mitchell Lee has been at LTC for two years as an Applications Engineer. He has worked in the semiconductor applications arena (and it certainly is an arena) for more than 12 years total. Mitchell's hobbies include fourth-season mountaineering and music. Unlike John, Mitchell doesn't fish Hat Creek.

Frank Cox is the newest member of our Applications Group. Frank describes the LT1228 100MHz current-feedback amplifier with DC gain control. He has been involved in RF and video systems for the past eight years. Frank has been at LTC for only four months but is already developing many video and RF circuits using LTC's high-speed operational amplifiers. Frank's outside interests include fishing and audio systems.

Alexander Strong and George Erdi describe some new LTC offerings in op amps, the LT1128 and the LT1028 in SO packaging. Alex has been at LTC for more than two years. He has worked in the semiconductor industry for more than 12 years, primarily designing op amps and D/A converters. Alex is a Vermont native whose interests include camping, hiking, and racing his diesel Mercedes at Laguna Seca. Alex is another loyal patron of the Foothill flea market.

Marco Pan is the designer and co-author of the article on the LTC1196/1198 serial 8-bit A/D converters that convert at speeds up to 1.3MHz. Marco has been at LTC for five years and has been in the industry a total of eight years. He designed the LTC690 series of microprocessor supervisory circuits, LTC1096, LTC1098, LTC1196 and the LTC1198. Marco's outside interests include his family, gardening, and home improvement.

Short biographies of John Wright, Willie Rempfer, and George Erdi appeared in previous issues. LT

LT1190 Family Ultra-High-Speed Op Amps Eclipse Prior Art

by John Wright and
Mitchell Lee

Introduction

The LT1190 series op amps combine bandwidth, slew rate, and output-drive capability to satisfy the demands of many high-speed applications. This family offers up to 350MHz gain-bandwidth product, slew rates of 450V/µs, and yet drives a 150Ω (75Ω, double-terminated) load. In 50Ω systems, the LT1190 family can deliver +13.5dBm to a double-terminated load. These parts are based on the familiar, easy-to-use, voltage-mode feedback topology.

Characteristics of the three members of the LT1190 series are shown in Table 1.

Table 1. Characteristics of the LT1190 family

Part	GBWP (MHz)	SR (V/µs)	Min Gain	Settling Time (0.1%, ns)
LT1190	50	450	+1	140
LT1191	90	450	+1	110
LT1192	350	450	+5	90

All of the LT1190 series devices operate on single 5 to 15V supplies, or split supplies of up to ±8V. Output current capability is ±50mA.

Careful chip design has made the LT1190 family quite tolerant of supply-rail bypassing. In many applications, a simple 100nF disc ceramic capacitor from each supply pin to ground is all that is needed. Where settling time is an issue, a 4.7µF tantalum capacitor should be added on each supply pin. Such a cavalier attitude toward supply bypassing is a radical departure from the industry norm.

Another unusual feature common to the LT1190 family is shutdown. This allows the user to multiplex outputs, gate signals, or conserve power when an op amp is idle.

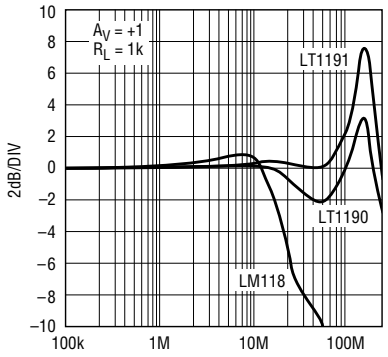

Figure 1. Small-signal response A_V = +1. 130MHz peaking due to socket and bypass components

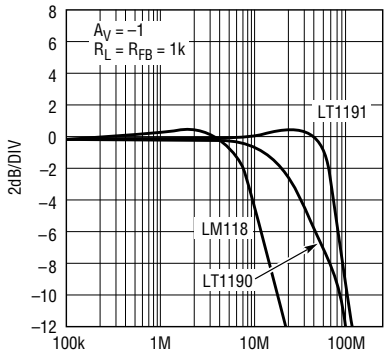

Figure 2. Small-signal response A_V = –1

Small-Signal Performance

Figures 1 and 2 show the small-signal performance of the LT1190 and LT1191 when configured for gains of +1 and –1. The non-inverting plots show peaking at 130MHz, which is characteristic of the socketed test fixture and supply bypass components. A tight PC-board layout would reduce the LT1190 peaking to 2dB. The small-signal performance of an LM118 is shown for comparison.

Applications

Fast peak detectors place unusual demands on amplifiers. The output stage must have a high slew rate in order to keep up with the intermediate stages of the amplifier. This condition causes either a long overload or DC-accuracy errors. To maintain a high slew rate at the output, the amplifier must deliver large currents into the capacitive load of the detector. Other problems include amplifier instability with large capacitive loads and preservation of output-voltage accuracy.

Detecting Sine Waves

The LT1190 is the ideal candidate for this application, with a 450V/µs slew rate, 50mA output current, and 70° phase margin. The closed-loop peak detector circuit of Figure 3 uses a Schottky diode inside the feedback loop to obtain good accuracy. A 20Ω resistor (R_O) isolates the 10nF load and prevents oscillation.

DC error with a sine-wave input is plotted in Figure 4 for various input amplitudes. The DC value is read with a DVM. At low frequencies, the error is small and is dominated by the decay of the detector capacitor between cycles.

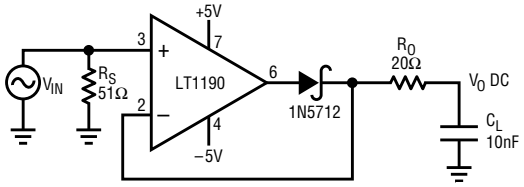

Figure 3. Closed-loop peak detector

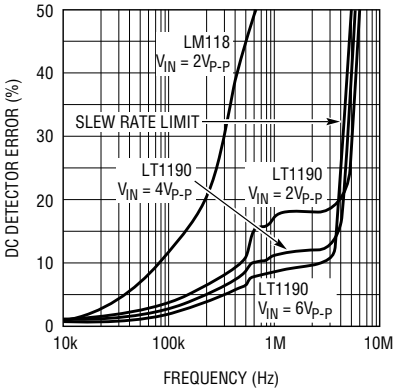

Figure 4. Closed-loop peak-detector error vs frequency

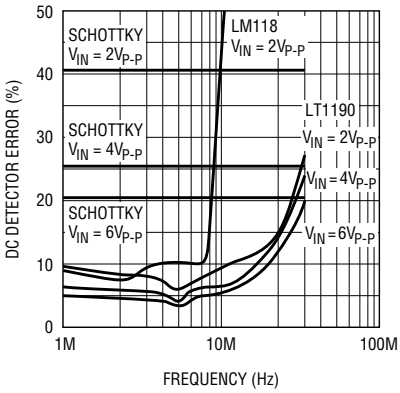

Figure 6. Open-loop peak-detector error vs. frequency

As frequency rises, the error increases because capacitor charging time decreases. During this time the overdrive becomes a very small portion of a sine wave cycle. Finally, at approximately 4MHz, the error rises rapidly owing to the slew-rate limitation of the op amp. For comparison purposes, the error of an LM118 is also plotted for $V_{IN} = 2V_{P-P}$.

A Schottky-diode peak detector can be built with a 1nF capacitor and a 10kΩ pulldown. Although this simple circuit is very fast, it has limited usefulness owing to the error of the diode threshold and its low input impedance. The accuracy of this simple detector can be improved with the LT1190 circuit of Figure 5.

In this open-loop design, D1 is the detector diode and D2 is a level-shifting or compensating diode. A load resistor, R_L, is connected to –5V, and an identical bias resistor, R_B, is used to bias the compensating diode. Equal-value resistors ensure that the diode drops are equal. Low values of R_L and R_B (1kΩ to 10kΩ) provide fast response, but at the expense of poor low-frequency accuracy. High values of R_L and R_B provide good low-frequency accuracy but cause the amplifier to slew-rate limit, resulting in poor high-frequency accuracy. A good compromise can be made by adding a feedback capacitor, C_{FB}, which enhances the negative slew rate on the (–) input.

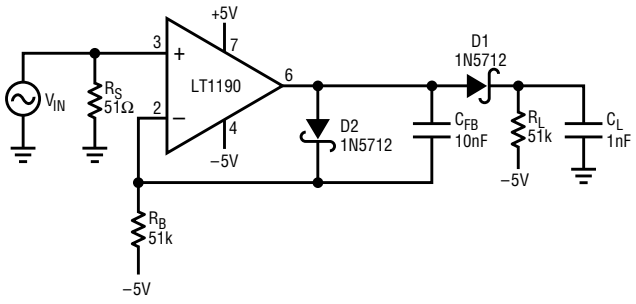

Figure 5. Open-loop, high-speed peak detector

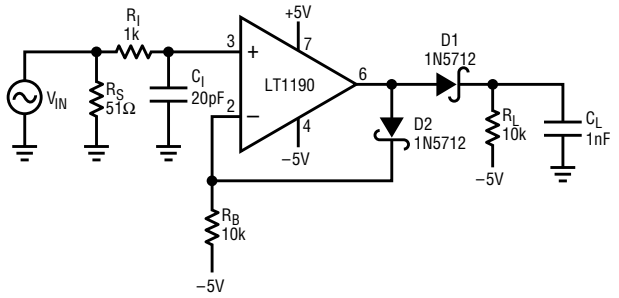

Figure 7. Fast pulse detector

The DC error with a sine-wave input, as read with a DVM, is plotted in Figure 6. For comparison purposes the LM118 error is plotted, as well as the error of the simple Schottky detector.

Pulse Detector

A fast pulse detector can be made with the circuit of Figure 7. A very fast input pulse will exceed the amplifier's slew rate and cause a long overload recovery time. Some amount of dV/dt limiting on the input can help this overload condition; however, it will delay the response.

Figure 8 shows the detector error versus pulse width. Figure 9 is the response to a $4V_{P-P}$ input pulse that is 80ns wide. The maximum output slew rate in the photo is 70V/µs. This rate is set by the 70mA current limit driving 1nF. As a performance benchmark, the LM118 takes 1.2µs to peak detect and settle, given the same amplitude input. This slower response is due, in part, to the much lower slew rate and lower phase margin of the LM118.

Instrumentation Amplifier Rejects High Voltage

Instrumentation amplifiers are normally used to process slowly varying outputs from transducers, rather than

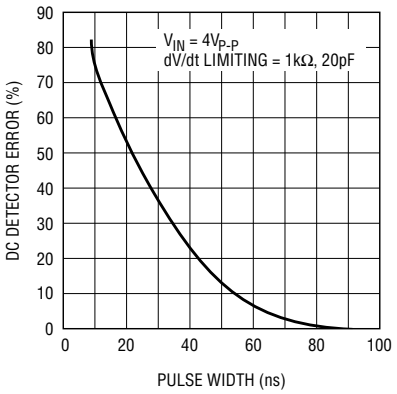

Figure 8. Detector error vs. pulse width

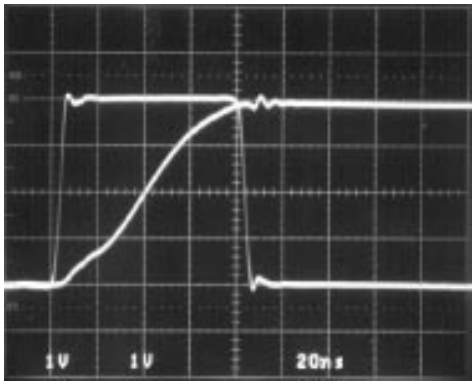

Figure 9. Open-loop peak detector response
Trace A: output (1 Volt/division)
Trace B: input (1 Volt/division)

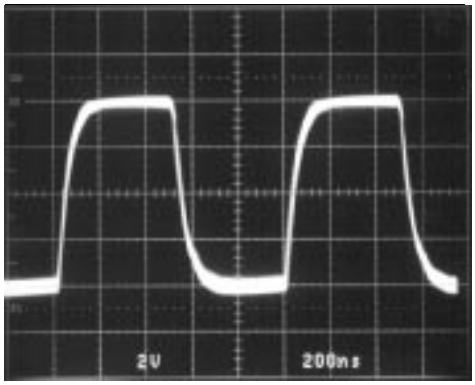

Figure 11. Output of instrumentation amplifier with a 1MHz square wave riding on $120V_{P-P}$ at the input

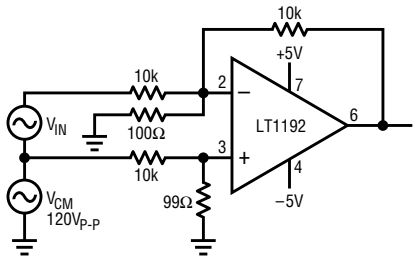

Figure 10. 3.5MHz instrumentation amplifier rejects $120V_{P-P}$

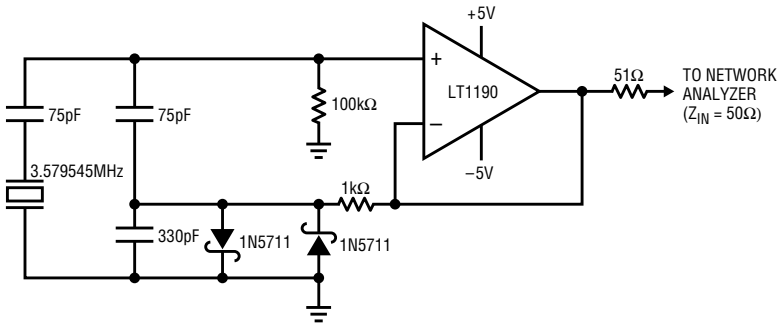

Figure 12. High-frequency Colpitts oscillator

fast signals. However, it is possible to make an instrumentation amplifier that responds very quickly, with good common mode rejection. For the circuit of Figure 10, an LT1192 is used to obtain 50dB of CMRR from a $120V_{P-P}$ signal. In this application, the CMRR is limited by the matching of the resistors, which should match to better than 0.01%.

An LT1192 is used in this application because the circuit has a noise gain of 100, and because the higher gain bandwidth of the LT1192 allows a –3dB bandwidth of 3.5MHz. Note also that the 100:1 attenuation of the common-mode signal presents a common-mode voltage to the amplifier of only $1.2V_{P-P}$. Figure 11 shows the amplifier output for a 1MHz square wave riding on a $120V_{P-P}$, 60Hz signal. The circuit exhibits 50dB rejection of the common-mode signal.

Crystal Oscillator

Op amps have found wide use in low-frequency (≤100kHz) crystal oscillator circuits, but just haven't had the bandwidth to operate successfully at higher frequencies. The LT1190 and LT1191 make excellent gain stages for high-frequency Colpitts oscillators. A practical implementation is shown in Figure 12.

Gain limiting is provided by two Schottky diodes, which maintain the output at approximately +11dBm—sufficient to directly drive +7 or +10dBm diode-ring mixers. Output-stage clipping is not recommended as a means of gain limiting, as this increases distortion and allows internal nodes to be overdriven. The recovery time would add excessive phase shift in the oscillator loop, degrading frequency stability.

Distortion performance is good, considering that the oscillator consists of one stage and can deliver useful output power. Figure 13 shows a spectral plot of the oscillator's output. The second harmonic is approximately 37dB down, limited primarily by the clipping action of the Schottky diodes. Power-supply rejection is excellent, showing a frequency sensitivity of approximately 0.1ppm/V. The LT1190 gives acceptable performance to 10MHz, while the LT1191 extends the circuit's operating range to 20MHz.

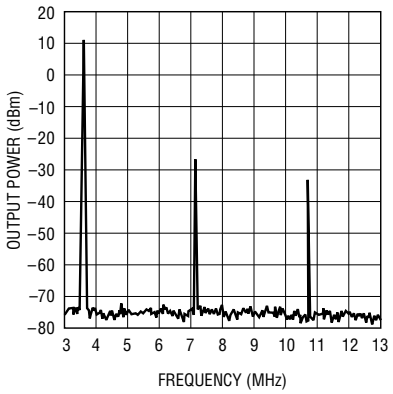

Figure 13. Oscillator output spectrum

LTC1196/1198 SO-8 Packaged SAR ADCs Beat Half-Flashes in Any Arena and Run on 3 or 5V Supplies

by William Rempfer and Marco Pan

INTRODUCTION

The LTC1196/1198 are 600ns, 1.2MHz sampling 8-bit A/D converters packaged in tiny 8-pin SO packages and operating on 3V to 6V supplies. The on-chip sample-and-holds have full-accuracy input bandwidths of 1MHz. The ADCs draw only 10mW from a 3V supply or 50mW from a 5V supply and the LTC1198 powers down to leakage current between conversions.

The LTC1196 has differential inputs and offers the highest sample rate (1.2MHz). The LTC1198 converts two input channels, single ended or differentially. These converters provide system designers with previously impossible levels of performance in an extremely small space. This article will discuss the ADCs' advantages, design techniques, 3V and 5V performance, and application considerations.

SIZE, SPEED, COST, AND POWER ADVANTAGES

The new LTC1196/1198 offer smaller size, better speed, lower cost, and much lower power dissipation than half-flash converters.

Size

The LTC1196/1198 can provide considerable space savings over half-flash ADCs for three reasons: First, the tiny SO-8 package and minimum number of external components makes the ADCs' configuration small compared to those of the 20-pin alternatives. Second, the low power dissipation and high-impedance inputs cut the space requirements in the power supply and signal-conditioning circuitry. Third, the serial interface to a processor, digital ASIC, or logic system requires only three wires and only three pins on the receiving system. This saves board space and allows the ADC to be located close to the signal source, making the physical configuration more flexible and smaller than the 11-wire-I/O half-flash alternatives. With the LTC1196/1198, an extremely small configuration can be implemented, as shown in Figure 1. The system is 3V powered and is 100% surface mountable.

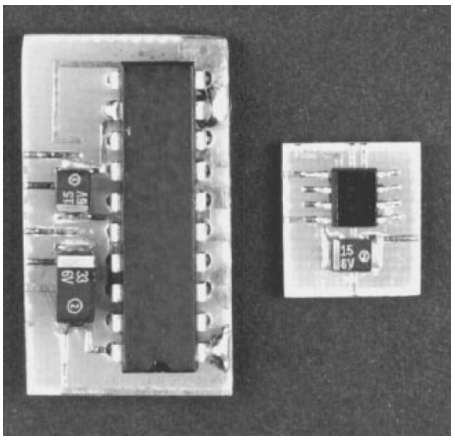

Figure 1. The LTC1196/1198 (right) can provide considerable space savings over half-flash ADCs (left)

Speed

The LTC1196 and LTC1198 beat half-flash ADCs on speed. They offer equivalent sample rates and three times wider input-sampling bandwidths than well known half-flash products such as the AD7821, ADC08061, or ML2261. With 600ns conversion times, 1.2MHz sampling rates, and 1MHz full-accuracy input bandwidths, the LTC1196/1198 are more than a match for half-flash ADCs.

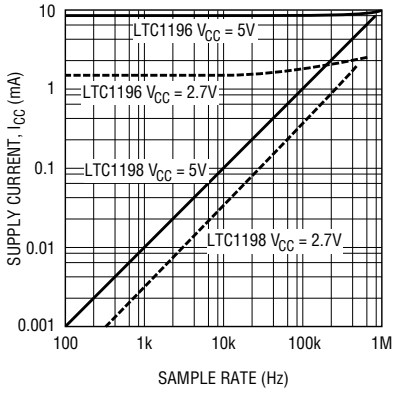

Figure 2. I_{CC} vs. sample rate for LTC1196 and LTC1198 operating on 5V and 2.7V supplies

Cost

The LTC1196/1198 reduce system cost relative to half-flash ADCs in a number of ways. First, they offer tremendous price/performance advantages when their sticker prices are compared to those of half-flash converters in this speed range. Second, the savings in board space can translate into a cheaper system or a system that wasn't even possible with older technology. Third, 3V operation can eliminate the cost of a regulated supply in 3V battery systems or the cost of generating a separate 5V supply in 3V systems. Fourth, reduced-span operation can reduce the cost of signal-conditioning circuitry. Finally, the reduced power consumption and power shutdown can reduce the cost of the system power supply or batteries.

Power

The power savings of the new ADCs, and especially of the LTC1198, can be very large. Their power consumption when operating on a 5V rail is equal to that of a half-flash converter. Power consumption can be reduced two ways. Using a 3V supply lowers the power consumption on both devices by a factor of five, to 10mW. The LTC1198 can reduce power even more because it shuts down whenever it is not converting. Figure 2 shows the supply current versus sample rate for the LTC1196 and the LTC1198 on 3V and 5V.

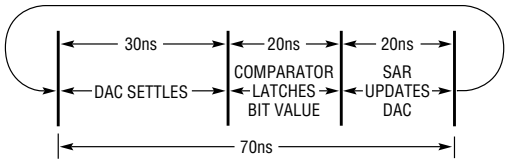

Figure 3. Bit-test timing sequence

INTERNAL DESIGN: GETTING HALF-FLASH SPEEDS WITH AN SAR CONVERTER

The LTC1196/1198 design uses the successive-approximation technique to achieve remarkable speed from a low-cost n-well CMOS process. To achieve its 600ns conversion time and 1.2MHz sample rate, bit tests are performed every 70ns. To digitize 1MHz input signals to full accuracy, the sample-and-hold has a 3dB bandwidth of 10MHz and acquires and settles in less than 100ns.

The partitioning of the 70ns bit-test time is shown in Figure 3. One cycle consists of the DAC switching and settling, the comparator making a decision, and the SAR latching the bit value and updating the DAC.

The capacitive DAC design settles to 0.02% in 30ns. The design and layout of the DAC is critical to achieving this speed. The settling time constant must be less than 3.5ns.

The comparator is an ultra-fast, auto-zeroed, sampled-data comparator. It is a redesign of the comparator used in the LTC1272 12-bit, 3µs sampling ADC. Its design includes cascaded stages of low gain and has an extremely wide (200MHz) small-signal bandwidth. It is designed to minimize disturbance to the power supply lines and responds to a 0.5mV overdrive in 20ns.

Figure 4 shows the conversion timing for the LTC1196. The conversion takes 8.5 clock cycles and the total cycle time is 12 clock cycles. These correspond to a conversion time of 600ns and a sample rate of 1.2MHz at the maximum 14.3MHz clock frequency. The sample-and-hold acquires the analog input from the end of a conversion to the start of the next. At that time it goes into hold mode and the conversion starts.

3V VERSUS 5V PERFORMANCE COMPARISON

The performance comparison in Table 1 shows that using a 3V supply gives great savings in power with only modest reductions in speed. The power dissipation drops by a factor of five when the supply is reduced to 3V. The converter slows down somewhat but still gives excellent performance on a 3V rail. It converts in 1.6µs, samples at 450kHz, and provides a 500kHz linear-input bandwidth, making it the fastest 3V ADC on the market. Getting rid of 80% of the power loss makes 3V operation very attractive.

Dynamic accuracy is excellent on both 5V and 3V. The ADCs typically provide 49.3dB or 7.9ENOBs (Effective Number Of Bits) of dynamic accuracy at both 3 and 5V. The noise floor is extremely low, corresponding to a transition noise of less than 0.1LSB. DC accuracy includes ±0.5LSB total unadjusted error at 5V. At 3V, linearity error is ±0.5LSB while total unadjusted error increases to ±1LSB.

APPLICATION CONSIDERATIONS

Analog Considerations

The LTC1196/1198 are remarkably easy to use. They will yield excellent performance if some simple rules are followed for board layout, bypassing, and driving the reference and analog inputs. (For a more detailed discussion see *Linear Technology* Volume I, Number 2, pp. 9–10 and the LTC1196/1198 data sheet.)

Board layout should include an analog ground plane to which all analog circuitry is referenced. Low-inductance ground and supply lines are recommended. Also, the input signal should be routed away from digital circuitry.

If the power supply is clean, bypassing the ADC requires only a 0.1µF capacitor, because the power-supply transients produced within the chip have been minimized. A surface-mount chip cap. or a ceramic cap. with short leads will give very good results.

continued on page 12

Table 1. 5V/3V performance comparison

LTC1196/1198	5V	3V
P_{DISS}	50mW	10mW
Max f_{SAMPLE}	1.2MHz	450kHz
Min t_{CONV}	600ns	1.6µs
INL (Max)	0.5LSB	0.5LSB
Typical ENOBs	7.9 @ 300kHz	7.9 @ 100kHz
Linear Input Bandwidth (ENOBs >7)	1MHz	500kHz

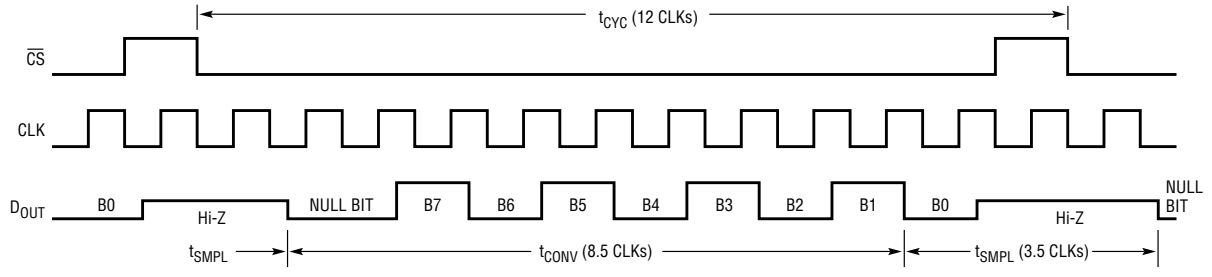

Figure 4. LTC1196 conversion timing

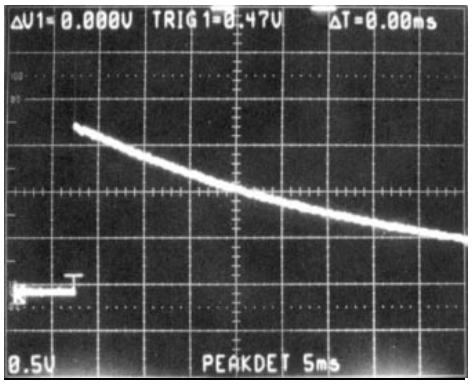

Figure 1. 3.5kV ESD pulse. (Photo taken with a low-capacitance voltage divider and a Tek type P6103 high-voltage probe)

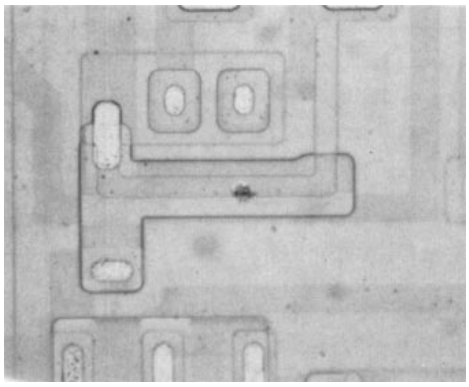

Figure 2. ESD damage results in a resistive short from a bond pad to a thin oxide n+ region on an unprotected bipolar IC

ESD, continued from page 1

The human body can store 20 to 30 millijoules of energy, but, because of the body's relatively high source impedance, not all of that energy can be transferred during a discharge.

ESD pulses exhibit a slowly decaying exponential response, but the rise time can be extremely fast. (Figure 1) ESD often contains frequency components well into the GHz range. At such frequencies, nearby cables and circuit-board traces look like receiving antennas that can pick up ESD noise.

ESD Damage

Early ICs were especially susceptible to ESD-induced oxide damage at low voltages. Discharges of less than 500V, which were commonly generated during assembly and handling, were sufficient to cause damage. Damage often occurred where the oxide's dielectric strength was weakest. The trouble spots were usually in regions where metal from a pad passed over thin oxide—often an n+ diffusion. Recognition of this problem and improved processing techniques have eliminated this type of damage.

Damage from ESD is fundamentally the result of a transfer of energy. Heat can destroy junctions and metallization when excessive energy dissipates within the chip. Intense electrostatic fields can also break down junctions or thin oxide preceding a destructive energy transfer. Figures 2 and 3 show some typical examples of ESD damage.

ESD noise can also drive circuitry into invalid or locked-up states that are not necessarily destructive. By definition, such "soft errors" are corrected by cycling the power supply or by forcing the circuit back into a valid operating state. If a soft error induces a high-current condition, prolonged heating may destroy an unprotected device. Systems can be made resilient to soft errors using digital control to detect invalid states and reset the circuit.

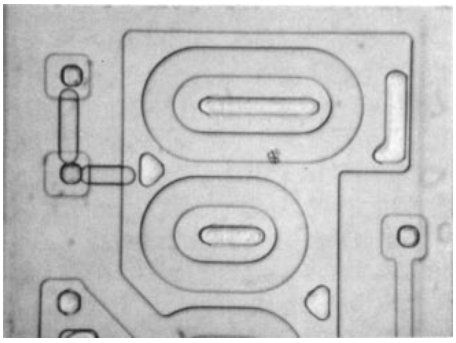

Figure 3. Removing metallization reveals junction damage between the emitter and the collector of a lateral PNP transistor

Circuit Models for ESD

The need to generate ESD pulses for test purposes prompted the development of a circuit model based on the charge storage characteristics of the human body. The switching circuit shown in Figure 4 consists of a 100pF high-voltage capacitor discharged through a 1.5kΩ resistor. The energy delivered to the load in each pulse is $E = (1/2)CV^2 \times (R_L/R_S + R_L)$. Test equipment based on this circuit model was used to determine the ESD tolerances quoted here.

ESD PROTECTION TECHNIQUES

Any action that eliminates the charge generator, circumvents charge transfer, or enhances the circuit's ability to absorb energy will increase a circuit's tolerance of ESD. Eliminating the ubiquitous charge generators or disrupting charge transfer are difficult tasks because they demand strict control of the circuit's operating environment. A more practical approach is to limit ESD entry points by shielding the circuit's enclosure and covering the exposed connectors when they are not in use.

Another practical remedy is to increase a circuit's ability to absorb energy by clamping the exposed pins

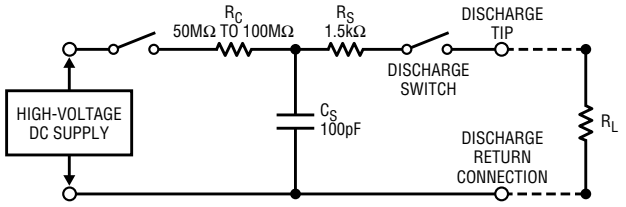

Figure 4. Human-body model circuit for ESD pulses

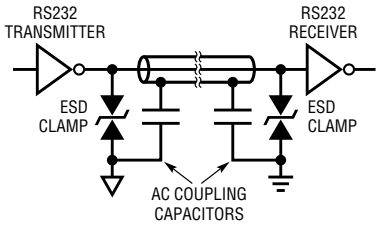

Figure 5. Older interface designs used external ESD clamps

to ground with fast-acting avalanche diodes or dedicated transient suppressors (Figure 5). Discrete suppressors are widely available and are extremely effective. Designers are often reluctant to use discrete suppressors because they are expensive—at up to $0.40/pin they can sometimes exceed the cost of the IC. Transient suppressors also introduce stray capacitance, which may prohibit their use in high-speed circuits.

Designers are often reluctant to use discrete suppressors because they are expensive... they can sometimes exceed the cost of the IC.

The LT1237 RS232 transceiver incorporates the clamps for diverting ESD energy on chip. These active structures quickly respond to positive or negative signals at threshold voltages higher than RS232 signals but below destructive levels for the device. The path of high current flow is through large pn junctions, which increase the device's capacity to absorb energy. The LT1237's ESD structures can absorb human-body-model discharges of >10kV. The resulting current flow is insignificant when the transceiver is turned off or powered down. When the transceiver is on and significant ESD discharge occurs, the resulting current may de-bias internal circuitry and cause nondestructive soft errors. Observations have shown these errors to be highly dependent upon the logical state of the transceiver.

Filters

When extremely high levels of ESD protection are required, an external LC filter can be used for additional protection. The circuit in Figure 6 has a 10MHz cutoff frequency with 40dB/decade rolloff, which is sufficient to drop ESD energy into a range that can be safely dissipated within the transceiver.

PC Board Layout

Energy shunted through an ESD clamp can still cause problems if the ground path's return inductance is large enough to create a sizable voltage drop. Such voltage drops may damage unprotected components that share the common ground line. Consider the circuit model shown in Figure 7. Suppose the return path to ground presents a 1Ω impedance at ESD frequencies. The voltage V_X at the local ground is approximately $V_X = V_P (R_G/R_G+R_S) = V_P/1500$. If there is poor common-mode coupling to V_{CC}, the digital ICs sharing the common ground will be damaged when V_X exceeds V_{CC}+0.7V. This condition occurs when the peak ESD voltage is greater than 8.55kV. Using a low-inductance ground plane, or, preferably, isolating the return path to low impedance ground, is therefore essential for good ESD protection.

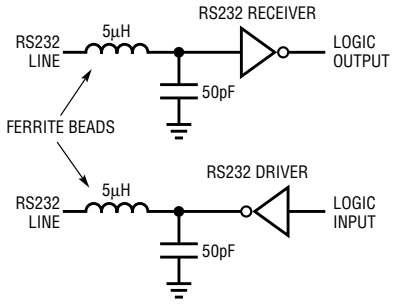

Figure 6. External LC filters provide protection from very high levels of ESD, yet cost less than discrete suppressors

Sometimes the high current path is not directly to ground. In the example with the LT1237, ESD currents flow through the device's substrate, which is connected to the negative charge pump output, V^-. V^- is AC coupled to ground through a 0.1µF storage capacitor, which must have low effective series resistance (ESR) to prevent damaging voltage drops. Adding a few hundred picofarads of low ESR capacitance in parallel with the primary storage capacitor effectively reduces ESR at ESD frequencies.

When using discrete transient suppressors or filters, place components as close as possible to the connector with short paths to the return plane. Increasing the distance, or the series resistance, between the entry point and the sensitive device diminishes the ESD energy transferred.

ESD pulses can easily arc from one trace to another when the spacing between traces is narrow. Increasing the spacing between the circuit board traces or surrounding signal lines with a separate return plane is helpful in preventing ESD energy from arcing between pins. Arcing occurs slowly compared with ESD rise time, so air spark gaps

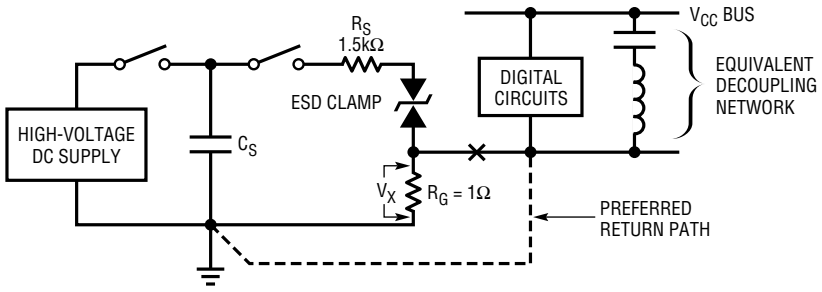

Figure 7. Circuit model for ESD current flow

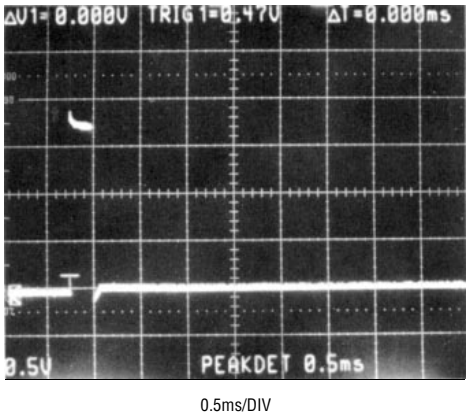

Figure 8. 10-mil spark gap limits ESD duration

alone will not protect circuitry from ESD. Spark gaps are, in fact, useful for limiting the ESD energy. Figure 8 shows a 300µs delay between the initial ESD rise and the activation of a 10 mil spark gap.

The connections to the cable shield affect noise and ESD performance. Designers may feel inclined to float the cable shield with respect to local ground to avoid circulating currents due to differences in ground potential. Do not do this! Instead, AC couple the grounds so they are shorted at ESD frequencies.

DC Isolation

ESD transients should not be confused with DC and low-frequency ground faults that occur when circuits with large differences in ground poten tial are connected together. The amount of energy transferred during a ground fault can be vastly greater than the energy of an ESD pulse. To guard against ground faults requires a circuit with true DC isolation. A fully isolated RS232 transceiver design is described in Linear Technology's Design Note 27.

CONCLUSION

The techniques described here cannot entirely eliminate ESD problems, but understanding ESD's nature and using careful circuit design will help protect against its intrusion.

[1]Triboelectric charging should not be confused with the primal creatures who worship the Tektronix 547 oscilloscope, and are often referred to as a "tribe-o-electricals."

References:

1. Linear Technology 1990 Databook, pp.15–23 to 15–34.
2. Clarke, O. and Neill, D., "Electrical-Transient Immunity: A Growing Imperative For System Design," *Electronic Design*, Jan 23, 1992, pp. 83–98.
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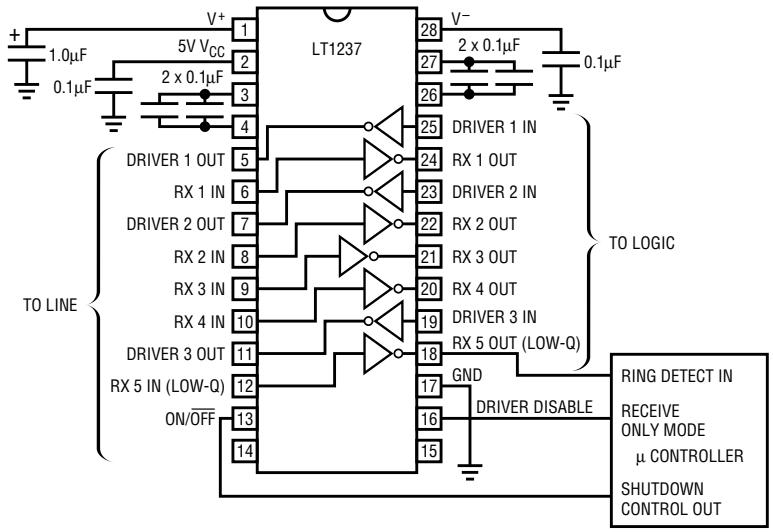


Figure 10. A typical application circuit for the LT1237 under digital control

Anatomy of the LT1237 RS232 Port

The LT1237 is a complete RS232 port, designed specifically for battery-powered computers and instrumentation. The device contains three drivers, five receivers, and a regulated charge pump to reduce supply current. Supply current is typically 6mA, but the device can be shut down with two separate logic controls. The driver-disable pin shuts off the charge pump and the drivers, leaving all receivers active, I_{SUPPLY} = 4mA. The ON/$\overline{OFF}$ pin shuts down all circuitry except for one micropower receiver, I_{SUPPLY} = 60µA. The active receiver is useful for detecting start-up signals. The LT1237 operates up to 120kbaud, and is fully compliant with all RS232 specifications and fault conditions. The flow-through pinout and the LT1237's ability to use small surface-mount capacitors helps reduce the interface's overall footprint. Connections to the RS232 cable are protected with internal ESD structures that can withstand repetitive ±10kV human-body-model ESD pulses.

LT1112/LT1114 Dual/Quad Precision Op Amps have Universal Appeal

by George Erdi

The LT1112 and LT1114 are dual and quad universal precision op amps. The universal description is justified by the fact that all important precision specifications have been optimized:

1. Microvolt offset voltage: the low cost grades (including the small-outline, 8-pin surface-mount package) are guaranteed to 75µV
2. Drift guaranteed to 0.5µV/°C (0.75µV/°C low cost grades)
3. Bias and offset currents are in the picoampere range, even at 125°C
4. Low noise: 0.32µV peak-to-peak, 0.1Hz to 10Hz
5. Supply current is 400µA max. per amplifier
6. Voltage gain is in excess of one million

Therefore, there are very few precision op-amp applications, where the LT1112/LT1114 will not be the dual or quad op amp of choice. They can be stocked as the universal dual or quad and used without time-consuming error-budget calculations. Table 1 lists the guaranteed specifications.

Table 1. LT1112 dual, LT1114 quad low-cost grades, guaranteed specifications V_S = ±15V, T_A = 25°C

Parameter	Typical	Min/Max	Units
Offset Voltage	25	75	µV
Drift with Temperature			
Plastic/CERDIP	0.2	0.75	µV/°C
SO-8	0.4	1.3	µV/°C
Offset Current	60	230	pA
Bias Current	80	280	pA
Noise 0.1 to 10Hz	0.32	—	μV_{P-P}
At 1kHz	13	20	$nV/\sqrt{Hz}$
Supply Current/Amp	350	450	µA
Gain	5000	800	V/mV
CMRR	136	115	dB

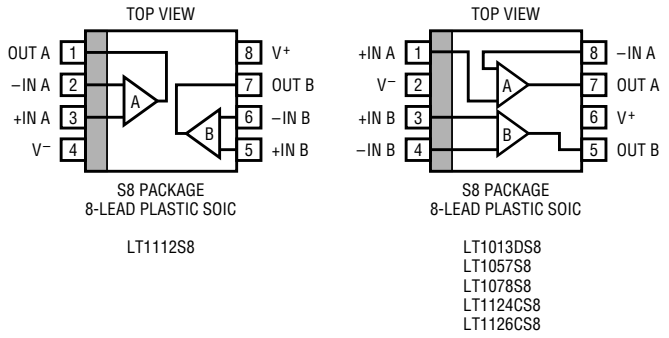


Figure 1. Standard S8 pin configuration and LTC proprietary S8 pin configuration

Standard SO8 Dual-Pin Configuration

The LT1112 is the first dual op amp offered by Linear Technology with the standard SO8 pin configuration (Figure 1), i.e., the pin locations are identical to the plastic or CERDIP packages. Note that the industry-standard package is called the SO8 package. To order this package type, add S8 to the LTC part number, as illustrated in Figure 1.

Matching Specifications

In addition to the outstanding specs of Table 1, the LT1112 and LT1114 also provide a full set of matching specifications, facilitating their use in such matching-dependent applications as two and three op amp instrumentation amplifiers (Table 2). The performance of these instrumentation amplifiers will be limited by the matching parameters only—not by the specifications of the individual amplifiers (Figure 2).

Guaranteed Specs for ±1.0V Supplies

Another set of specifications is furnished for ±1V supplies. This, combined with the low 320µA supply current per amplifier, allows the

Table 2. Guaranteed matching specifications of low-cost grades, V_S = ±15V, T_A = 25°C

Parameter	Typical	Min/Max	Units
Offset Voltage Match	40	130	µV
Drift with Temperature			
Plastic/CERDIP	0.3	1.0	µV/°C
SO-8	0.5	1.9	µV/°C
Non-Inverting Bias Current Match	100	500	pA
Common-Mode Rejection Match	136	113	dB
Power-Supply Rejection Match	130	112	dB

Table 3. Specifications for low-cost grades with ±1.0V supplies, T_A = 25°C

Parameter	Typical	Min/Max	Units
Offset Voltage	45	130	µV
Drift with Temperature			
Plastic/CERDIP	0.25	—	µV/°C
SO-8	0.45	—	µV/°C
Supply Current/Amp	320	420	µA
Common-Mode Range	+250, –320	—	mV
Swing (Light Load)	±270	—	mV

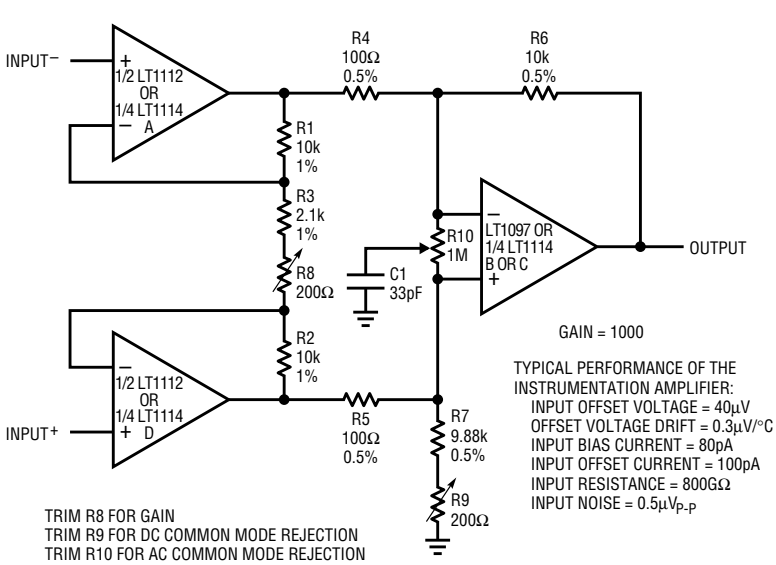
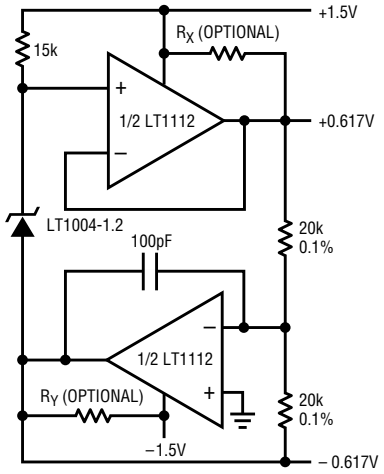


Figure 2. Three op amp instrumentation amp with gain = 100



TOTAL SUPPLY CURRENT = 700µA.

WORKS WITH BATTERIES DISCHARGED TO ±1.3V.

AT ±1.5V: MAXIMUM LOAD CURRENT = 800µA;
CAN BE INCREASED WITH OPTIONAL R_X, R_Y;
AT $R_X = R_Y = 750\Omega$ LOAD CURRENT = 2mA.

TEMPERATURE COEFFICIENT LIMITED BY
REFERENCE = 20ppm/°C.

Figure 3. Dual-output reference operates on two AA cells

LT1112/LT1114 to be powered by two nearly discharged AA cells (Table 3).

A dual-output, buffered reference application is shown in Figure 3.

Figure 3 works on two AA batteries, which can be discharged to ±1.3V. With two equal 20k resistors, two equal but opposite-sign reference voltages are available. Changing the ratio of the two 0.1% resistors allows for other values: one positive and one negative.

LTC1196/1198, continued from page 7

The reference input can be driven with standard voltage references. Bypassing the reference with at least 0.1µF is recommended to keep the high-frequency impedance low. Some references require a small resistor in series with the bypass cap for frequency stability. See the individual reference data sheets for details.

To achieve the full sampling rate, the analog input should be driven with a low-impedance source (<100Ω) or a high-speed op amp (e.g., the LT1223, LT1191, or LT1226). Higher-impedance sources or slower op amps can easily be accommodated by allowing more time between conversions for the analog input to settle.

Digital Considerations

The LTC1196/1198 will interface via three or four wires to ASICs, PLDs, microprocessors, DSPs, and shift registers. To run at its fastest conversion rate (600ns) it must be clocked at 14.3MHz. HC logic families and any high speed ASIC or PLD will easily interface to the ADC at that speed.

Connection to a microprocessor or DSP serial port is very easy. It requires no additional hardware, but the speed will be limited by the clock rate of the microprocessor or DSP. The TMS320 family's 7MHz serial-port clock rate is the fastest available at the present time. This limits the conversion time of the LTC1196/1198 to about 1µs. Full-speed operation can still be achieved with 3V ASICs, PLDs or HC logic circuits. Check the clock frequency and timing specifications of your particular ASIC or PLD.

CONCLUSION

The new LTC1196 and LTC1198 must be considered as an alternative to half-flash ADCs in high-speed data acquisition systems because of their high conversion speeds, small size, low cost, low power consumption, and their ability to operate on both 3V and 5V power supplies.

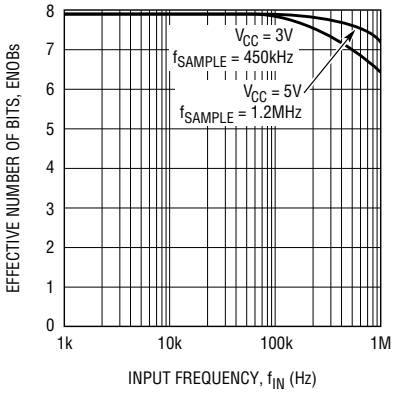


Figure 5. LTC1196/1198 ENOBs vs. input frequency

The LTC1157 Dual 3.3V Micropower MOSFET Driver

by Tim Skovmand

A 3.3V-powered MOSFET driver is now available. The LTC1157 dual micropower MOSFET driver makes it possible to switch either supply- or ground-referenced loads through a low $R_{DS(ON)}$, N-channel switch. N-channel switches are required at 3.3V because P-channel MOSFETs do not have guaranteed $R_{DS(ON)}$ with V_{GS} = 3.3V. The LTC1157's internal charge pump boosts the gate-drive voltage 5.4V above the positive rail (8.7V above ground), fully enhancing a logic-level, N-channel MOSFET for 3.3V high-side switching applications.

On-Chip Charge Pump

The charge pump is completely on-chip and therefore requires no external components to generate the higher gate voltage. Figure 1 is a graph of gate voltage above supply versus supply voltage. The charge pump has been designed to be very efficient, requiring only 3 microamps in the standby mode and 80 microamps while delivering 8.7V to the power MOSFET gate. This makes the LTC1157 particularly well suited for battery-powered applications, which benefit from micropower operation.

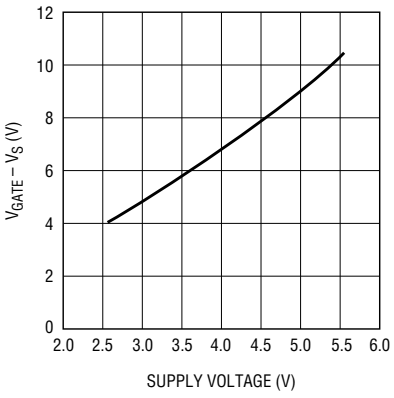


Figure 1. Gate voltage above supply vs. supply voltage

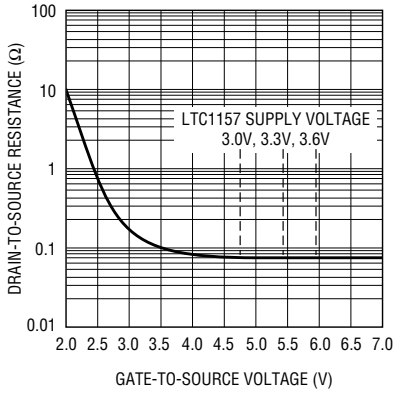


Figure 2. $R_{DS(ON)}$ vs V_{GS} for typical logic level, N-channel MOSFET switch

Logic Level MOSFET Switches

Figure 2 is a graph of $R_{DS(ON)}$ versus V_{GS} for a typical logic-level, N-channel MOSFET switch. The $R_{DS(ON)}$ drops dramatically as the gate voltage is taken above the threshold voltage (1–2V) and begins to flatten off at about 3.5V. Further gate drive does not significantly reduce the $R_{DS(ON)}$, because the MOSFET channel is already fully enhanced. By mapping the LTC1157 supply voltage onto Figure 2, it can be seen that the on-chip charge pump produces ample gate voltage to drive a logic-level, high-side N-channel switch into full enhancement. This combination of a low $R_{DS(ON)}$ MOSFET switch and micropower gate drive produces the maximum switch efficiency in 3.3V and 5V high-side switch applications.

Typical Applications

Figure 3 illustrates how two surface-mount MOSFETs and the LTC1157 (also available in 8-pin SO packaging) can be used to switch two 3.3V loads. The gate rise and fall times are typically in the tens of microseconds, but can be slowed by adding two resistors and a capacitor, as shown on the second channel. Slower rise and fall times are sometimes required to reduce the start-up current demands of large supply capacitors, which might otherwise glitch the main supply.

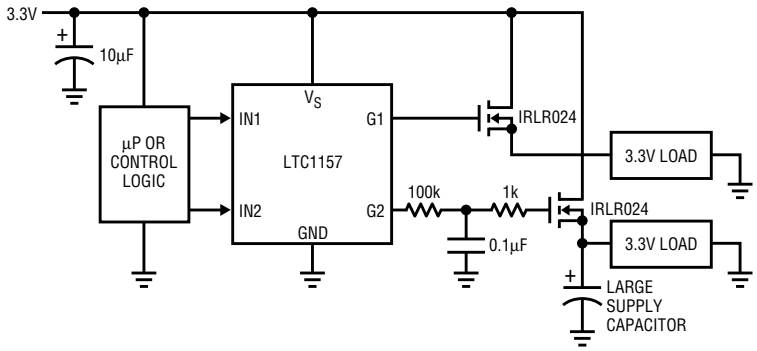


Figure 3. LTC1157 used to switch two 3.3V loads

The World's Lowest-Noise Op Amp is Now Available in 8-pin SO and in a Unity-Gain Stable Version

by George Erdi
and Alexander Strong

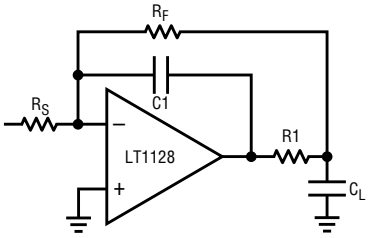


Figure 1. Driving a heavy capacitive load

The LT1028 was introduced in 1986. With its 0.85nV/√Hz noise (less than that of a 50Ω resistor) it became the lowest voltage-noise op amp, wresting the title from the LT1007, which features noise of 2.5nV/√Hz. The LT1028 combined minuscule noise with excellent precision and high-speed specifications (Table 1).

Six years later, the LT1028 is still the reigning low-noise champion. In addition, the LT1028 is now available in the 8-pin small-outline surface-mount package—designated as the LT1028CS8. For many op amps, assembly shifts in the surface-mount packages necessitate a loosening of specifications compared to other packages. For the LT1028CS8, spec relaxation is not necessary. The "C" designation indicates that the LT1028CS8's specifications are identical to the LT1028CH, LT1028CJ8, and LT1028CN8.

The LT1028 is stable in closed-loop gains of +2 or –1, not as a voltage follower. At first glance, this should never be a problem, since proper use of the LT1028 always involves amplification of microvolt-level signals to take advantage of its low noise. However, to optimize noise, the bandwidth of the amplifier should be limited to the bandwidth of the signal being processed. In many applications, the only convenient means of limiting bandwidth is to connect a capacitor (C_F) in parallel with the feedback resistor. At high frequencies this capacitor becomes a short, requiring a unity-gain-stable amplifier.

Enter the LT1128

The LT1028 is stable for many combinations of R_S, R_F, and C_F. The LT1128, however, is unconditionally stable for all values of R_S, R_F, and C_F.

Another example which requires unity-gain stability is shown in Figure 1. Here, a heavy capacitive load, C_L, is isolated from the op amp's output by resistor R1. The extra phase shift caused by the R1, C_L pole is eliminated from consideration by the presence of C1, which shorts the op amp's output to its input at high frequencies.

Op amp instrumentation amplifiers usually have op amps with a fixed gain greater than one at the input stage (Figure 2). At low frequencies, decompensated op amps work well, but at high frequencies and with one input grounded, the virtual ground begins to lose its integrity. As the frequency of the input signal increases, the amplitude at the virtual ground increases, making the virtual ground look inductive, eventually requiring a unity-gain-stable amplifier. The LT1028 can be made stable under these conditions with bypass capacitors and a little experimenting, but the LT1128 is unconditionally stable.

The LT1028/LT1128 team offers the user excellent AC performance, unconditional DC stability, and the lowest noise available in an op amp. All of these features are now available in the SO8 surface mount package.

Table 1. LT1028/LT1128 Comparison

		LT1028A/ 1128A	LT1028C/ 1128C	Units	
V_{OS}		40	80	µV	Max
TCV_{OS}		0.8	1.0	µV/°C	Max
I_B		±90	±180	nA	Max
e_n	10kHz	1.0	1.0	nV/√Hz	Typ
	1kHz	0.85	0.9	nV/√Hz	Typ
	1kHz (100% tested)	1.1	1.2	nV/√Hz	Max
A_{VOL}	R_L = 1k	5.0	5.0	V/µV	Min
SR	1028	11.0	11.0	V/µs	Min
	1128	5.0	4.5	V/µs	Min
GBW	1028 f_0 = 20kHz	50	50	MHz	Min
	1128 f_0 = 200kHz	13	11	MHz	Min

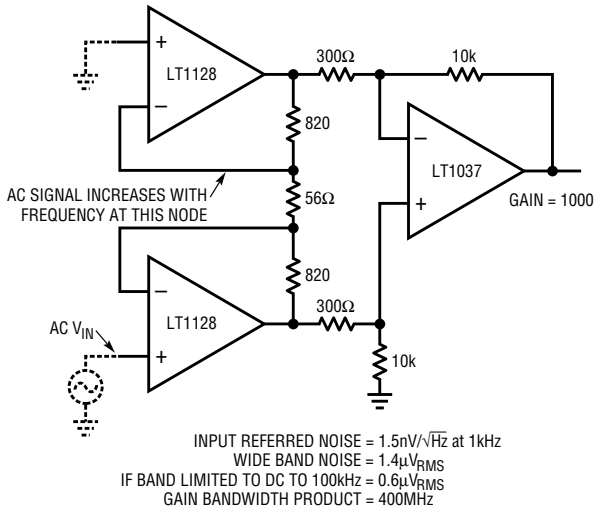


Figure 2. Three op amp, ultra-low noise instrumentation amplifier

A Temperature-Compensated, Voltage-Controlled-Gain Amplifier Using the LT1228

by Frank Cox

It is often convenient to control the gain of a video or intermediate frequency (IF) circuit with a voltage. The LT1228, along with a suitable voltage-to-current converter circuit, forms a versatile gain-control building block ideal for many of these applications. In addition to gain control over video bandwidths, this circuit can add a differential input and has sufficient output drive for 50Ω systems.

The transconductance of the LT1228 is inversely proportional to absolute temperature at a rate of –0.33%/°C. For circuits using closed-loop gain control (i.e., IF or video automatic gain control) this temperature coefficient does not present a problem. However, open-loop gain-control circuits that require accurate gains may require some compensation. The circuit described here uses a simple thermistor network in the voltage-to-current converter to achieve this compensation. Table 1 summarizes the circuit's performance.

Table 1. Characteristics of example

Input Signal Range	0.5V – 3.0V pk
Desired Output Voltage	1.0V pk
Frequency Range	0Hz – 5MHz
Operating Temperature Range	0°C – 50°C
Supply Voltages	±15V
Output Load	150Ω (75Ω + 75Ω)
Control Voltage vs Gain Relationship	0V to 5V Min to Max Gain
Gain Variation Over Temperature	±3% from Gain at 25°C

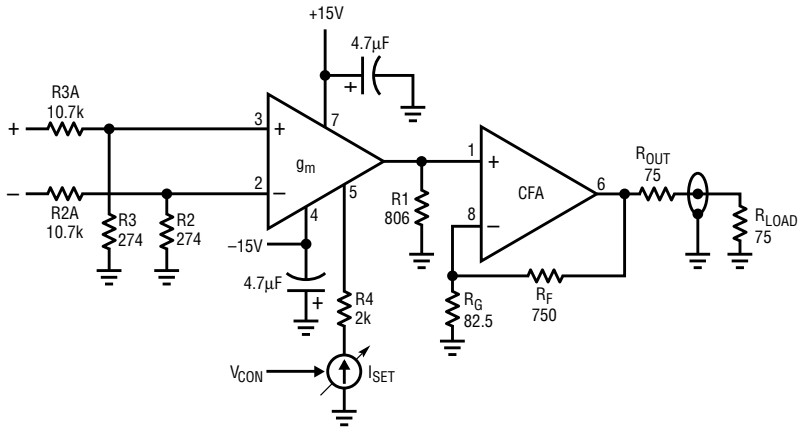


Figure 1. Differential-input, variable-gain amplifier

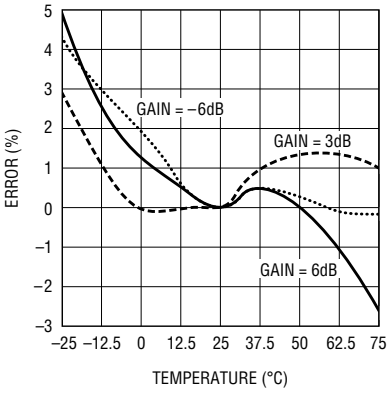


Figure 2. Gain error for circuit in Figure 1 plus temperature compensation circuit shown in Figure 3 (normalized to gain at 25°C)

Figure 1 shows the complete schematic of the gain-control amplifier. Please note that these component choices are not the only ones that will work nor are they necessarily the best. This circuit is intended to demonstrate one approach out of many for this very versatile part and, as always, the designer's engineering judgment must be fully engaged. Selection of the values for the input attenuator, gain-set resistor, and current-feedback-amplifier resistors is relatively straightforward, although some iteration is usually necessary. For the best bandwidth, remember to keep the gain-set resistor, R1, as small as possible, and the set current as large as possible (with due regard for gain compression). The voltage-controlled current source (I_{SET}) is detailed in the boxed section.

Several of these circuits have been built and tested using various gain options and different thermistor values. Test results for one of these circuits are shown in Figure 2. The gain error versus temperature for this circuit is well within the limit of ±3%. Compensation over a much wider range of temperatures or to tighter tolerances is possible, but would generally require more sophisticated methods, such as multiple thermistor networks.

The VCCS is a standard circuit with the exception of the current-set resistor R5, which is made to have a temperature coefficient of –0.33%/°C. R6 sets the overall gain and is made adjustable to trim out the initial tolerance in the LT1228 gain characteristic. A resistor (R_P) in parallel with the thermistor will tend, over a relatively small range, to linearize the change in resistance of the combination with temperature. R_S trims the temperature coefficient of the network to the desired value.

Voltage-Controlled Current Source (VCCS) with a Compensating Temperature Coefficient

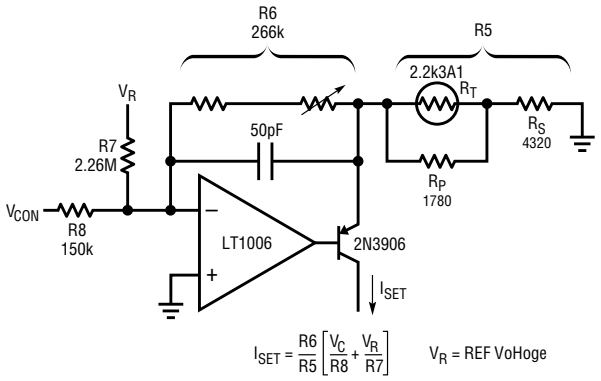


Figure 3. Voltage-controlled current source (VCCS) with a compensating temperature coefficient

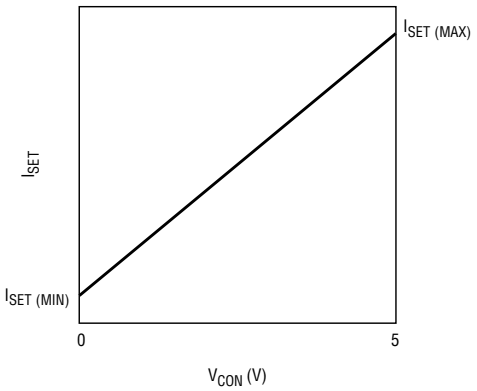


Figure 4. Voltage control of I_{SET} with temperature compensation

VCCS Design Steps

1. Measure or obtain from the data sheet the thermistor resistance at three equally spaced temperatures (in this case 0°C, 25°C, and 50°C). Find R_P from:

$$R_P = \frac{(R0 \times R25 + R25 \times R50 - 2 \times R0 \times R50)}{(R0 + R50 - 2 \times R25)}$$

where R0 = thermistor resistance at 0°C
R25 = thermistor resistance at 25°C
R50 = thermistor resistance at 50°C

2. Resistor R_P is placed in parallel with the thermistor. This network has a temperature dependence that is approximately linear over the range given (0°C–50°C).

3. The parallel combination of the thermistor and R_P ($R_P \| R_T$) has a temperature coefficient of resistance (temp. co.) given by:

$$\text{temp. co. } R_P\|R_T = \left(\frac{R0\|R_P - R50\|R_P}{R25\|R_P}\right)\left(\frac{100}{T_{HIGH} - T_{LOW}}\right)$$

where T_{HIGH} = the high temperature
T_{LOW} = the low temperature
R_T = the thermistor

4. The desired temp. co. to compensate the LT1228 gain temperature dependence is –0.33%/°C. A series resistance (R_S) is added to the parallel network to trim its temp. co. to the proper value. R_S is given by:

$$\frac{(\text{temp. co. } R_P\|R_T)}{(0.33)} \times (R_P\|R_{25}) - (R_P\|R_{25})$$

5. R6 contributes to the resultant temp and so is made large with respect to R5.

6. The other resistors are calculated to give the desired range of I_{SET}.

This procedure was performed using a variety of thermistors (one possible source is BetaTHERM corporation—phone 508-842-0516). Figure 5 shows typical results reported as errors normalized to a resistance with a –0.33%/°C temperature coefficient. As a practical matter, the thermistor need only have about a 10% tolerance for this gain accuracy. The sensitivity of the gain accuracy to the thermistor tolerance is decreased by the linearization network, in the same ratio as is the temperature coefficient; The room temperature gain may be trimmed with R6. Of course, particular applications require analysis of aging stability, interchangeability, package style, cost, and the contributions of the tolerances of the other components in the circuit.

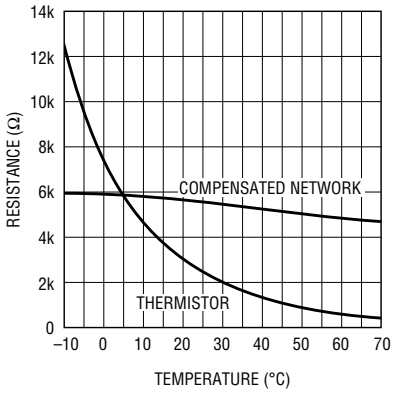


Figure 5. Thermistor and thermistor network resistance vs. temperature

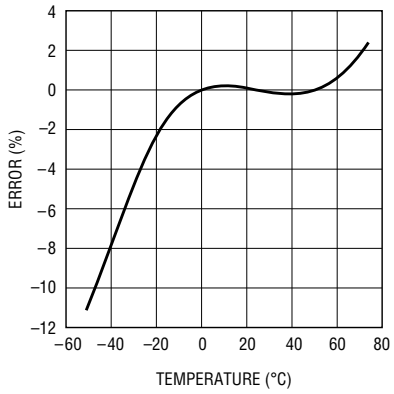


Figure 6. Thermistor-network resistance normalized to a resistor with exact –0.33%/°C temp. co.

Flash-Memory VPP Generator Shuts Down with 0V Output

by Sean Gold

Nonvolatile "flash" memories require a well-controlled 12V bias (VPP) for programming. The tolerance on VPP is ±5% for 12V memories. Excursions in VPP above 14V or below –0.3V are destructive. VPP is often generated with a boost regulator whose output follows the input supply when shut down. It is sometimes desirable to force VPP to 0V when the memory is not in use or in read-only mode.

The circuit in Figure 1 generates a smoothly rising 12V, 60mA supply that drops to 0V under logic control. Shortly after driving the $\overline{\text{SHUTDOWN}}$ pin high, the LT1109-12 switching regulator drives L1, producing high-voltage pulses at the device's switch pin (Figure 2). The 1N5818 Schottky diode rectifies these pulses and charges a reservoir capacitor C2. Q1 functions as a low-on-resistance pass element. The 1N4148 diode clamps Q1 for reverse voltage protection. The circuit does not overshoot or display unruly dynamics, because the regulator gets its DC feedback directly from the output at Q1's collector. Minor slew aberrations are due to Q1's switching characteristics.

Even with the additional losses introduced by Q1, efficiency is 83% with a 60mA load. Line and load regulation are both less than 1%. Output ripple is about 100mV under light loads. Quiescent current drops to 400µA when shut down. All components shown in Figure 1 are available in surface mount packages, making the circuit well suited for flash memory cards and other applications where minimizing pc-board space is critical.

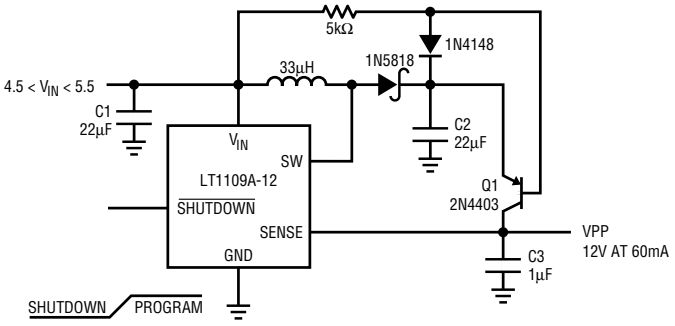


Figure 1. Boost-mode switching regulator with low R-on pass transistor for flash-memory programming

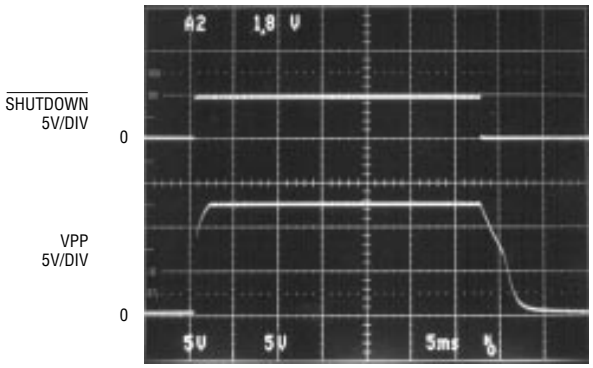


Figure 2. Input and output waveforms for the flash-memory programming circuit

LCD Bias Supply

by Steve Pietkiewicz

An LCD requires a bias supply for contrast control. The supply's variable negative output permits adjustment of display contrast. Relatively little power is involved, easing RF radiation and efficiency requirements. An LCD bias generator is shown in Figure 1. In this circuit, U1 is an LT1173 micropower DC-to-DC converter. The 3V input is converted to +24V by U1's switch, L2, D1, and C1. The switch pin (SW1) also drives a charge pump composed of C2, C3, D2, and D3 to generate –24V. Line regulation is less than 0.2% from 3.3V to 2V inputs. Although load regulation suffers somewhat because the –24V output is not directly regulated, it measures 2% for loads from 1mA to 7mA. The circuit will deliver 7mA from a 2V input at 75% efficiency.

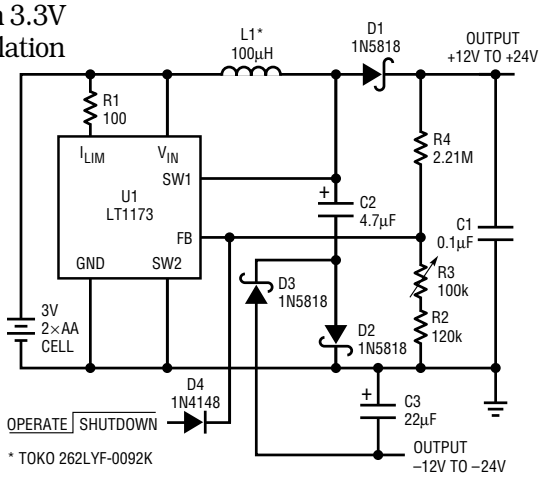


Figure 1. DC to DC Converter Generates LCD Bias

New Device Cameos

LT1201/LT1202: High-Speed, Low-Power, Dual and Quad Operational Amplifiers

The LT1201 is a dual version of the LT1200 high-speed, low-power operational amplifier; the LT1202 is a quad version. Each unity-gain-stable amplifier has an 11MHz gain bandwidth, 50V/µs slew rate, and 430ns settling time to 0.1% (10V step), and draws only 1mA of quiescent supply current. The LT1201/1202 are ideal choices for applications where power consumption and board space must be minimized. With 1mV maximum offset voltage, 100nA maximum offset current, and 8V/mV open-loop gain combined with fast settling, the LT1201/1202 are excellent choices for fast data-acquisition systems.

Each amplifier can drive a 2kΩ load to ±12V from a ±15V supply and can drive 500Ω to ±3V on ±5V supplies. The amplifiers are stable with all capacitive loads, which makes them useful as buffers or for driving A-to-D converters. Wideband active filters are another excellent application, especially where power consumption is critical due to battery operation.

The LT1201 comes in the industry-standard pinout in 8-lead plastic mini-DIP or 8-lead, small-outline surface-mount package. The LT1202 comes in 14-lead plastic DIP.

LT1208/LT1209: 50MHz, 400V/µs Dual and Quad Operational Amplifiers

The LT1208 is a dual version of the LT1224 high-speed operational amplifier; the LT1209 is a quad version. Each amplifier is unity-gain stable with 50MHz gain bandwidth, 400V/µs slew rate, 90ns settling time to 0.1% (10V step), and 7mA of supply current. The LT1208 and LT1209 are ideal choices for applications where high speed is essential and board space must be minimized.

The LT1208/1209 DC specifications include 2mV maximum offset voltage, 400nA maximum offset current, and 7V/mV open-loop gain. The outputs can drive a 500Ω load to ±12V with a ±15V supply and can drive 150Ω to ±3V on a ±5V supply.

The amplifiers are stable with all capacitive loads, which makes them useful as buffers or in cable-driving applications. The excellent settling time lends itself to data-acquisition applications, such as DAC current-to-voltage converters and A-to-D input buffers. Other applications include wide-band active filters, RF amplification, and video amplifiers.

The LT1208 comes in the industry-standard pinout in an 8-lead plastic mini-DIP or 8-lead small-outline surface-mount package. The LT1209 comes in 14-lead plastic DIP.

The LTC1250 Very-Low-Noise Bridge Op Amp

The LTC1250 is a zero-drift op amp optimized for use with bridge transducers. It features typical 0.1Hz–10Hz noise of $0.65\mu V_{P-P}$ and 0.1Hz–1Hz noise of $0.2\mu V_{P-P}$, making it ideal for use with low noise, low frequency signals. The LTC1250's 10µV maximum offset, 50nV/°C maximum drift, and ±150pA maximum bias currents keep DC errors negligible. The zero-drift loop samples the input at 5kHz, allowing signals up to 2.5kHz to be amplified with no aliasing. All of the zero-drift circuitry is integrated on-chip, allowing the LTC1250 to plug into standard op-amp sockets with no additional external components.

The LTC1250 has an enhanced CMOS output stage capable of swinging ±4V into 1kΩ with ±5V supplies; it will swing to within millivolts of the rail into lighter loads. 10V/µs slew rate and 1.5MHz gain bandwidth allow the LTC1250 to track input transients. The inputs recover from overload in 1.5ms, many times faster than standard zero-drift op amps with external capacitors. The LTC1250 is ideally suited for electronic scales, pressure transducers, and low-frequency digitizing applications.

The LTC1154 High-Side, Microprocessor-Compatible, Micropower MOSFET Driver

The LTC1154 single micropower gate driver is designed to drive a standard N-channel power MOSFET in a high-side switch configuration. The LTC1154 contains an on-chip charge pump so that less expensive, lower $R_{DS(ON)}$ N-channel MOSFETs can be used in place of P-channel switches. The charge pump requires no external components and has been designed to be very efficient, requiring only microamps to operate.

All of the circuitry to drive, control, and protect the power MOSFET and load, and to interface to a host microprocessor, are provided by the LTC1154. The input is compatible with both TTL and CMOS logic families and the standby current with the input switched off is only 8 microamps from a 5V supply. The quiescent current rises to 85 microamps when the switch is turned on and the charge pump is producing 12V from a 5V supply. An active-low enable input is provided to control multiple LTC1154 switches in banks. An open-drain status output is provided to advise the microprocessor when a fault condition exists at the output of the switch. If an over-current condition is detected at the drain end of the power MOSFET, the output is latched off and the status pin is pulled low. A built-in 10-microsecond delay ensures that the LTC1154 protection circuitry is not false triggered by transient load or power-supply conditions. A longer RC delay can be added externally to accommodate loads with large transient start-up current requirements, such as lamps or DC motors.

The versatile microprocessor interface, coupled with the comprehensive protection features and micropower operation, make the LTC1154 the ideal choice for applications that require maximum efficiency and protection on a lean power budget. And the 8-lead SO packaging makes it the ideal choice for applications with a lean board-space budget.

LT1269: 4A, 100kHz, High-Efficiency Switching Regulator

A new integrated switching regulator IC, the LT1269, allows high-efficiency converters to be constructed using smaller inductors than were required with previous devices.

Similar to the LT1271 and other members of LTC's 5-pin integrated switching-regulator family, the LT1269 contains a 100kHz current-mode PWM control section, a fully integrated 4A high-efficiency switch, and fault protection on a single chip. It can be operated in all standard switching configurations, including buck (step-down), boost (step-up), flyback, inverting, and others.

Used with a companion control chip, the LT1432, the LT1269 can be used to make a very-high-efficiency 5V step-down regulator for use with the typical NiCad and Nickel-Hydride battery packs used in portable computers. In addition to providing high efficiency (≈ 90%) at load currents of 1A and beyond, the device, when used with the LT1432, accomplishes the difficult task of maintaining high efficiency under low power-demand conditions. Such conditions are encountered in portable computers when power-management schemes such as "suspend-mode" are employed.

A 3.3V version of the LT1432 that allows the LT1269 to be used to generate 3.3V logic supplies with high efficiency is now available (see below). The LT1269 comes in a 5-lead TO-220 and a 5-lead DD surface-mount package is planned for future release.

LT1432: 3.3 High-Efficiency, Step-Down Switching-Regulator Controller

The LT1432-3.3 is an 8-pin control chip designed to work in conjunction with LTC's family of 5-pin integrated switching regulators to make very-high-efficiency 3.3V switching regulators with advanced power-management capability.

High efficiency at nominal output currents from 0.1A to over 3A is achieved by employing one of LTC's LT1070 family of low-loss switching regulators in buck mode, while using the LT1432-3.3 for feedback signal conditioning. Portable, battery-powered systems achieve significant power savings for increased battery life by using an idle or "suspend" mode when the system is not actively in use. Notebook computers typically employ such a power-saving scheme. In the suspend mode, when output load demand is light, the LT1432-3.3 can place the main regulator into a "burst" mode to maintain high efficiency at low load currents (0 to 50mA). A logic-compatible shutdown pin is included that, when taken high, shuts the entire regulator down.

The LT1432-3.3 is offered in an 8-lead SOIC package and an 8-pin mini-DIP.

LT1129: 700mA Low-Iq, Low-Dropout Regulator

The LT1129 is a low-dropout regulator with ultra-low quiescent current and shutdown current. The device can supply over 700mA of output current with a dropout voltage of 0.4V at maximum output. The low 50µA quiescent current in operating mode and 30µA in shutdown mode is perfect for battery powered operation. This quiescent current does not rise in the dropout region as it does with other low-dropout PNP regulators.

Other features of the LT1129 include the ability to operate with small output capacitors. Stability is guaranteed with only 3.3µF of output capacitance, whereas other low-dropout regulators require as much as 100µF. The input of the LT1129 may be connected to ground, or reverse input voltages may be applied without current flow from the output to the input. This makes LT1129 ideal for back-up power applications where the output is held high while the input is at ground.

The device is available in 5-lead TO-220 and surface mount DD packages.

New Publications

AN49: Illumination Circuitry for Liquid Crystal Displays (Tripping the Light Fantastic...) Liquid crystal displays have become almost universal in portable instruments and computers. In dimly lit environments some form of backlighting is required to make the LCD panel readable. The preferred light source is a cold-cathode fluorescent lamp, otherwise known as a "CCFL."

CCFLs are relatively efficient light sources, but they require special power supplies to develop high starting and running voltages (up to 1kV). AN49 explains the nature of the CCFL as a load, and tells how to design a suitable power supply.

The circuits described in AN49 preserve the overall efficiency of the CCFL to extend battery life in portable systems and eliminate "hot spots" inside the product.

AN51: Power Conditioning for Notebook and Palmtop Systems Notebook and palmtop systems need a multiplicity of regulated voltages developed from a single battery. Small size, light weight, and high efficiency are mandatory for competitive solutions in this area. Small increases in efficiency extend battery life, making the final product much more usable with no increase in weight. Additionally, high efficiency minimizes the heat sinks needed on the power-regulating components, further reducing system weight and size.

AN51 presents a collection of twenty circuits that represent state-of-the-art solutions to power-supply problems in portable computing products. These circuits were designed for high efficiency and small size, and cover every requirement from battery charging to LCD-bias generation. LT

For further information on the above or any other devices mentioned in this issue of* Linear Technology, *use the reader service card or call the LTC literature-service number: (800) 637-5545. Ask for the pertinent data sheets and application notes.

DESIGN TOOLS

Applications on Disk

NOISE DISK
This IBM-PC (or compatible) progam allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise, and calculate noise using specs for any op amp.
Available at no charge.

SPICE MACROMODEL DISK
This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models, and a demonstration copy of PSPICE™ by MicroSim.
Available at no charge.

Technical Books

1990 Linear Databook — This 1,440 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices.
$10.00

1992 Linear Databook Supplement — This 1248 page supplement to the *1990 Linear Databook* is a collection of all products introduced since then. The catalog contains full data sheets for over 140 devices. The *1992 Linear Databook Supplement* is a companion to the *1990 Linear Databook*, which should not be discarded.
$10.00

Linear Applications Handbook — 928 pages full of application ideas covered in depth by 40 Application Notes and 33 Design Notes. This catalog covers a broad range of "real world" linear circuitry. In addition to detailed, systems-oriented circuits, this handbook contains broad tutorial content together with liberal use of schematics and scope photography. A special feature in this edition includes a 22-page section on SPICE macromodels.
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Monolithic Filter Handbook — This 232 page book comes with a disk which runs on PCs. Together, the book and disk assist in the selection, design and implementation of the right switched capacitor filter circuit. The disk contains standard filter responses as well as a custom mode. The handbook contains over 20 data sheets, Design Notes and Application Notes.
$40.00

SwitcherCAD Handbook — This 144 page manual, including disk, guides the user through SwitcherCAD – a powerful PC software tool which aids in the design and optimization of switching regulators. The program can cut days off the design cycle by selecting topologies, calculating operating points and specifying component values and manufacturer's part numbers.
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