Introduction
Routine maintenance and upgrades to high reliability computing, networking and telecommunications systems require that new or replacement circuit boards be inserted into a powered 48V (typical) bus. When a circuit board is inserted into a live backplane, the input capacitors on the board can draw high inrush currents from the backplane power bus as they charge. The inrush current can permanently damage the connector pins and board components as well as glitch the system supply, causing other boards in the system to reset. The new LT4256 family (LT4256-1 and LT4256-2) provides a compact and robust solution to eliminate these hot plugging issues.

The LT4256 is designed to turn on a board’s supply voltage in a controlled manner, allowing the board to be safely inserted or removed from a live backplane having a supply voltage from 10.8V to 80V. The device features programmable inrush current control, current foldback, programmable undervoltage threshold with a 1% tolerance, overcurrent protection, and a power good output signal that indicates when the output supply voltage is ready.

The LT4256-1 and LT4256-2 are offered in an 8-pin SO package and are pin compatible with the LT1641-1 and LT1641-2. The LT4256 family upgrades the LT1641 and offers several superior electrical specifications (see Table 1), requiring only a few minor component modifications.

Power-Up Sequence
Figure 1 shows a typical LT4256 application. An external N-channel MOSFET pass transistor (Q1) is placed in the power path to control the turn-on and turn-off characteristics of the supply voltage. Capacitor C1 controls the GATE slew rate, R7 provides compensation for the current control loop and R6 prevents high frequency oscillations in Q1. When the power pins first make contact, transistor Q1 is

Table 1. Differences between LT1641 and LT4256

<table>
<thead>
<tr>
<th>SPECIFICATION</th>
<th>LT1641</th>
<th>LT4256</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>UV Threshold</td>
<td>1.233V</td>
<td>4V</td>
<td>Higher 1% Reference for Better Noise Immunity and System Accuracy</td>
</tr>
<tr>
<td>FB Threshold</td>
<td>1.233V</td>
<td>3.99V</td>
<td>Higher 1% Reference for Better Noise Immunity and System Accuracy</td>
</tr>
<tr>
<td>TIMER Current</td>
<td>±70%</td>
<td>±26%</td>
<td>More Accurate TIMEOUT</td>
</tr>
<tr>
<td>TIMER Shutdown V</td>
<td>1.233V</td>
<td>4.65V</td>
<td>Higher Trip Voltage for Better Noise Immunity</td>
</tr>
<tr>
<td>GATE IPULLUP</td>
<td>10µA</td>
<td>30µA</td>
<td>Higher Current to Accommodate Higher Leakage MOSFETs or Parallel Devices</td>
</tr>
<tr>
<td>GATE Resistor</td>
<td>1kΩ</td>
<td>100Ω</td>
<td>Different Compensation for Current Limit Loop</td>
</tr>
<tr>
<td>Foldback ILIM</td>
<td>12mV</td>
<td>14mV</td>
<td>Slightly Different Current Limit Trip Point</td>
</tr>
<tr>
<td>ILIM Threshold</td>
<td>47mV</td>
<td>55mV</td>
<td>Slightly Different Current Limit Trip Point</td>
</tr>
</tbody>
</table>
DESIGN FEATURES

held off. The $V_{CC}$ and GND connector pins should be longer than the pin that goes to R1 so they connect first and keep the LT4256 off until the board is completely seated in its connector. When the voltage on the $V_{CC}$ pin is above the externally programmed undervoltage threshold, transistor Q1 is turned on (Figure 2). The voltage at the GATE pin rises with a slope equal to $30\mu A/C_1$ and the supply inrush current is:

$$I_{INRUSH} = C_1 \times \frac{30\mu A}{C_1}$$

where $C_1$ is the total load capacitance. If the voltage across the sense resistor reaches $55mV$ (typical), the inrush current is limited by the internal current limit circuitry. When the FB pin voltage goes above $4.45V$, the PWRGD pin goes high.

**Short-Circuit Protection**

The LT4256 features a programmable foldback current limit with an electronic circuit breaker that protects against short circuits or excessive load currents. The current limit is set by placing a sense resistor (R5) between $V_{CC}$ and SENSE. To limit excessive power dissipation in the pass transistor and to reduce voltage spikes on the input supply during short-circuit conditions at the output, the current folds back as a function of the output voltage, which is sensed internally on the FB pin. When the voltage at the FB pin is 0V, if the part goes into current limit, the current limit circuitry drives the GATE pin to force a constant $14mV$ drop across the sense resistor.

Under high current (but not short-circuit) conditions, as the FB voltage increases linearly from 0V to 2V, the controlled voltage across the sense resistor increases linearly from $14mV$ to $55mV$ (see Figure 3). With FB above 2V, a constant $55mV$ is maintained across the sense resistor.

During startup, a large output capacitance can cause the LT4256 to go into current limit. The current limit level when $V_{OUT}$ is low is only one quarter of the current limit level under normal operation, and it is time limited, so careful attention is needed to insure proper start up. The maximum time the LT4256 is allowed to stay in current limit is defined by the TIMER pin capacitor.

The current limit threshold (during normal operation) is:

$$I_{LIMIT} = \frac{55mV}{R5}$$

where $R5$ is the sense resistor. For a $0.02\Omega$ sense resistor, the current limit is set at $2.75A$ and folds back to $700mA$ if the output is shorted to ground.

For a 48V application, MOSFET peak power dissipation under short circuit conditions is reduced from 132W to 33.6W.

The LT4256 also features a variable overcurrent response time. The time required for the part to regulate the GATE pin voltage is proportional to the voltage across the sense resistor, R5. This helps to eliminate sensitivity to current spikes and transients that might otherwise unnecessarily trigger a current limit response and increase MOSFET dissipation.

**Current Limit TIMER**

The TIMER pin provides a method for programming the maximum time the part is allowed to operate in current limit. When the current limit circuitry is not active, the TIMER pin is pulled to GND by a $3\mu A$ current source. When the current limit circuitry becomes active, a $118\mu A$ pull-up current source is connected to the TIMER pin and the voltage rises with a slope equal to $115\mu A/C_2$. Once the desired maximum current limit time is chosen, the capacitor value is:

$$C(nF) = 25 \times t(ms)$$

If the TIMER pin reaches $4.65V$ (typ), the internal fault latch is set causing the GATE to be pulled low and the TIMER pin to be discharged to GND by the $3\mu A$ current source. The LT4256-1 latches off after a current limit fault. The LT4256-2 does not turn on again until the voltage at the TIMER pin falls below $0.65V$ (typ).

**Undervoltage Detection**

The LT4256 uses the UV (undervoltage) pin to monitor $V_{IN}$ and allow the user the greatest flexibility for setting the operational threshold. Figure 1 also shows the UV level programming via a resistor divider (R1 and R2). If the UV pin goes below $3.6V$, the GATE pin is immediately pulled low until the UV pin voltage goes above $4V$. The UV pin is also used to reset the current limit fault latch after the LT4256-1 has latched off. This is accomplished by grounding the UV pin for a minimum of $5\mu s$.

continued on page 29
Automatic Restart and Latch Off Operation

Following a current fault, the LT4256-2 provides automatic restart by allowing Q1 to turn on when voltage on the TIMER pin has ramped down to 650mV. If the overcurrent condition at the output persists, the cycle repeats itself until the overcurrent condition is relieved. The duty cycle under short-circuit conditions is 3%, which prevents Q1 from overheating (see Figure 4).

The LT4256-1 latches off after a current fault (see Figure 5). After the LT4256-1 latches off, it can be commanded to restart by cycling UV to ground and then above 4V. This command can only be accepted after the TIMER pin discharges below the 0.65V (typ) threshold (to prevent overheating transistor Q1).

Power Good Detection

The LT4256 includes a comparator for monitoring the output voltage. The output voltage is sensed through the FB pin via an external resistor string. If the FB pin goes above 4.45V, the comparator’s output releases the PWRGD pin so it can be externally pulled up. The comparator’s output (PWRGD pin) is an open collector capable of operating from a pull-up voltage as high as 80V, independent of VCC.

GATE Pin

The GATE pin is clamped to a maximum of 12.8V above the VCC voltage. This clamp is designed to sink the internal charge pump current. An external Zener diode must be used from VOUT to GATE. When the input supply voltage is between 12V and 15V, the minimum gate drive voltage is 4.5V, and a logic level MOSFET must be used. When the input supply voltage is higher than 20V, the gate drive voltage is at least 10V, and a MOSFET with a standard threshold voltage can be used.

Conclusion

The LT4256’s comprehensive set of advanced protection and monitoring features make it applicable in a wide variety of Hot Swap™ solutions. It can be programmed to control the output voltage slew rate and inrush current. It has a programmable undervoltage threshold, and monitors the output voltage via the PWRGD pin. The LT4256 provides a simple and flexible Hot Swap solution with the addition of only a few external components.