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# Take the Easy Road to Digitally Managed Power

by Andy Gardner

## Introduction

Digital management of high availability power supplies holds great promise, but it often comes at the cost of complicated multichip circuit solutions. For example, an application with voltage-current monitoring and supply voltage margining can require a number of ICs, including a low-drift reference, a multichannel, differential input ADC with at least 12 bits of resolution, an 8-bit DAC, and a dedicated microcontroller. Add to this the considerable software development effort required for margining algorithms, voltage and current monitor functions, and the cost, complexity, spacious board real-estate

requirements and blossoming design-debug time can deter even the most dedicated power supply designer from trying digitally managed power.

The LTC2970 simplifies the design of digitally managed power supplies by incorporating important features into one easy-to-use device: a dual power supply monitor and controller. Figure 1 shows a block diagram of the LTC2970, highlighting the following features:

❑ A 14-bit, differential input,  $\Delta\Sigma$  ADC with a maximum total unadjusted error (TUE) of  $\pm 0.5\%$  over the industrial temperature range when using the on-chip reference.

❑ A 7-channel ADC multiplexer with four external differential inputs, a 12V input, a 5V  $V_{DD}$  input, and an input for the on-chip temperature sensor.

❑ Two continuous time, 8-bit, current output DACs with voltage buffered outputs. The outputs of the voltage buffers can be placed in a low leakage, high impedance state.

❑ A built-in, closed-loop servo algorithm that adjusts the point-of-load voltage of a DC/DC converter to the desired value. The range and resolution of the voltage servo is user adjust-

able with two external resistors.

❑ Extensive, user configurable overvoltage and undervoltage fault monitoring.

❑ An I<sup>2</sup>C and SMBus compliant 2-wire serial bus interface, two GPIO pins, and an  $\overline{\text{ALERT}}$  pin.

❑ An on-chip, 5V, linear regulator that allows the LTC2970 to operate from an external 8V to 15V voltage supply.

❑ Another part in the family, the LTC2970-1, adds a tracking algorithm that allows two or more power supplies to be ramped up and down in a controlled manner.

*continued on page 3*

**The LTC2970  
simplifies the design of  
digitally managed power  
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important features into one  
easy-to-use device.**



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# Issue Highlights

**D**igital management of high availability power supplies holds great promise, but it often comes at the cost of complicated multichip circuit solutions. The LTC2970 simplifies the design of digitally managed power supplies by incorporating important features into one easy-to-use device.

See our cover article for more about this breakthrough device.

## Featured Devices

Below is a summary of the other devices featured in this issue.

The LTC3415 provides a compact, simple, complete and versatile **point-of-load power supply with 7A capability**. (Page 6)

The LTC4304 is a **hot swappable 2-wire bus buffer** that features pro-

prietary stuck bus protection circuitry to unburden the MCU from the tasks of monitoring, troubleshooting and resolving stuck I<sup>2</sup>C buses. (Page 10)

The LTC4261 integrates a **-48V Hot Swap controller**, 10-bit ADC monitoring and I<sup>2</sup>C/SMBus communication. It monitors the real-time board parameters such as current and voltages and communicates the data to the host. (Page 13)

The LTC4011 is a **complete stand-alone nickel chemistry fast charger** that operates at high efficiency with an input voltage of up to 34V, even with a battery voltage that is much less than the DC input supply. (Page 19)

The LT3750 is a current-mode flyback controller optimized for **charging large value capacitors** to a user selected target voltage. (Page 22)

The LTC2926 **MOSFET-controlled power supply tracker** provides exceptionally flexible control of supply tracking and sequencing. (Page 24)

The LTC3783 is a **current-mode boost controller** optimized for constant-current True Color PWM™ dimming of **high powered LEDs**. (Page 31)

The LTC3412A is a **monolithic buck regulator in a 4mm × 4mm QFN** that can deliver efficiencies to 95% and operate at 4MHz. (Page 34)

## Design Ideas and Cameos

Design Ideas start on page 37, including a, low noise, very low drift FET amplifier; a simple, digitally tunable active RC filter; and a way to increase the dimming range of an LED driver. Cameos appear on page 46. 

## Linear Technology in the News...

### EDN Magazine Nominates Linear for Innovation Awards

EDN magazine has announced nominations for its annual EDN Innovation Awards, honoring outstanding engineering professionals and products.

Linear Technology's LTM4600 high power DC/DC  $\mu$ Module is nominated for an award in the Power Systems and Modules category. The LTM4600 is the first in a new family  $\mu$ Modules from Linear Technology that leverages the company's core strengths in power management and conversion. The LTM4600 provides designers with a complete 10A switching power supply in a tiny, low profile package that can be mounted on either side of a PC board.

EDN has also nominated for Best Contributed Article, Jim Williams' article, "Minimizing Switching Regulator Residue in Linear Regulator Outputs." Winners will be announced in the April issue of EDN.

### Linear A/D Converters Nominated for EE Times ACE Awards

EE Times announced that they have nominated Linear Technology's family of A/D converters as an Ultimate Product Finalist in the Analog category in the 2006 EE Times ACE Awards. The publication highlights the most significant products of the past year, with EE Times' readers selecting finalists from a list of Ultimate Products chosen by the publication's editors. EE Times will announce the ACE Award winners in April.

Linear Technology now offers a broad line of high performance A/D converters. These ADCs at 10, 12, 14 and 16 bits, and up to 185Msps, have the lowest noise and provide extremely high bandwidth for undersampling. Linear's A/D converter family also includes 3V devices, featuring the lowest power consumption and smallest solution size, spanning sampling rates from 10 to 125Msps at 10-, 12- and 14-bit resolution.

### Electronic Products Selects LTM4600 $\mu$ Module as Product of the Year

Electronic Products magazine selected Linear Technology's LTM4600  $\mu$ Module for their Product of the Year Awards, honoring the most significant new products of the past year.

The LTM4600 was highlighted in a cover article in the January issue of *Electronic Products*, as well as in a February feature on how the product came about.

*Electronic Products'* editors commented, "Representing a new level of device integration for DC/DC conversion, the LTM4600  $\mu$ Module synchronous switchmode DC/DC converter from Linear Technology is a complete power supply that can be placed almost anywhere on the board—even on the bottom—as it offers a reduction in space and circuit complexity of up to 60% over solutions using multiple components." 

LTC2970, continued from page 1

### Margining and Monitoring Application

Figure 2 shows a typical application circuit for monitoring and margining a DC/DC converter with external feedback resistors.

The LTC2970's  $V_{IN0\_A}$  differential inputs sense the voltage directly at the point-of-load while inputs  $V_{IN0\_B}$  monitor the voltage across sense resistor  $R_{50}$ . The DC/DC converter's output voltage can be margined to precise, user-programmable set points by a

linear search algorithm that compares the digitized point-of-load voltage against the target. The current being sourced by IDACO is then adjusted as needed one LSB per servo iteration. This current develops a point-of-load ground referenced correction voltage across resistor  $R_{40}$  which is buffered to the  $V_{OUT0}$  pin. The resulting voltage differential between the  $V_{OUT0}$  pin and the converter's feedback node is multiplied by a factor of  $-R_{20}/R_{30}$  and added to the nominal output voltage of the DC/DC converter, thus closing

the servo loop. When voltage margining is disabled, the converter's feedback node can be isolated from the LTC2970 by placing the  $V_{OUT0}$  pin in a high impedance state.

Figure 3 shows the LTC2970 applied to a DC/DC converter with a TRIM pin. As in Figure 2, two external resistors are required:  $V_{OUT0}$  connects to the TRIM pin through resistor  $R_{30}$  and  $I_{OUT0}$  is terminated at the DC/DC converter's point-of-load ground by  $R_{40}$ . Following power-up, the  $V_{OUT0}$  pin defaults to a high impedance

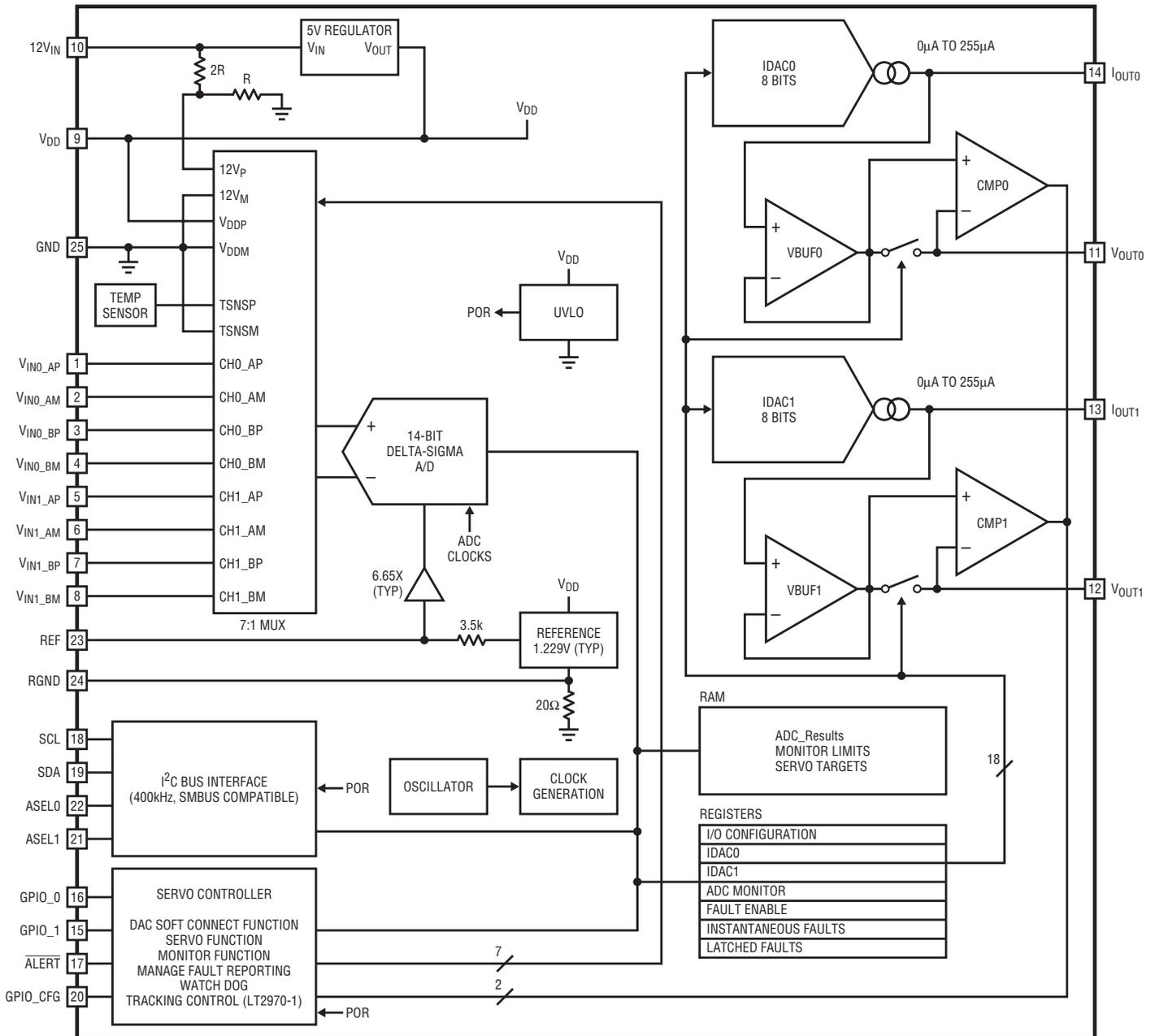


Figure 1. Block diagram of the LTC2970

state allowing the DC/DC converter to power-up to its nominal output voltage. After power-up, the LTC2970's soft-connect feature can be used to automatically find the IDAC code that most closely approximates the TRIM pin's open-circuit voltage before enabling  $V_{OUT0}$ .

Applications that need to be sequenced can be configured to hold off the DC/DC converter when the LTC2970 powers-up by tying the GPIO\_CFG pin high. This causes the GPIO\_0 pin to automatically pull the DC/DC converter's RUN pin low until the SMBus compatible I<sup>2</sup>C interface releases it.

The absolute accuracy of the LTC2970 is demonstrated in Figure 4. The LTC2970 is configured to servo one of the outputs of a LTC3728 DC/DC converter to 1V if the converter's voltage deviates by more than  $\pm 0.1\%$ . The LTC2970 is easily able to hold the output voltage to within  $\pm 1\text{mV}$  of 1V while both it and the DC/DC converter are heated from  $-50^{\circ}\text{C}$  to  $100^{\circ}\text{C}$ . When the LTC2970 is isolated from the LTC3728, the output voltage drifts between 1.002V and 1.0055V over the same temperature range.

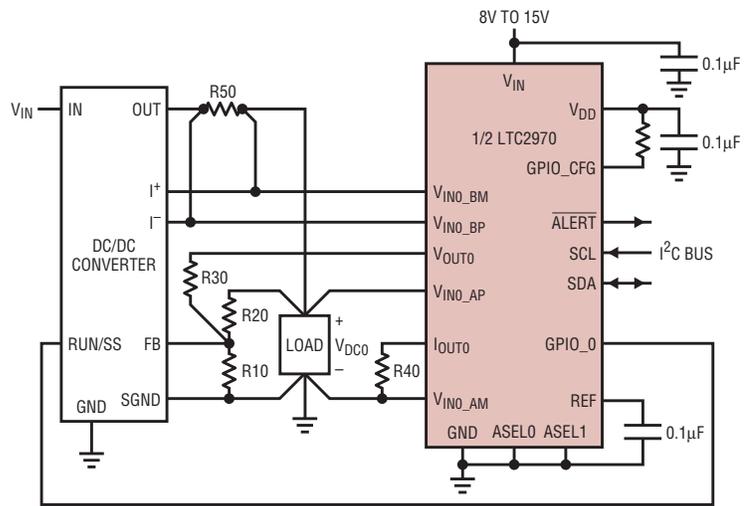
**Features**

The LC2970's features offer several benefits that differentiate it from competitive solutions:

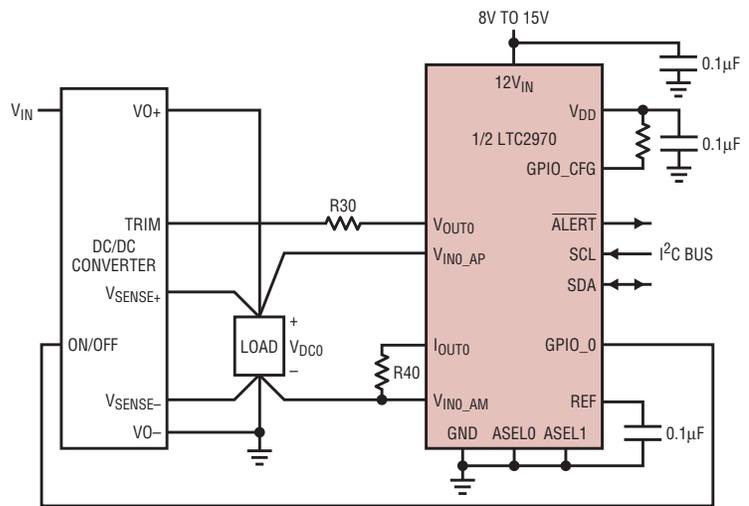
**Delta-Sigma ADC**

The LTC2970's ADC is a second-order delta-sigma modulator followed by a sinc<sup>2</sup> digital filter that converts the modulator's serial data into a 14-bit word at a conversion rate of 30Hz. The ADC's TUE is less than  $\pm 0.5\%$  when using the on-chip reference.

One advantage delta-sigma ADCs offer over conventional ADCs is on-chip digital filtering. Combined with a large over-sampling ratio (OSR = 512), this feature makes the LTC2970 insensitive to the effects of noise when sampling power-supply voltages. The LTC2970's sinc<sup>2</sup> digital filter provides high rejection except at integer multiples of the modulator sampling frequency,  $f_s = 30.72\text{kHz}$ . Adding a simple RC low-pass filter at the input of the ADC



**Figure 2. Application circuit for DC/DC converter with external feedback resistors**

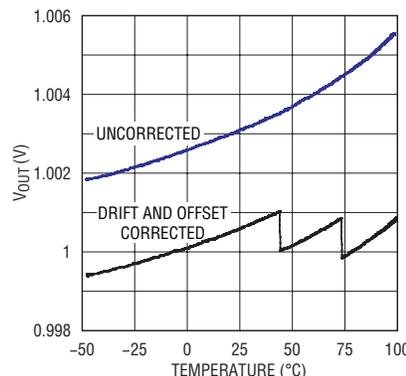


**Figure 3. Application circuit for a DC/DC converter with a trim**

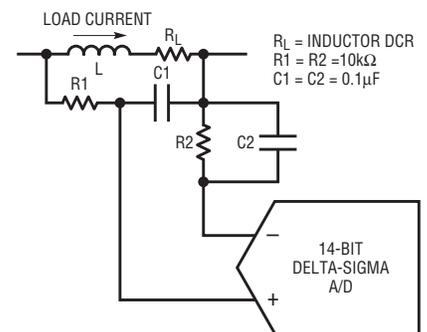
attenuates ripple components that have the potential to alias to DC.

The ADC's differential inputs can monitor supply voltages at the point of load and sense resistor voltages.

The differential and common mode input ranges span  $-0.3\text{V}$  to  $6\text{V}$ . With its  $500\mu\text{V}/\text{LSB}$  resolution, the ADC can resolve voltages for a wide range of load current across sense resistor values of only a few milliohms. For



**Figure 4. Corrected and uncorrected DC/DC converter output voltage vs temperature**



**Figure 5. Network for sensing load current with inductor DCR**

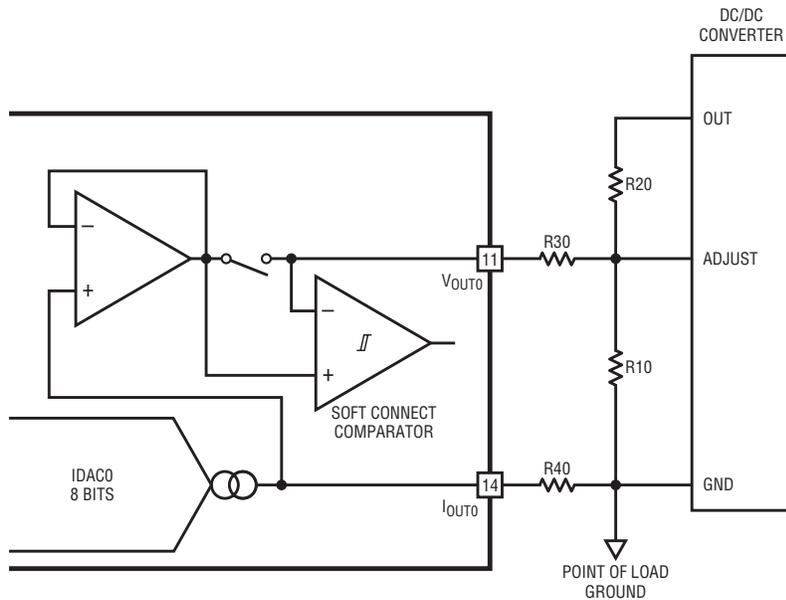


Figure 6. DAC connections to DC/DC converter with an external feedback resistors

disturbance to the converter's output voltage.

There is no body diode from the  $V_{OUT0}$  pin to the LTC2970's  $V_{DD}$  supply, and the  $V_{OUT0}$  pin goes into a high impedance state when  $V_{DD}$  drops below the LTC2970's undervoltage lockout threshold. So no special precautions need to be taken in the event the DC/DC converter is still active when the LTC2970 powers down.

**Voltage Servo**

The voltage servo feature can be configured to trigger on under voltage and/or over voltage events, run continuously, or run just once. The LTC2970 relies on a simple linear search algorithm to find the IDAC code that results in an ADC input voltage that most closely corresponds to the servo target. The polarity of the servo algorithm can be programmed as inverting (default) or noninverting.

**Voltage Monitor**

The LTC2970 is able to perform ADC conversions on any combination of seven different input channels. Over-voltage and undervoltage threshold

*continued on page 46*

switching power supply applications without sense resistors, measure the load current via the DC resistance of the inductor using the application circuit shown in Figure 5.

The ADC inputs are also isolated from the LTC2970's internal supply. So the user can measure differential and common mode input voltages that are greater than  $V_{DD}$  without turning on body diodes, and no special precautions need to be taken if the LTC2970 loses power while monitoring DC/DC converter voltages powered from a different supply.

**Voltage Buffered IDACs**

Figure 6 illustrates how each of the LTC2970's continuous-time IDACs connects to a DC/DC converter with an external feedback network. The servo'd correction voltage is set by resistor  $R_{40}$ . Since  $R_{40}$  is terminated at the point-of-load ground, the correction voltage is insensitive to load induced ground bounce. The correction voltage is buffered to the  $V_{OUT0}$  pin by a unity-gain amplifier whose output can be placed in a low-leakage (<100nA), high impedance state. Resistor  $R_{30}$  connects the  $V_{OUT0}$  pin to the feedback node of the DC/DC converter. The range and resolution over which the correction voltage can

move the converter's output is adjustable via resistor  $R_{30}$ .

A "soft-connect" feature allows the LTC2970 to automatically find the  $V_{OUT0}$  voltage that most closely approximates the DC/DC converter's feedback node voltage before enabling the voltage buffer thus minimizing any

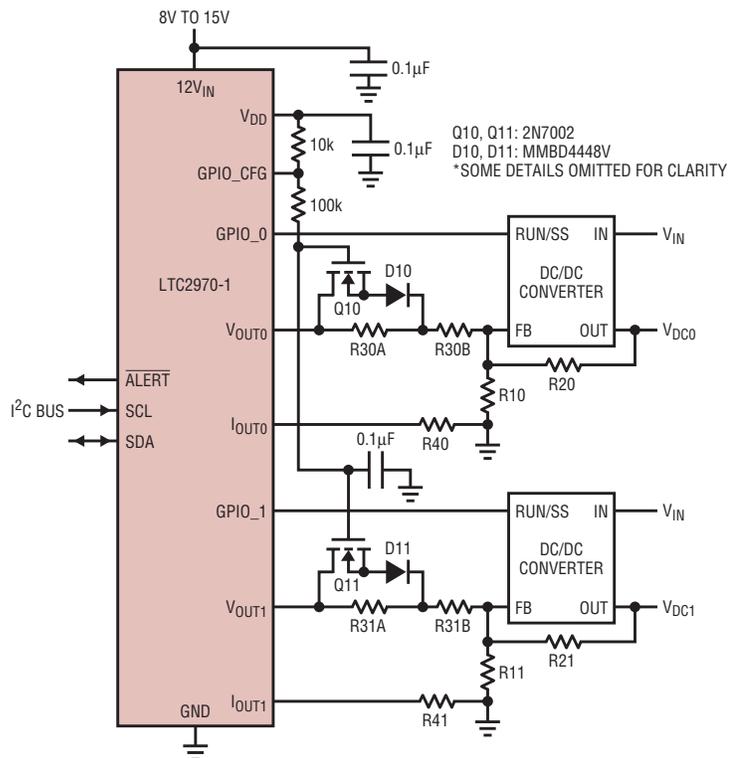


Figure 7. The LTC2970-1 enables supply tracking

# Cascadable, 7A Point-of-Load Monolithic Buck Converter

by Peter Guan

## Introduction

Easy-to-use and compact point-of-load power supplies are necessary in systems with widely distributed, high current, low voltage loads. The LTC3415 provides a compact, simple, complete and versatile solution. It includes a pair of integrated complementary power MOSFETs (32mΩ top and 25mΩ bottom) and requires no external sense resistor. A complete design involves choosing an inductor and input/output capacitors, and that's it. The result is a fast, constant frequency, current mode, 7A DC/DC switching regulator.

## Features

The overall solution is extremely compact since the LTC3415's QFN 5mm × 7mm package footprint is small while its high operating frequency of 1.5MHz allows the use of small low profile surface mount inductors and ceramic capacitors. For loads higher than 7A, multiple LTC3415s can be cascaded to share the load while running mutually antiphase, which reduces overall ripple at both the input and the output. Other features include:

- ❑ Spread spectrum operation to reduce system noise,
- ❑ Output tracking for controlled  $V_{OUT}$  ramp-up and ramp-down,
- ❑ Output margining for easy system stress testing,
- ❑ Burst Mode<sup>®</sup> operation to lower quiescent current and boost efficiency during low loads,
- ❑ Low shutdown current of less than 1μA,
- ❑ 100% duty-cycle for low drop out operation, phase-lock-loop to allow frequency synchronization of ±50%,
- ❑ Easily cascadable for multi-device load sharing with multiphase operation
- ❑ Internal or external  $I_{TH}$  compensation for either ease of use or loop optimization.

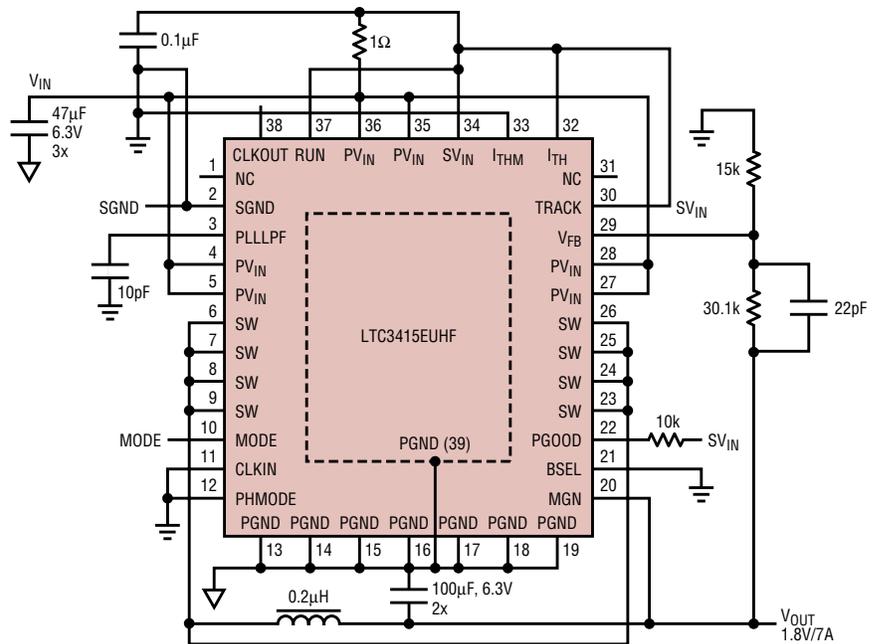


Figure 1. Typical application of the LTC3415 in a 3.3V to 1.8V/7A step down converter

## Operation

Figure 1 shows a typical application of the LTC3415 in a 3.3V to 1.8V/7A step down converter. Figure 2 shows its efficiency and power loss vs load current. Figure 3 shows its transient response to a 5A load.

The LTC3415 uses a constant frequency, current mode architecture to drive an integrated pair of complementary power MOSFETs. An internal oscillator sets the 1.5MHz operating

frequency of the device. The main P-channel power MOSFET turns on with every oscillator cycle and turns off when the internal current comparator trips, indicating that the inductor current has reached a level set by the  $I_{TH}$  pin. An internal error amplifier, in turn, drives the  $I_{TH}$  pin by monitoring the output voltage through an external resistive divider connected to the VFB pin. While the P-channel power MOSFET is off, the internal synchronous N-channel power MOSFET turns on until either the inductor current

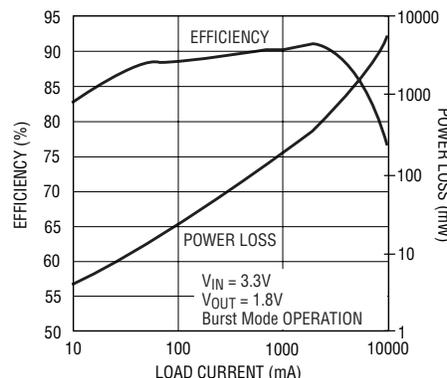


Figure 2. Efficiency and power loss vs load current for the circuit in Figure 1

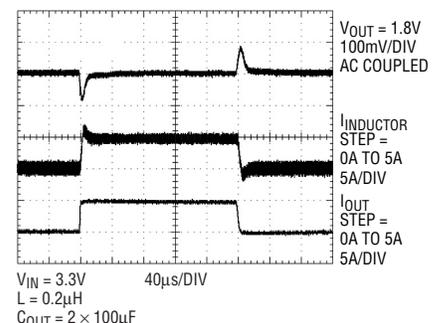


Figure 3. Transient response to a 5A load for the circuit in Figure 1

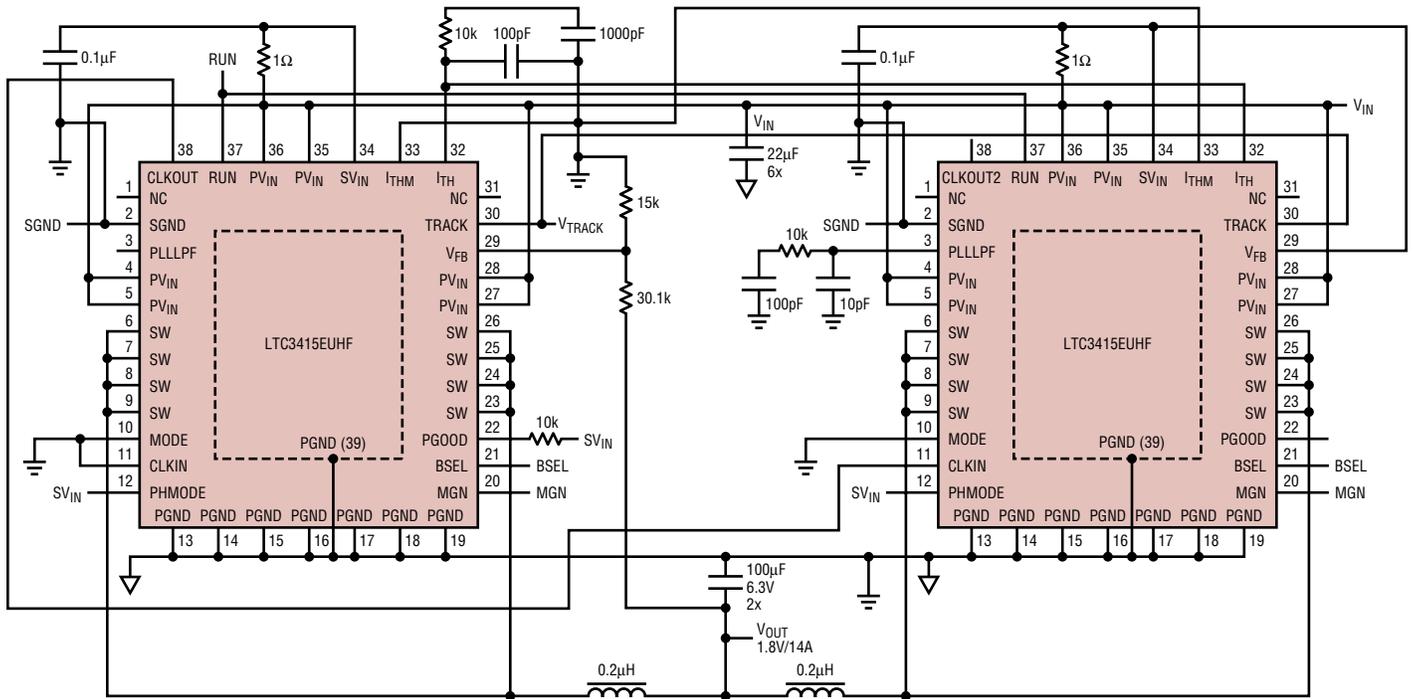


Figure 4. Dual-phase single output 3.3V to 1.8V 15A application using two LTC3415s running 180° out of phase with respect to each other.

starts to reverse, as indicated by the SW pins going below ground, or until the beginning of the next cycle.

**Modes of Operation:  
Burst, Pulse-Skip, and  
Forced Continuous**

Three modes of operation can be selected through the MODE pin. Tying it to  $V_{IN}$  enables Burst Mode operation for highest efficiency. During low output loads, the peak inductor current limit is clamped to about a quarter of the maximum value and the  $I_{TH}$  pin is monitored to determine whether the device will go into a power-saving Sleep mode. Quiescent current is reduced to 450µA in Burst Mode operation because most of the internal circuitry is turned off.

For applications that aim to reduce output ripple and strive to maximize operating time at constant frequency, pulse-skip mode is a good solution. Pulse-skip mode is enabled by letting the Mode pin float or tying it to  $V_{IN}/2$  or  $V_{OUT}$ . Inductor current is still not allowed to reverse as in Burst Mode operation, but the peak inductor current limit is no longer clamped internally.  $I_{TH}$  has full control of output current until  $I_{TH}$  drops so low (at low output

loads) that minimum on-time of the device is reached and the LTC3415 begins to skip cycles.

For applications that require constant frequency operation even at no load, the LTC3415 can be put into forced continuous mode operation by tying the Mode pin to ground. In this mode, inductor current is allowed to reverse while the internal power MOSFETs are always driven at the same frequency.

**Output Tracking**

For applications that require controlled output voltage tracking between

their various outputs in order to prevent excessive current draw or even latch-up during turn-on and turn-off, the LTC3415 includes a Track pin that allows the user to program how its output voltage ramps during start-up and shutdown. During start-up, if the voltage on the Track pin is less than 0.57V, the feedback voltage regulates to this tracking voltage, thus programming the output voltage to follow along. Inductor current is not allowed to reverse during tracking, ensuring monotonic voltage rise. When the tracking voltage exceeds 0.57V, tracking is disabled and the feedback voltage regulates to the internal reference voltage (0.596V). In other words, output voltage is controlled by the Track voltage until the output is in regulation.

Taking the LTC3415's Run pin to below 1.5V would normally shut down the part, but if the output also needs tracking during shutdown, then the LTC3415 must remain active even if the Run pin is low. So, during shutdown, if Track is 0.5V or more below  $SV_{IN}$ , then even if Run is low, the LTC3415 will not shutdown until Track has fallen below 0.18V, thus allowing the output to properly

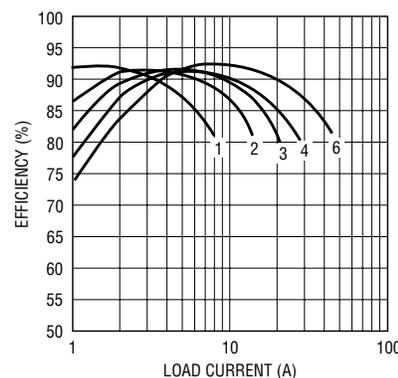
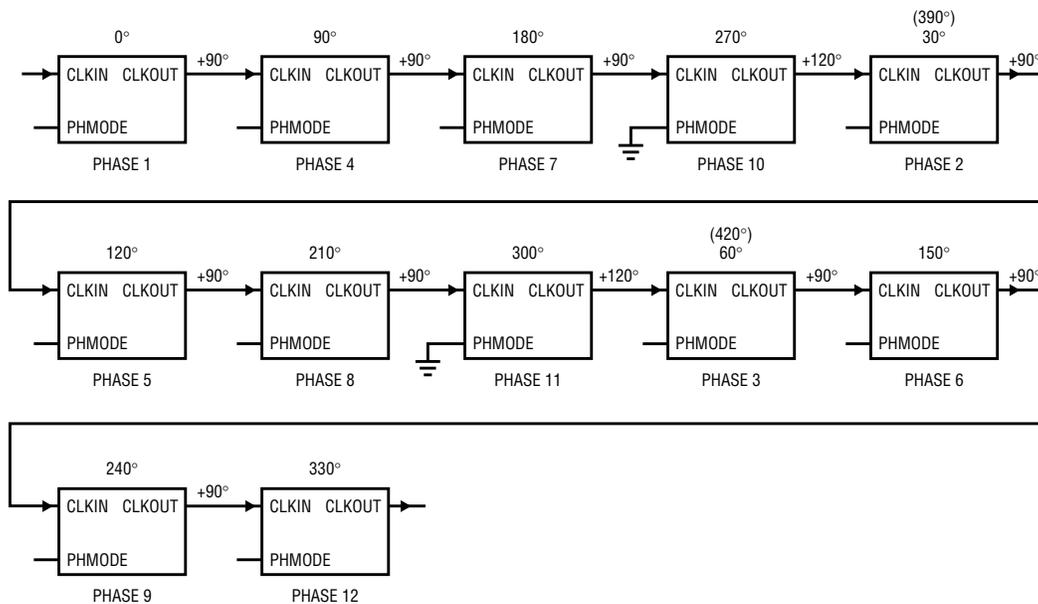


Figure 5. Combined efficiency of load-sharing in 1-phase, 2-phase, 3-phase, 4-phase, and 6-phase operation.



**Figure 6. Cascaded, 12-phase operation makes for efficient high current load sharing**

track the master voltage during its ramp-down. For applications that do not require tracking or externally controlled soft start, simply tie the Track pin to  $SV_{IN}$ .

### Output Margining

For convenient and accurate system stress test on the LTC3415's output, the user can program the LTC3415's output to  $\pm 5\%$ ,  $\pm 10\%$ , and  $\pm 15\%$  of its nominal operational voltage. The MGN pin, when left floating, forces normal operation. When MGN is tied to GND, it forces negative margining, in which the output voltage is below the regulation point. When MGN is tied to  $SV_{IN}$ , then the output voltage is forced to above the regulation point. The amount of output voltage margining is determined by the BSEL pin. When BSEL is low, it's 5%. When BSEL is high, it's 10%. When BSEL is left floating, margin percentage is 15%. To prevent system glitches while margining, the internal output overvoltage and undervoltage comparators are disabled and thus PGOOD remains pulled high by the external resistor.

### Multiphase Operation

For output loads that demand more than 7A of current, multiple LTC3415s can be cascaded to run out of phase while equally sharing output load

current. Figure 4 shows a dual-phase single output 3.3V to 1.8V 14A application using two LTC3415s running 180° out of phase with respect to each other. Figure 5 shows the combined efficiency of 1-phase, 2-phase, 3-phase, 4-phase, and 6-phase operation.

The CLKIN pin allows the LTC3415 to synchronize to an external frequency (between 0.75Mhz and 2.25Mhz) and the internal phase-lock-loop allows the LTC3415 to lock on to CLKIN's phase as well. The CLKOUT signal can be connected to the CLKIN pin of the following LTC3415 stage to line up both the frequency and the phase of the entire system. Tying the PHMODE pin to  $SV_{IN}$ , SGND, or  $SV_{IN}/2$  (floating) respectively generates a phase difference (between CLKIN and CLKOUT) of 180°, 120°, or 90°, which respectively corresponds to 2-phase, 3-phase, or 4-phase operation. A total of 12 phases can be programmed by setting the PHMODE pin of each phase to different levels. For instance, a slave stage that's 180° out of phase from the master can generate a 120° CLKOUT signal that's 300° (PHMODE = SGND) away from the master for the next stage, which then can generate a CLKOUT signal that's 420°, or 60° (PHMODE =  $SV_{IN}/2$ ) away from the master for its following stage. See Figure 6.

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is divided by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by, and the effective ripple frequency is increased by, the number of phases used.

### Output Current Sharing

When multiple LTC3415s are cascaded to drive a common load, accurate output current sharing is essential to achieve optimal performance and efficiency. Otherwise, if one stage is delivering more current than another, then the temperature between the two stages is different, and that can translate into higher switch  $R_{DS(ON)}$ , lower efficiency, and higher RMS ripple. Each LTC3415 has a trimmed peak current limit such that when the  $I_{TH}$  pins of multiple LTC3415s are tied together, the amount of output current delivered from each LTC3415 is nearly the same.

Different ground potentials among LTC3415 stages, caused by physical distances and switching noises, could cause an offset to the absolute  $I_{TH}$  value

seen by each stage. To ensure that the ground level doesn't affect the  $I_{TH}$  value, the LTC3415 uses a differential amplifier that takes as input not just the  $I_{TH}$  pin, but also the  $I_{THM}$  pin, which doesn't connect to any other circuitry except for the  $I_{TH}$  differential amplifier. Therefore, the  $I_{THM}$  pins of all the LTC3415 stages should be tied together and then connected to the SGND pin at only one point.

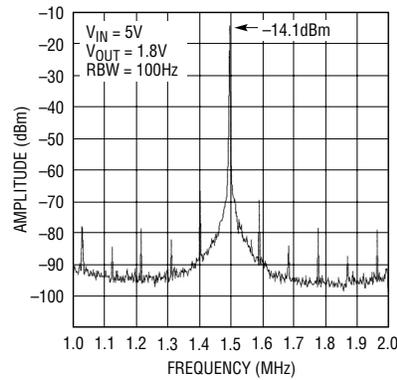
### Internal/External $I_{TH}$ Compensation

During single phase operation, the user can simplify the compensation of the internal error amplifier loop (on the  $I_{TH}$  pin) by tying it to  $SV_{IN}$  to enable internal compensation, which connects an internal 50k resistor in series with a 50pF cap to the internal  $I_{TH}$  compensation point. This is a trade-off for simplicity and ease of use at the expense of OPTI-LOOP<sup>®</sup> optimization, where external  $I_{TH}$  components can be selected to optimize the loop transient response with minimum output capacitance.

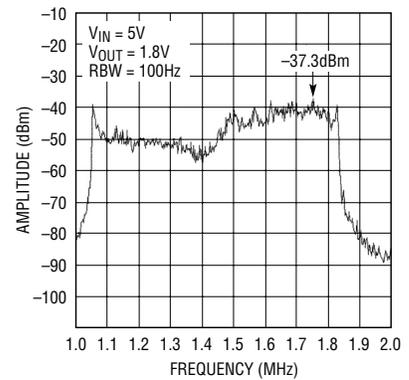
In multi-phase operation where all the  $I_{TH}$  pins of each phase are tied together to achieve accurate load sharing, internal  $I_{TH}$  compensation is disabled and external compensation components need to be properly selected for optimal transient response and stable operation.

### Master/Slave Operation

In multiphase single-output operation, the user has the option to run in multi-master mode where all the FB,  $I_{TH}$ , and output pins of the stages are tied to each other. All the error amplifiers are effectively operating in parallel and the total transconductance ( $g_m$ ) of the system is increased by the number of stages. The  $I_{TH}$  value, which dictates how much current is delivered to the load from each stage, is averaged and smoothed out by the external  $I_{TH}$  compensation components. Nevertheless, in certain applications, the resulting higher  $g_m$  from multiple 3415s can make the system loop harder to compensate; in this case, the user can choose an alternative mode of operation.



a. The LTC3415's output noise spectrum analysis in free-running constant frequency operation



b. The LTC3415's output noise spectrum analysis in spread spectrum operation

Figure 7. Spread spectrum operation reduces EMI peaks by spreading the EMI energy over a range of frequencies

The second mode of operation is single-master operation where only the error amplifier of the master stage is used while the error amplifiers of the other stages (slaves) are disabled. The slave's error amplifier is disabled by tying its FB pin to  $SV_{IN}$ , which also disables the internal overvoltage comparator and power-good indicator. The master's error amplifier senses the output through its FB pin and drives the  $I_{TH}$  pins of all the stages. To account for ground voltage differences among the stages, the user should tie all  $I_{THM}$  pins together and then tie it to the master's signal ground. As a result, not only is it easier to do loop compensation, this single-master operation should also provide for more accurate current sharing among stages because it prevents the error amplifier's output ( $I_{TH}$ ) of each stage from interfering with that of another stage.

### Spread Spectrum Operation

Switching regulators can be troublesome where electromagnetic interference (EMI) is a concern. Switching regulators operate on a cycle-by-cycle basis to transfer power to an output. In most cases, the frequency of operation is fixed or is a constant based on the output load. This method of conversion creates large components of noise at the frequency of operation (fundamental) and multiples of the operating frequency (harmonics).

To reduce this noise, the LTC3415 can run in spread spectrum operation by tying the CLKIN pin to  $SV_{IN}$ . In spread spectrum operation, the LTC3415's internal oscillator is designed to produce a clock pulse whose period is random on a cycle-by-cycle basis but fixed between 60% and 140% of the nominal frequency. This has the benefit of spreading the switching noise over a range of frequencies, thus significantly reducing the peak noise. Figures 7 and 8 show how the spread spectrum feature of the LTC3415 significantly reduces the peak harmonic noise vs free-running constant frequency operation. Spread spectrum operation is disabled if CLKIN is tied to ground or if it's driven by an external frequency synchronization signal.

### Conclusion

With its many operational features and compact total solution size, the LTC3415 is an ideal fit for today's point-of-load power supplies. It also has the advantage of simple upgradability: if the load requirement of a power supply increases, no need to dread the redesign of the whole system, just stack on another LTC3415 and keep going. 



# I<sup>2</sup>C Bus Buffer Resolves Stuck Buses, Eliminates Heavy Load Limitations and Provides Level Translation

by George Humphrey

## Introduction

The I<sup>2</sup>C bus is a 2-wire bidirectional communications bus primarily used for system configuration and monitoring. A bus master, typically a microcontroller unit (MCU), polls system components for information such as supply voltage and temperature, Vital Product Data (VPD) from memories on removable cards, and system configuration. The master can also use the bus to reconfigure the system through general purpose

input/output ports (GPIOs) and other programmable devices. Large-scale telecommunication and data storage systems are divided up into several peripheral cards. Each card plugs on to the I<sup>2</sup>C bus and communicates its system information to the MCU through the back plane.

Certain considerations must be addressed to ensure a high level of reliability when designing a system using the I<sup>2</sup>C bus. Primarily, systems must

provide protection against a hung or stuck bus. If for any reason the bus is stuck low, there is the potential to bring the entire system down. Another consideration is dealing with heavy capacitive loads on the bus. The I<sup>2</sup>C standard specifies a 400pF limit on the bus. With systems becoming larger, this specification becomes problematic because of so many devices connected directly to the bus. Systems also need to be robust, allowing cards to

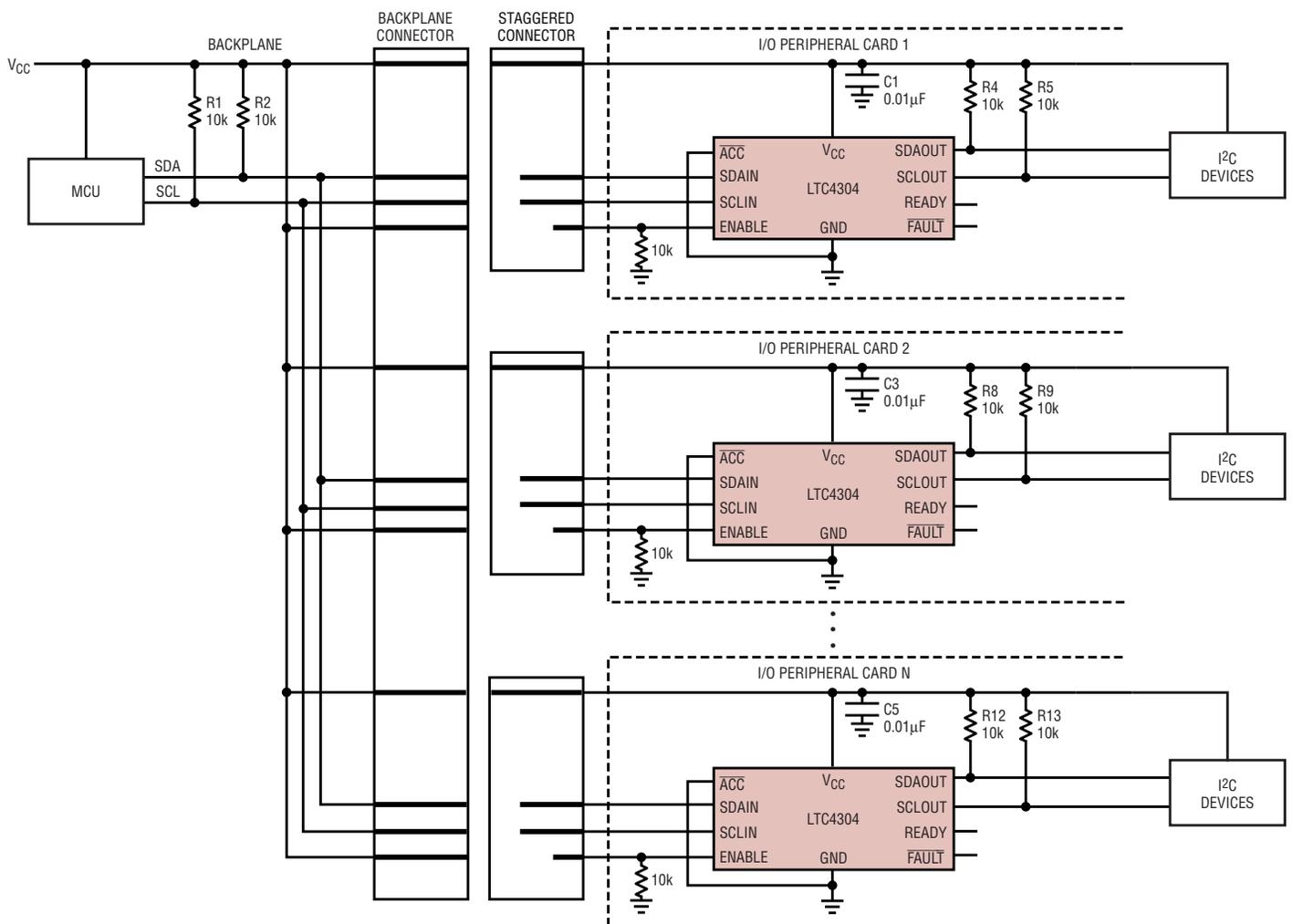


Figure 1. Typical application of the LTC4304

be inserted or removed from a live backplane without corruption of the I<sup>2</sup>C bus data. Finally, cards must be immune to ESD events that can occur from human handling.

The LTC4304 is a multifunctional device. It has a flexible architecture that allows it to be configured into almost any system. The LTC4304 features proprietary stuck bus protection circuitry that unburdens the MCU from the tasks of monitoring, troubleshooting and resolving stuck buses. Simplifying this task also saves PCB board space and connector pins. The LTC4304 provides bidirectional capacitance buffering, isolating the card bus from the backplane bus. Rise time accelerators help heavily capacitive-loaded buses meet I<sup>2</sup>C rise time specifications. The LTC4304 also enables cards to be inserted or removed from the system without corrupting the data on the I<sup>2</sup>C bus. Built-in ±15kV of human Body Model ESD protection provides a rugged front end for cards that typically have the SDA and SCL lines connected directly to the card connector.

## Circuit Operation

### Startup and Hot Swap

To take full advantage of the LTC4304's Hot Swap features, a staggered connector must be used: where V<sub>CC</sub> and GND are the longest pins, SDA and SCL pins medium length and ENABLE the shortest. After the card's V<sub>CC</sub> and GND connect with the live backplane, the voltage on V<sub>CC</sub> starts to rise. At this time, the LTC4304's precharge circuitry charges the capacitance on the SDA and SCL lines to 1V. Precharged SDA/SCL lines minimize disturbances on the bus when they connect to the backplane. The remainder of the LTC4304's circuitry is disabled until the supply voltage rises above 2.5V (typical) and the voltage on ENABLE is above 1.4V (typical). Making ENABLE the shortest pin insures that SCL and SDA are firmly seated before a connection is established on the bus. When the V<sub>CC</sub> supply to the LTC4304 is valid, it assumes that the card is connected to a live backplane and looks

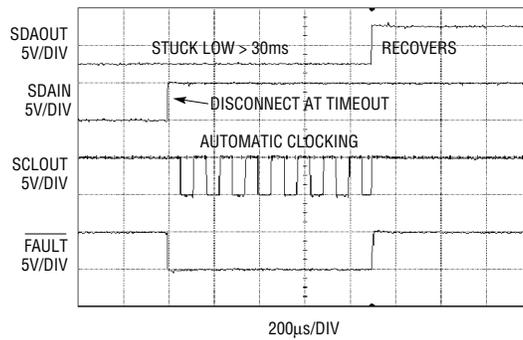


Figure 2. Stuck bus resolved with automatic clocking

for either a stop bit or a bus idle on the backplane side on SDAIN and SCLIN. When one of these conditions is met and SDAOUT and SCLOUT are high, the connection circuitry is activated, connecting the card side bus with the backplane bus. These requirements ensure that the data on the bus is not corrupted when the card is plugged in. READY indicates the status of the connection circuitry and is high when the connection circuitry is active.

### Bus Stuck Low Timeout

The LTC4304 monitors SDAOUT and SCLOUT on the card side of the I<sup>2</sup>C bus. When SDAOUT or SCLOUT is low, an internal timer is started, only to be reset when SDAOUT and SCLOUT are both high. If SDAOUT or SCLOUT do not go high within 30ms, the connection between the inputs and outputs is automatically disconnected, and FAULT asserts low indicating a stuck bus. The LTC4304 also detects a fault if powered up into a stuck bus condition. In either case, the LTC4304 automatically generates up to 16 clock pulses at 8.5kHz on SCLOUT. If SDAOUT and SCLOUT go high, FAULT releases and is pulled high. The LTC4304 then looks for a stop bit or a bus idle before automatically reconnecting. While there is a stuck bus condition, a connection can be forced with a rising edge on ENABLE, even if bus idle conditions are not met.

### Capacitance Buffering

The connection circuitry contains a unique patent-pending architecture that provides electrical isolation, isolating the capacitance on the card side bus from the backplane side bus,

while maintaining full I<sup>2</sup>C functionality. This means that the MCU only sees the capacitance of the backplane and the low input capacitance of the LTC4304, <10pF guaranteed by design. The LTC4304 drives the capacitance of the circuitry on the card side. The LTC4304 regulates the voltage on the opposite side from which it is being driven to a slightly higher voltage. This voltage (call it V<sub>OS</sub>) is a function of V<sub>CC</sub>, the pull-up resistor, and an internally set constant terms given by the equation:

$$V_{OS} = \frac{V_{CC}}{R_{PULLUP}} \cdot 20 + 75mV$$

For example: For a 2.7kΩ pull-up and a V<sub>CC</sub> of 3.3V,

$$V_{OS} = \frac{3.3mV}{2.7k\Omega} \cdot 20 + 75mV = 99.4mV$$

### Rise Time Accelerators

Rise-time accelerators are included on all four SDA and SCL pins. Once activated, the accelerators switch in 3.5mA of current (typical at V<sub>CC</sub>=2.7V) into the SDA and SCL lines to make them rise faster. This ensures that rise-time requirements are met and allows the use of larger pull-up resistors to reduce power consumption. When ACC is connected to ground, all four accelerators are ON. When ACC is connected to V<sub>CC</sub>, all four accelerators are OFF. And when ACC is floating, only the accelerators on SDAOUT and SCLOUT are activated. Accelerators cannot be used on pins where the pull-up voltage is less than V<sub>CC</sub>. The flexibility of the accelerators control provided by ACC allows the LTC4304

to interface with buses not common with its supply.

**Applications**

**Stuck Bus Automatically Resolved Independent of the MCU**

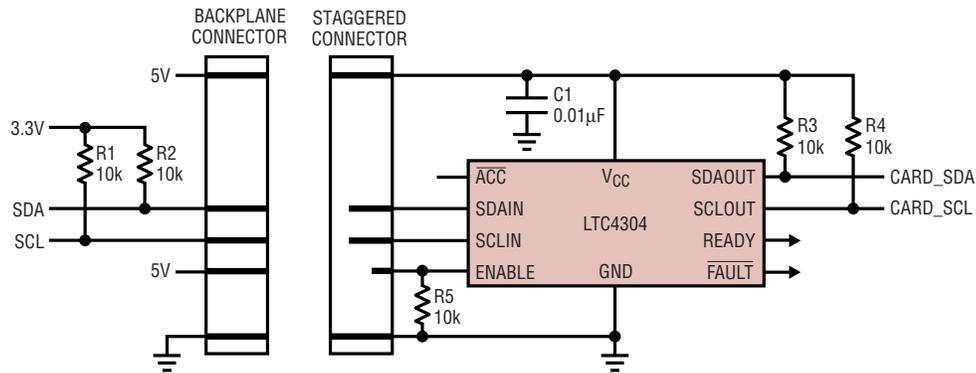
The I<sup>2</sup>C bus protocol calls for bidirectional communication between devices. A typical example is a microcontroller unit (or MCU) communicating with a slave device. As the slave device's internal register is read

by the MCU, the MCU clocks the slave device to receive each bit of data. A problem occurs when the MCU is out of sync with the slave device—the slave device is waiting for another clock and the MCU thinks it has already sent out enough clocks. If the slave device happens to be holding the data line low, all further communications are prevented and the I<sup>2</sup>C bus is stuck.

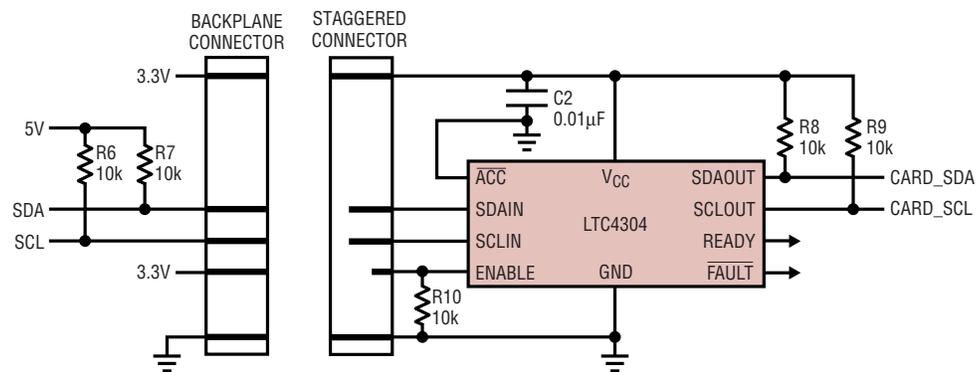
Figure 1 shows a card with a resident LTC4304 that acts as the interface between the devices on the

card and the I<sup>2</sup>C bus, when the card is plugged into the backplane. In normal, plugged-in operation, a connection is established between SDAIN and SDAOUT, and SCLIN and SCLOUT. Internal comparators monitor the SDAOUT and SCLOUT nodes of the circuit. When SDAOUT or SCLOUT is low, an internal timer starts. The timer is only reset when SDAOUT and SCLOUT are both high. If they don't go high within 30ms, it is determined that the bus is stuck low and the con-

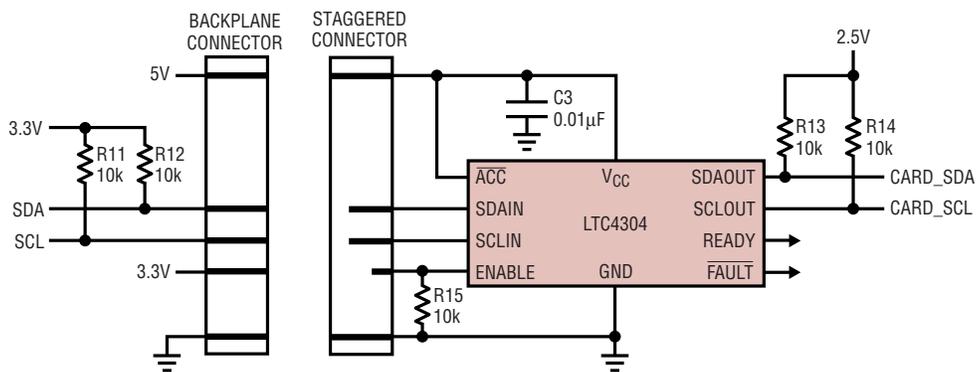
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**a.  $V_{CC}$  is higher than the pull-up voltage on SDAIN and SCLIN.**



**b.  $V_{CC}$  is equal to the output side pull-up voltage, and less than input side pull-up voltage.**



**c.  $V_{CC}$  is greater than the pull-up voltages of both sides.**

**Figure 3. The LTC4304 can be the bridge between a backplane operating at one voltage and a card operating at a different voltage. Here are three possible scenarios and appropriate configurations.**

# Negative Voltage Hot Swap Controller with 10-Bit ADC and I<sup>2</sup>C Monitoring

by Zhizhong Hou

## Introduction

High availability –48V power systems, such as telecom and AdvancedTCA systems, allow for circuit board upgrade and replacement on a live powered backplane. The primary role of a Hot Swap controller is to make this possible by limiting potentially large inrush currents, which can cause damage to the hot swapped board or create disturbances on the backplane. Traditionally, –48V Hot Swap controllers operate autonomously—the Hot Swap controller shuts down an abnormally operating board before the host processor knows why. This simplifies system design, but gives little in the way of diagnostic support to the host.

A far more robust system would use the Hot Swap controller to communicate the conditions of the board to the host processor, and let the host processor take action. To this end, the LTC4261 integrates a –48V Hot Swap controller, 10-bit ADC monitoring and I<sup>2</sup>C/SMBus communication. It monitors the real-time board parameters such as current and voltages and communicates the data to the host.

## Features

Figure 1 shows a simplified block diagram of the LTC4261. Power is derived from the –48V RTN using an external dropping resistor connected to the V<sub>IN</sub> pin. An internal shunt regulator clamps the voltage at V<sub>IN</sub> to 11.2V above V<sub>EE</sub> (chip ground). This floating architecture allows a wide operating voltage range. The device also provides a 5V linear-regulated voltage at the INTV<sub>CC</sub> pin that can source current up to 20mA for driving external circuits.

Using an external N-channel pass transistor, the negative Hot Swap circuit of the LTC4261 allows a board to be safely inserted and removed from a live –48V backplane. The device features a new inrush control technique

that minimizes stresses on the pass transistor in all operating conditions. Turning the device on or off can be either autonomous or controlled by a host processor through the I<sup>2</sup>C interface. Auto-retry following a fault is programmable and fully controlled by the host. Configurations of the device are stored in the internal registers as shown in Table 1.

The LTC4261 continuously monitors and registers board status and fault conditions. With an onboard 10-bit ADC and 3-channel multiplexer, it accurately measures real-time board current (through the voltage across the sense resistor) and two external voltages. The data are stored in the ADC registers (see Table 1). When polled by a host processor, the LTC4261 reports the ADC data along with the status and fault information using the I<sup>2</sup>C interface. The real-time board current and voltages provides a means for the host to detect any early warn-

ing signal and to flag the board for maintenance before it fails. With the  $\overline{\text{ALERT}}$  pin, the LTC4261 interrupts the host for specific fault conditions, when configured to do so.

One unique feature of the LTC4261 is that the I<sup>2</sup>C interface can be easily configured using the address pins (ADR1 and ADR0) into a single-wire broadcast mode that only uses a single I<sup>2</sup>C signal, SDAO, to report the ADC data and fault information. This mode simplifies the interface and saves component cost by eliminating two optoisolators.

The LTC4261 has additional features to sequence two power good outputs, detect insertion of a board and turn off the pass transistor if an external supply monitor fails to indicate power good within a timeout period. Using the PGIO and  $\overline{\text{FLTIN}}$  pins along with the ADC, the device can detect a specific fuse that is open for up to four fuses.

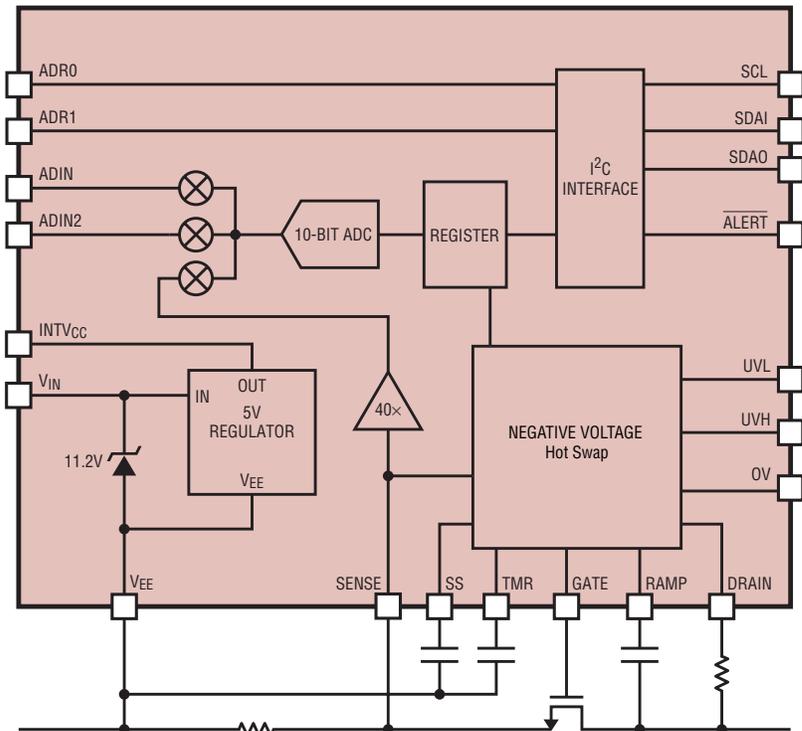
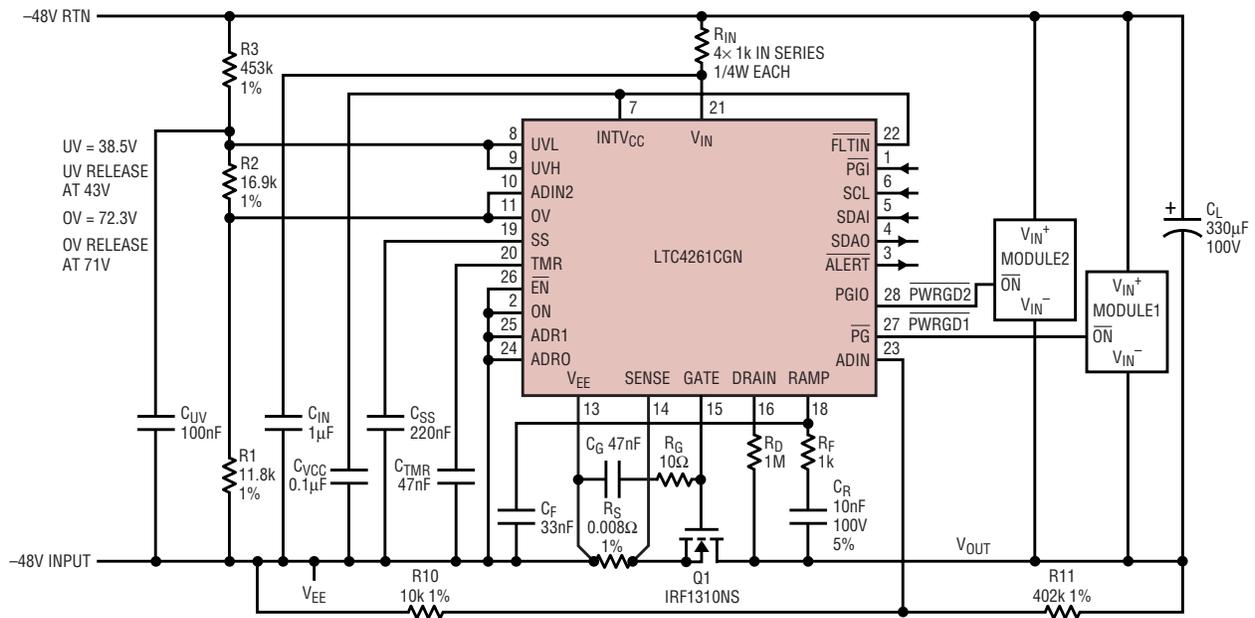


Figure 1. Simplified block diagram of LTC4261



**Figure 2. A -48V/200W Hot Swap controller (5.6A current limit, 0.66A inrush) using LTC4261 with current, input voltage and  $V_{DS}$  monitoring**

**10-Bit ADC Provides Accurate Measurement of Real-Time Board Current and Voltages**

Quantitative monitoring of real-time board level voltage and current (and thus power) provides significant benefits in high availability systems. Real time operating data can be compared to budgeted or historical data to detect whether a circuit board is using its allotted power or if is operating abnormally. By issuing early warning to system management, an abnormally operating board can be flagged for

service even before it fails. This feature greatly improves the reliability of high availability systems.

The LTC4261 includes a 10-bit ADC that accurately measure voltages at the SENSE, ADIN2 and ADIN pins, all referred to chip ground ( $V_{EE}$ ). With a 2.56V full scale and 2.5mV resolution, the ADIN and ADIN2 pins are uncommitted inputs that allow monitoring of any external voltages. With the sense resistor, the SENSE pin voltage is used to measure current flowing through the pass transistor. This voltage is

internally amplified by 40 times resulting in a 64mV full scale and 62.5µV resolution. The digital codes of the three voltages after each conversion are stored in corresponding ADC registers (see Table 1) and updated at a frequency of 7.3Hz. Setting the test mode bit in the CONTROL register halts the updating so that software testing can be performed by writing to and reading from the registers.

An example of using the ADC monitoring is shown in Figure 2, where current, input voltage and  $V_{DS}$  of the pass transistor are measured at the SENSE, ADIN2 and ADIN pins, respectively. The latter two voltages can be used to derive the output voltage referred to RTN. Another application of the ADC monitoring is to detect an open fuse in a multi-feed system, which is detailed later in this article.

**Independently Adjustable Inrush and Overcurrent Limits Minimize Stress on Pass Transistor**

A typical -48V/200W Hot Swap application using the LTC4261 is shown in Figure 2. Initial turn-on of pass transistor Q1 is autonomous but I<sup>2</sup>C can take over the control after power-up. To protect the pass transistor from overstress, the LTC4261 independently controls inrush current

**Table 1. LTC4261 registers**

| Register | Read/ Write | Description  |
|----------|-------------|--|
| STATUS   | R           | Provides pass transistor (on/off), $\overline{EN}$ (high/low) and PGIO input conditions. Also lists five fault present conditions.   |
| FAULT    | R/W         | Latches overcurrent, overvoltage, undervoltage, power bad, FETshort faults and $\overline{EN}$ changed state. Also logs FLTIN and PGIO inputs.                             |
| ALERT    | R/W         | Enables which faults interrupt the host using the ALERT pin. Defaults not to alert on faults at power-up.  |
| CONTROL  | R/W         | Controls on or off of the pass transistor and whether the part auto-retries or latches off after a fault. Also configures the PGIO pin and enables ADC register test mode. |
| SENSE    | R/W         | ADC data for the SENSE voltage measurement   |
| ADIN2/OV | R/W         | ADC data for the ADIN2 (on TSSOP) or OV (on QFN) pin voltage measurement   |
| ADIN     | R/W         | ADC data for the ADIN pin voltage measurement  |

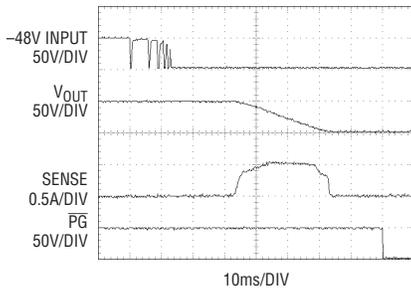


Figure 3. The LTC4261 start-up behavior

during power-up and overcurrent upon a short circuit. As indicated in Figure 2, the current limit and circuit breaker threshold is set to 5.6A by the sense resistor  $R_S$ , while the inrush is set to a much lower level (0.66A) by controlling the ramp rate of  $V_{OUT}$  with an external capacitor  $C_R$  connected between  $V_{OUT}$  and the RAMP pin. The operation theory and the benefits of this inrush and overcurrent control technique are demonstrated below.

Following a start-up debounce delay, the turn-on sequence of the LTC4261 starts with charging the SS pin up with a  $10\mu A$  current. The SS voltage ( $V_{SS}$ ) is converted to a GATE pull-up current. When the GATE voltage reaches the threshold voltage of the pass transistor  $Q1$ , the inrush starts to flow through  $Q1$ . The output voltage ( $V_{OUT}$ ) begins to move and  $C_R$  begins to

charge. This draws a current from the RAMP pin that flows through  $C_R$  and causes the GATE current to drop to 0. The RAMP pin is regulated at 1.1V so the inrush is set by the ramp rate of  $V_{OUT}$ , which leads to:

$$I_{INRUSH} = 20\mu A \frac{C_L}{C_R}$$

The slew rate of  $V_{SS}$  determines  $di/dt$  of the inrush current. Figure 3 shows the start-up behavior of the LTC4261.

The LTC4261 provides 2-level overcurrent protection: an active current limit (ACL) amplifier that also serves as a circuit breaker comparator with a threshold of  $50mV \pm 10\%$ , and a fast pull down comparator with a threshold of 150mV. In the event of an output short or a fast input step, when  $V_{SENSE}$  exceeds 150mV, the fast pull down comparator immediately brings the GATE down with a 110mA current. Once  $V_{SENSE}$  falls back below 150mV, the ACL starts to servo the GATE and maintains a constant output current of  $50mV/R_S$ . If the short-circuit condition lasts longer than the circuit breaker delay of  $530\mu s$ , the pass transistor is turned off and an overcurrent fault is registered. The device defaults to latch off upon an overcurrent fault but can

be configured to automatically re-try after a cooling delay. Figure 4 illustrates the response of the LTC4261 to the short-circuit condition. In the case of an input step, the inrush control circuit takes over following the fast GATE pull-down and the current limit loop is disengaged before the circuit breaker timer expires. The device then operates similarly to the start-up, only with a difference that the current through the pass transistor is now a sum of inrush and load current.

By decoupling start-up inrush from the current limit/circuit breaker threshold, the LTC4261 makes it possible to optimize the safe operating area (SOA) of the pass transistor in all operating conditions. The short circuit breaker timer substantially reduces the stress on the pass transistor in a short-circuit condition. Startup and input step typically impose the greatest stress on the pass transistor. Setting the inrush current much smaller than the current limit relieves the SOA requirement during start-up and input step. This allows using smaller pass transistors for large load applications, making selection of pass transistors much easier. Using the dedicated RAMP pin that is regulated separately from GATE

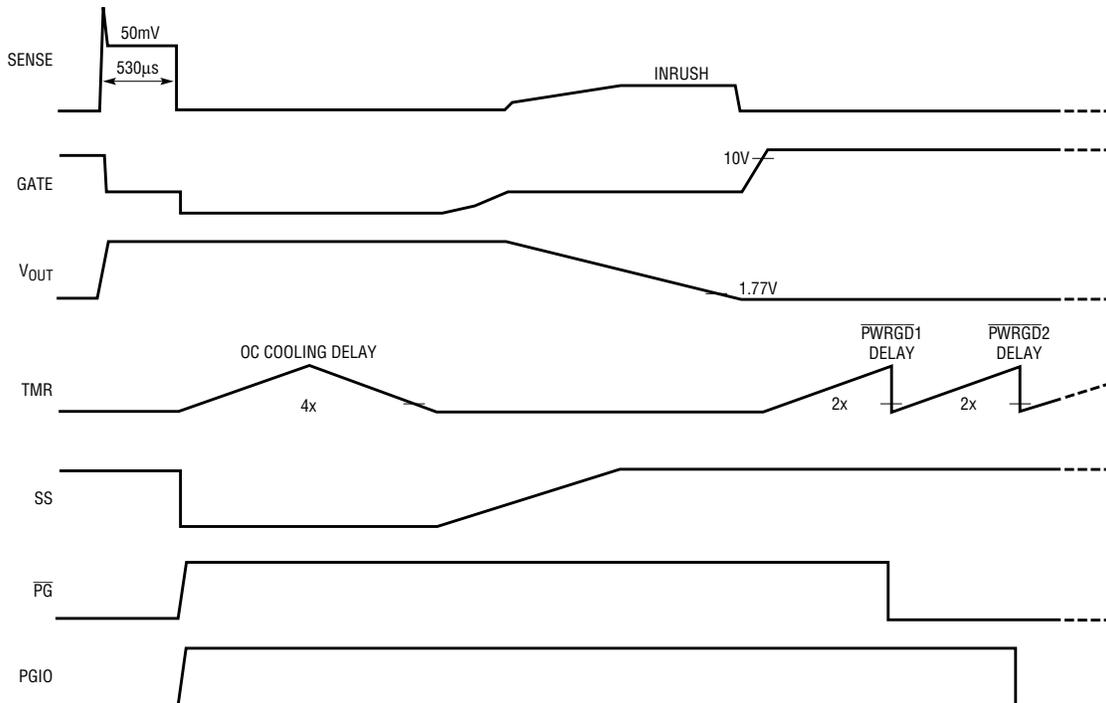


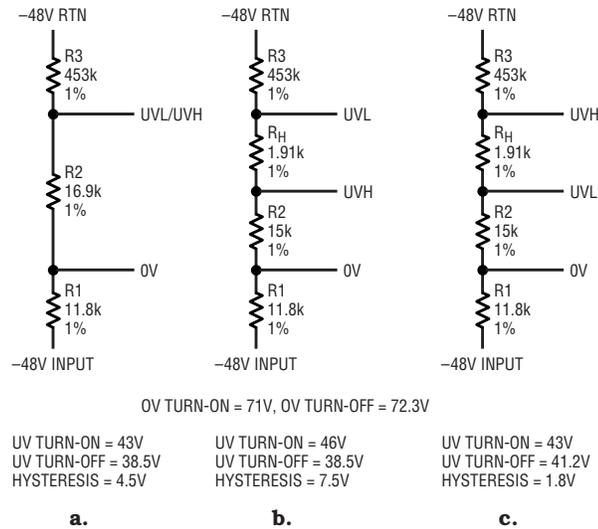
Figure 4. Response of the LTC4261 to overcurrent fault in auto-retry mode

for inrush control, the LTC4261 does not require a large capacitor between GATE and  $V_{EE}$  that relates to  $C_R$ , so the turn-off of the pass transistor upon short-circuit can be fast even for large load applications.

**Adjustable Undervoltage Comparator Offers Both Precision and Flexibility**

The LTC4261 provides two UV pins (UVH and UVL) that can be used to precisely set the undervoltage threshold and hysteresis. Each of the two pins has an accurate threshold: 2.56V for UVH rising (turn-on) and 2.291V for UVL falling (turn-off), and both pins have a small, built-in hysteresis of 15mV. With either a rising or falling input voltage, both the UVH and UVL pins have to cross their thresholds for the comparator output to change state. If both pins fall below their thresholds, an undervoltage fault is registered.

The ratio between the UVH and the UVL thresholds is designed to precisely set 43V turn-on and 38.5V turn-off UV thresholds popular in telecom applications with minimum external components, by tying UVH and UVL together. Along with the OV pin (with a threshold of 1.77V and a hysteresis of 37.5mV), the 3-resistor divider shown in Figure 5a sets an accurate operating range of 43V to



**Figure 5. Adjustment of undervoltage thresholds and hysteresis**

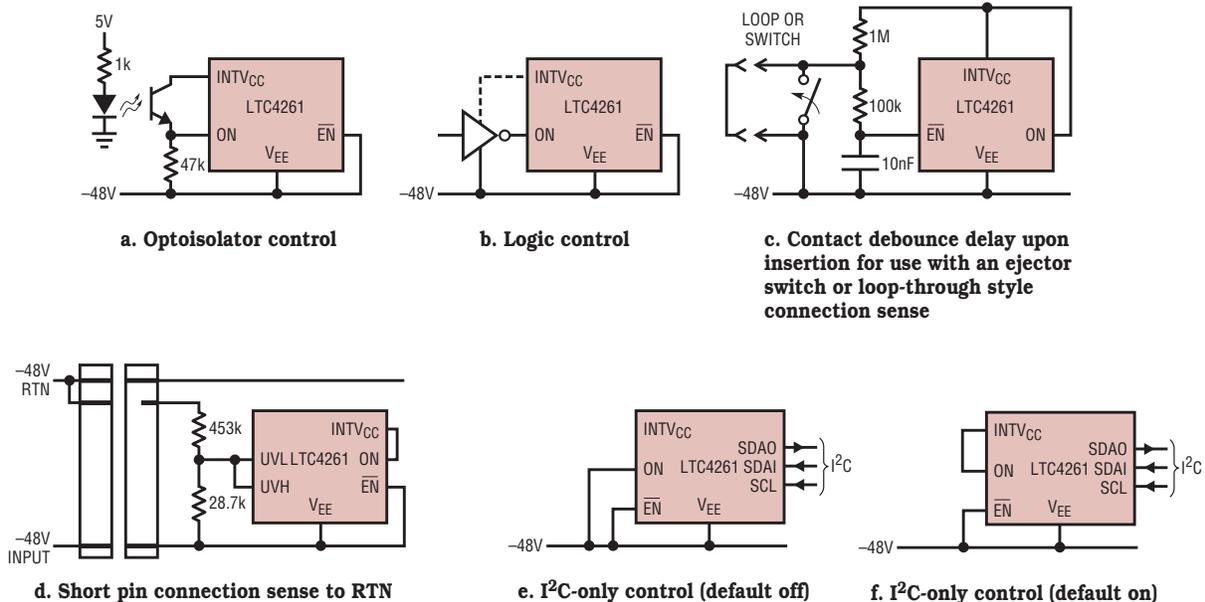
71V with UV turn-off at 38.5V and OV turn-off at 72.3V.

The UV levels can be adjusted by connecting a resistor  $R_H$  between the UVH and UVL pins, as illustrated in Figure 5b (UVL tap above UVH tap for a larger hysteresis) and Figure 5c (UVL tap below UVH tap for a smaller hysteresis). In the latter case, the LTC4261 does not allow hysteresis to drop to zero or negative values if a larger  $R_H$  is used. Instead, hysteresis reaches a guaranteed minimum (15mV typical) and increases with increasing  $R_H$ , preventing comparator oscillation.

**Versatile On/Off Control**

The LTC4261 provides various methods of on/off control using the ON,  $\overline{EN}$ , UVH/UVL/OV, PGIO or  $\overline{FLTIN}$  pins along with the I<sup>2</sup>C interface. Turning on or off the pass transistor can be either autonomous or controlled by the system host through the I<sup>2</sup>C interface. Furthermore, the LTC4261 may reside on either the removable board or on the backplane.

Even when operating autonomously, the host can exercise control over the GATE output through I<sup>2</sup>C, although  $\overline{EN}$  and ON could subsequently override conditions set by I<sup>2</sup>C



**Figure 6. The LTC4261 provides versatile on/off control**

command. Card insertion/extraction can be conveniently detected with the  $\overline{EN}$ -changes-state bit in the FAULT register. After power-up, UV, OV and other fault conditions seize control as needed to turn off the GATE output, regardless of the state of  $\overline{EN}$ , ON or the I<sup>2</sup>C port.

Auto-retry following the faults can be enabled or disabled by the host at any time and the configurations are stored in the CONTROL register (Table 1). Although PGIO (when configured as an input) and  $\overline{FLTIN}$  control nothing directly, they are useful for I<sup>2</sup>C monitoring of connection sense or other important signals. The host can then use the information detected by these two pins to take action.

Figure 6 shows some examples for on/off control using the LTC4261. The circuits in Figures 6a to 6d work equally well in both backplane and board resident applications. Circuits in Figures 6e and 6f are for I<sup>2</sup>C-only control.

### Broadcast Mode Saves Cost and Space

To facilitate I<sup>2</sup>C communication between the LTC4261 and a system host that are isolated from each other, the SDA signal is split into SDAI and SDAO. Separate pins allow the device to drive optoisolators with a minimum number of external components. Still, three optoisolators (two for inputs on SCL and SDAI, and one for output on SDAO) are needed for typical I<sup>2</sup>C operations. To further reduce component count, the LTC4261 provides a special single-wire mode that only uses the SDAO pin to continuously transmit ADC data and fault information (Figure 7). This simple communication mode saves component cost and board space by eliminating two optoisolators and is useful for applications where only monitoring is needed.

The single-wire broadcast mode is simply enabled by tying the ADR1 pin to INTV<sub>CC</sub> and the ADR0 pin to V<sub>EE</sub> (Figure 7). At the end of conversion of each ADC channel, a serial data stream is sent out to SDAO with a fixed data rate of 15.3kHz  $\pm$ 20% in the format shown in Figure 8. The data stream

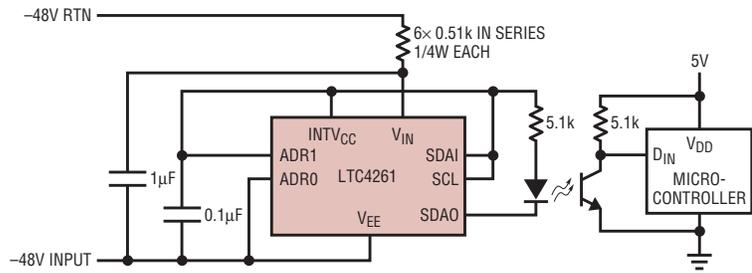


Figure 7. The LTC4261 in single-wire broadcast mode reports ADC data and fault information using a single optoisolator and the SDAO signal.

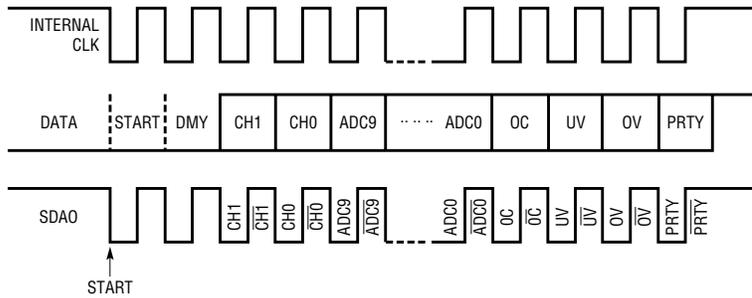


Figure 8. Data format of the single-wire broadcast mode

consists of a start bit (STAT), a dummy bit (DMY), two bits of ADC channel labeling (CH1 and CH0), ten bits of ADC data (ADC9:0), three fault bits (OC, UV, OV) and a parity bit (PRTY). The data are encoded with an internal clock in a way similar to Manchester encoding that can be easily decoded by a microcontroller.

### Which of the Four Fuses is Open?

Some high availability systems such as AdvancedTCA require dual feeds on both -48V and RTN lines and a fuse on each feed, resulting in four fuses. Since the plug-in card is designed to operate without interruption even if one of the fuses is open, it can be dif-

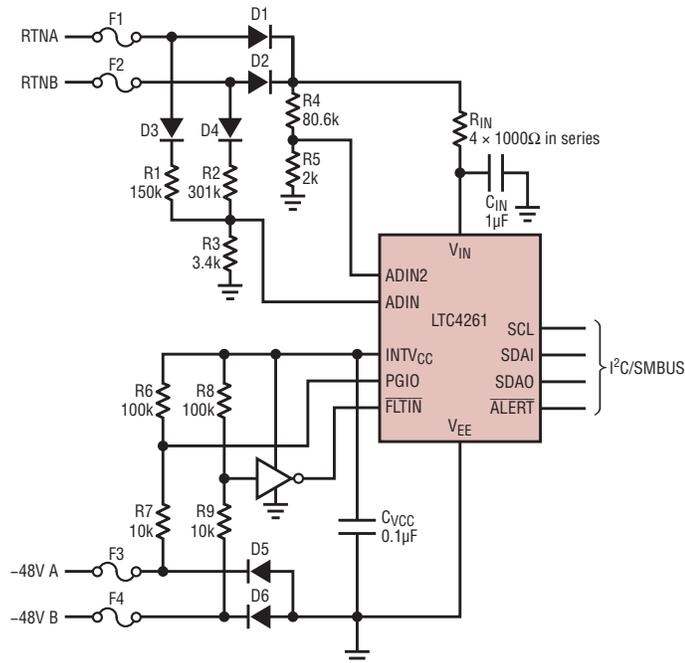


Figure 9. LTC4261 makes it possible to determine which of the four fuses is open in an AdvancedTCA system.

**Table 2. The voltages at ADIN and ADIN2 (referred to  $V_{EE}$ ) indicate which RTN fuse is open in the 4-fuse monitor in Figure 9**

|  |                         |
|--|-------------------------|
| $V_{ADIN} = V_{ADIN2} = 0V$                                | Both F1 and F2 are open |
| $0.25 \cdot V_{ADIN2} \leq V_{ADIN} < 0.7 \cdot V_{ADIN2}$ | F1 is open              |
| $0.7 \cdot V_{ADIN2} \leq V_{ADIN} < 1.1 \cdot V_{ADIN2}$  | F2 is open              |
| $V_{ADIN} > 1.1 \cdot V_{ADIN2}$                           | Normal Operation        |

difficult, without direct fuse monitoring, to detect a single open fuse.

The integrated ADC, I<sup>2</sup>C monitoring, and general-purpose pins of the LTC4261 make it possible to monitor the individual fuses, as shown in Figure 9. Fuses on the RTN side are sensed using resistors R1, R2 and R3 with the output measured by the ADC at the ADIN pin. At the same time, the input voltage after the ORing diodes is sensed using R4 and R5 and measured at the ADIN2 pin. Diodes D3 and D4 are used to compensate the ORing

diodes. Table 2 shows how the voltages at ADIN and ADIN2 indicate which fuse on the RTN side is open.

Using the input voltage as the reference ensures valid detection in the full operating range.

Fuse monitoring on the -48V side is more straightforward using the INTV<sub>CC</sub> pin along with two logic input pins, PGIO (when configured as input) and  $\overline{FLTIN}$  as shown in Figure 9. Fuse F3 is sensed with R6 and R7 at PGIO, and fuse F4 is sensed with R8 and R9 at  $\overline{FLTIN}$  with inverted input. If F3

is open, PGIO is pulled high and the PGIO input bit in the FAULT register is set. If F4 is open,  $\overline{FLTIN}$  is pulled low and the FLTIN bit is set. In the latter case, if the corresponding bit in the ALERT register is also set, the LTC4261 interrupts the host using the ALERT pin.

## Conclusion

The LTC4261 is a full-featured, intelligent Hot Swap controller that enhances the reliability and durability of high availability -48V power systems. The internal 10-bit ADC, I<sup>2</sup>C/SMBus and registers make it easy to monitor faults and real-time power and communicate with the system host. Its unique inrush and overcurrent control technique minimizes stresses on the pass transistor in all operating conditions. 

LTC4304, continued from page 12

nection between SDAIN and SDAOUT, and SCLIN and SCLOUT is broken, isolating the problem device from the bus.  $\overline{FAULT}$  pulls low indicating a stuck bus. At this time it is assumed that the MCU and the device it is communicating with are out of sync. The MCU sent out all of the clocks necessary for the transaction, but the device is still in the middle of the transaction. The device is waiting for more clocks to finish putting its data on the bus, and the last bit it put on the bus happened to be a low, hence it holds the bus low until it gets more clocks (bus is stuck). Because the connection is broken, the problem device is now isolated from the I<sup>2</sup>C bus, and the rest of the system is free to resume normal operation.

After the connection is broken, the LTC4304 automatically generates up to 16 clock pulses at 8.5kHz on SCLOUT, enough clocks to clear the internal register on the problem device. The device could be cleared with one or any number of clocks (up to 16) depending on how the fault occurred. At anytime, if SDAOUT and SCLOUT go high,  $\overline{FAULT}$  is released to go high and the automatic clocking is stopped, and a connection is automatically enabled.

When the slave that was stuck sees a START bit after connection, it will abort the stalled communication and reset. The fault is cleared independently of the MCU. If the fault cannot be cleared, the offending circuit remains isolated from the system. Figure 2 shows an example of a stuck bus being resolved with automatic clocking.

## Supply Independence and Level Translation

The LTC4304 can be the bridge between a backplane operating at one voltage and a card operating at a different voltage. Figure 3 shows some typical configurations. Notice that V<sub>CC</sub>, the pull-up voltage on SDAIN and SCLIN and the pull-up on SDAOUT and SCLOUT are independent of each other.

The rise time accelerators must be disabled when the bus pull-up voltage is lower than V<sub>CC</sub>. Figure 3a shows a situation where the V<sub>CC</sub> is higher than the pull-up voltage on SDAIN and SCLIN. In this case  $\overline{ACC}$  must be floating, disabling the rise time accelerators on the inputs only. In Figure 3b, V<sub>CC</sub> is equal to the output side pull-up voltage, and less than input side pull-up voltage.  $\overline{ACC}$  is connected to GND to

enable all four rise time accelerators. Finally, in Figure 3c, V<sub>CC</sub> is greater than the pull-up voltages of both sides.  $\overline{ACC}$  is connected to V<sub>CC</sub> to disable all four accelerators.

## Conclusion

The LTC4304 is a multifunctional device with an impressive number of features designed to increase the reliability of an I<sup>2</sup>C bus. The flexible architecture allows the LTC4304 to be configured into almost any system. The LTC4304 isolates and resolves stuck buses independently of the MCU. Capacitance buffering, level translation, Hot Swap features and ±15kV human body ESD protection make the LTC4304 an ideal solution for any I<sup>2</sup>C application.

The LTC4304 is offered in small 10 pin MSOP and DFN (3mm × 3mm) packages.

A feature-reduced version of the LTC4304 is also available. The LTC4303 provides all of the functionality of the LTC4304 with the exception of the  $\overline{FAULT}$  output flag and  $\overline{ACC}$  control pin. The LTC4303 is a drop in replacement for the LTC4300A-1 and its rise time accelerators are permanently enabled. 

# High Efficiency Nickel Charger Operating to 34V is Easily Configured to Deliver a Safe Fast Charge

by James A. McKenzie

## Introduction

The LTC4011 is a complete standalone nickel chemistry fast charger that operates at high efficiency with an input voltage of up to 34V, even with a battery voltage that is much less than the DC input supply. Typical efficiency with a 5.5V and 20V input supply is shown in Figure 1. An undervoltage lockout of 4.25V ensures stable operation with an input as low as 5V, assuming a 10% tolerance. The IC offers a full range of charge control features that are easy to program with a minimal number of external components. Its multiple levels of safety features provide reliable fault protection that is also simple to configure. The LTC4011 functions without the need for any host Microcontroller Unit (MCU) support and requires no software of firmware.

## Accurate, Rock-Solid Fast Charge Termination

The LTC4011 implements a complete fast charge control algorithm, best suited for charge rates of C/2 to 2C

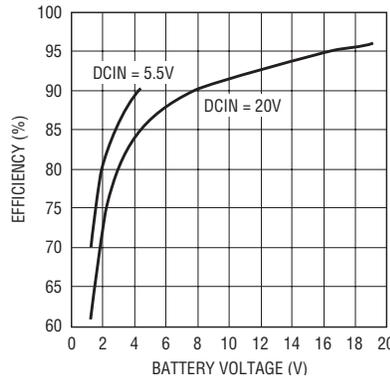


Figure 1. The LTC4011 charging efficiency with 2A output current.

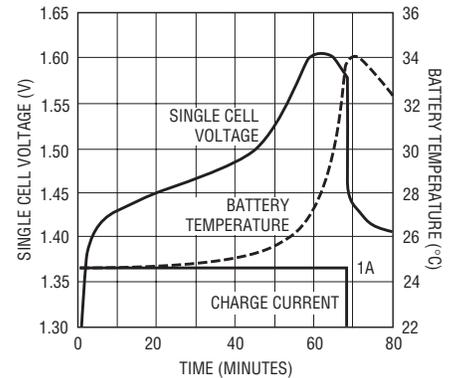


Figure 2. A 1C NiCd charge cycle

for NiMH batteries and C/3 to C, or higher, for NiCd batteries. This means fully discharged batteries can be recharged to 100% capacity in one hour or less. Reliable charge termination at these higher rates is controlled by well-proven voltage and temperature detection techniques tailored to the selected nickel chemistry to ensure minimum charge time without degradation of recharge cycle life. Various

internal and external filters, both analog and digital, eliminate spurious noise in the voltage and temperature data channels used to determine both general battery health and appropriate charge termination.

## Monitoring Battery Voltage for $-\Delta V$

The primary fast charge termination technique employed by the LTC4011 involves detection of peak battery

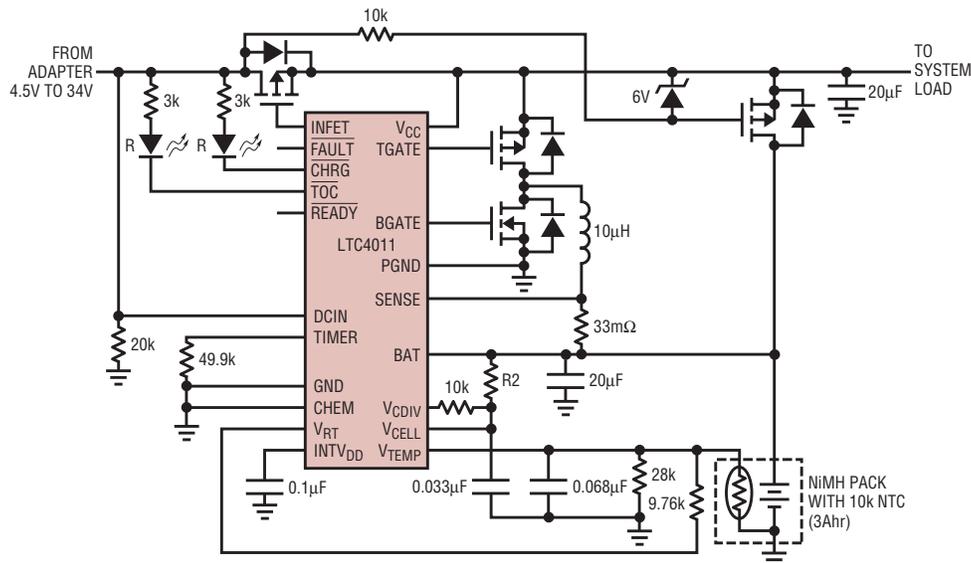


Figure 3. A 3A NiMH charger with full PowerPath control

voltage followed by a sufficient drop in that terminal potential ( $-\Delta V$  detection). The typical NiCd charge cycle shown in Figure 2 is terminated by  $-\Delta V$ .

To support a wide range of battery pack configurations, the IC senses the average cell voltage of the battery pack. A simple resistive voltage divider between the positive battery terminal and the  $V_{CDIV}$  pin, along with some capacitance to eliminate residual PWM switching noise, is all that is required to provide this average cell voltage to the  $V_{CELL}$  input pin. This technique, combined with the 5V to 34V input operating range, allows charging of from 1 to 16 in-series nickel cells. A negative delta of only 10mV to 20mV per cell indicates the battery is fully charged. The  $V_{CELL}$  voltage is also monitored as a measure of basic battery health and to detect catastrophic fault conditions, as described below.

## Monitoring Battery Temperature for $\Delta T/\Delta t$

The LTC4011 can also process battery temperature using information provided by a negative temperature coefficient (NTC) thermistor. The thermistor should be in good thermal contact with the cell casings located most near the center of mass of the battery pack. This thermistor is then included in a voltage divider network between the  $V_{RT}$  pin and ground, as shown in Figure 3, to provide a linearized input to the  $V_{TEMP}$  pin. This configuration is flexible enough to support a very wide range of NTC thermistor types.

An external analog single-pole passive filter is recommended to eliminate PWM switching noise. The voltage on the  $V_{TEMP}$  pin is then used by the LTC4011 to qualify the charge process according to an acceptable range, roughly 0°C to 45°C. In addition, the internal data acquisition subsystem uses an on-board real-time clock to monitor the rate of temperature increase of the battery ( $\Delta T/\Delta t$ ) during fast charge. Values between 1°C/min and 2°/min typically indicate a fully charged nickel battery.

Figure 4 shows a NiMH charge cycle at a 1C rate with the fast charge

portion of the charge cycle terminated by  $\Delta T/\Delta t$ . Temperature processing is optional on the LTC4011 for all chemistries. Simply tying  $V_{TEMP}$  to  $V_{RT}$  disables all temperature-based charge qualification and termination.

## Chemistry-Specific Battery Profiling

The basic charging algorithm applied by the LTC4011 is modified for the selected battery chemistry. Tying the CHEM pin to ground selects NiMH charging parameters, while leaving the CHEM pin open or tying it to  $V_{RT}$  selects NiCd charging parameters. While similar, these chemistries do require slightly different fast charge termination to ensure maximum recharge cycle life. The older NiCd chemistry benefits from slight overcharge. When charging NiCd cells, the LTC4011 uses threshold levels that favor  $-\Delta V$  termination, resulting in a final charge of slightly more than the rated capacity (100%) of the pack. In this case,  $\Delta T/\Delta t$  termination, if enabled, serves as a secondary termination technique for additional safety. This is shown in the example of Figure 2.

Newer NiMH batteries are normally designed to accept higher charge rates than their older NiCd cousins, but manufacturers often warn against any amount of overcharge. So, for NiMH cells, the LTC4011 selects internal thresholds that favor  $\Delta T/\Delta t$  termination at a point when the pack is charged to about 95% capacity. In order to avoid false termination on highly discharged cells that have been inactive for a long period of time, the IC can vary the  $\Delta T/\Delta t$  limit as the fast charge cycle

progresses. The  $-\Delta V$  limit then serves as secondary termination (safety), and the IC applies a timed top-off charge after fast charge termination to achieve 100% capacity, as shown in Figure 4. Obviously, while optional, use of a thermistor input for NiMH batteries is strongly recommended.

In addition to these chemistry-specific measures, the LTC4011 applies some generic charge profile techniques. Battery open-circuit voltage is measured at the beginning of a new charge cycle to determine the state of charge of the attached pack. If the pack is initially heavily discharged, the IC applies a smaller conditioning current for a fixed period of time to recover the battery to a point of suitable fast charge acceptance. If the pack is initially discharged, the LTC4011 applies a  $-\Delta V$  termination hold-off period to allow the internal chemistry—and hence terminal potential—to stabilize after applying full charge current. This avoids premature termination. However, if the pack is already moderately charged, the initial terminal voltage is well-behaved and  $-\Delta V$  processing begins immediately to avoid accidental overcharging of the battery. If enabled,  $\Delta T/\Delta t$  detection is always active.

## Automatic Recharge Keeps Batteries Ready for Use

Nickel batteries exhibit a high self-discharge rate of up to 3% per day. Once a charge cycle has completed, the LTC4011 continues to monitor the open-circuit terminal voltage of the battery for as long as an input power source is connected. If the battery volt-

Table 1. LTC4011 time limit programming examples

| $R_{TIMER}$ ( $\Omega$ ) | Typical Fast Charge Rate | Precharge Limit (minutes) | Fast Charge Stabilization (minutes) | Fast Charge Limit (hours) | Top-Off Charge (minutes) |
|--------------------------|--------------------------|---------------------------|-------------------------------------|---------------------------|--------------------------|
| 24.9k                    | 2C                       | 3.8                       | 3.8                                 | 0.75                      | 15                       |
| 33.2k                    | 1.5C                     | 5                         | 5                                   | 1                         | 20                       |
| 49.9k                    | 1C                       | 7.5                       | 7.5                                 | 1.5                       | 30                       |
| 66.5k                    | 0.75C                    | 10                        | 10                                  | 2                         | 40                       |
| 100k                     | 0.5C                     | 15                        | 15                                  | 3                         | 60                       |

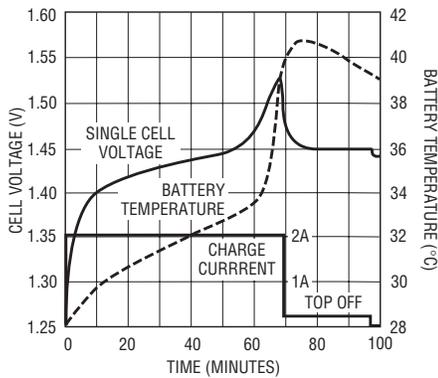


Figure 4. Typical NiMH charge cycle at 1C

age indicates a loss of more than about 15% capacity, a refresh fast charge cycle is initiated to bring the stored energy level back to 100%. The duration of the recharge cycle is normally only a few minutes. This technique replaces more traditional continuous trickle charge methods. Trickle charge operates the battery in a constant state of overcharge, which can reduce the cycle life of some NiMH cells, generates continuous heat, and is somewhat less efficient than the LTC4011 automatic recharge approach.

### Multiple Safety Features

Many safety features are built into the LTC4011. It monitors important voltage and temperature parameters during all charging phases.

If the  $V_{TEMP}$  input has been enabled, the sensed temperature is required to lie between 0°C and 45°C, or charging is suspended. After fast charge begins, the battery temperature is allowed to rise to 60°C. If this limit is exceeded, however, the sensed temperature must fall below 45°C before charging can resume. The LTC4011 also tracks its own die temperature and disables charging if it rises above an acceptable limit.

Charging is not allowed to begin until the necessary voltage headroom to operate the PWM (about 500mV) has been established between the  $V_{CC}$  and BAT pins. The battery voltage is also continuously monitored for overvoltage. If the average cell voltage on  $V_{CELL}$  exceeds 1.95V, charging is disabled and a fault is indicated. The LTC4011 also profiles the battery voltage during charging to ensure

proper charge acceptance, checking open-circuit voltage at the beginning of precharge and fast charge, and in-circuit voltage after about 20% of the fast charge cycle has been completed.

Finally, the LTC4011 contains a safety timer that limits the length of time any single charge can continue. This timer is easily programmed with an external resistor connected between  $TIMER$  and  $GND$  according to the formula  $R_{TIMER} (\Omega) = t_{MAX} (\text{hours})/30\mu\text{s}$ .

### Timing Can be Everything

The LTC4011 uses the programming of the safety timer to a variety of purposes by inferring a relation between the set time limit, the programmed charge current and the capacity of the battery being charged. It assumes the period of this timer is set to 150% of the time normally required to deliver 100% charge to a fully discharged battery at the programmed current of  $R_{SENSE}/100\text{mV}$ . The safety checkpoints discussed above, along with top-off charge duration, are then determined by intermediate intervals of the safety timer. Table 1 shows suitable values for  $R_{TIMER}$  for a range of programmed fast charge rates.

### A Smaller PWM Solution

The LTC4011 also embodies a complete PWM controller. Its buck regulator uses a synchronous pseudo-constant off-time architecture with high-side PFET power switch. This choice yields a PWM that is extremely easy to configure with a minimum number of external parts. Simply connect the external PFET power switch, optional NFET synchronous diode, the Schottky clamp and choke as shown in Figure 3. No external loop compensation is required, and the charge current is set by a single resistor connected between the  $SENSE$  and  $BAT$  pins. This resistor is in series between the inductor output and the battery with a value determined by the equation  $R_{SENSE} = 100\text{mV}/I_{PROG}$ .

The LTC4011 PWM uses a unique floating LV differential architecture to deliver 5% current accuracy and low cycle-to-cycle jitter with high inductor ripple current. That in turn allows

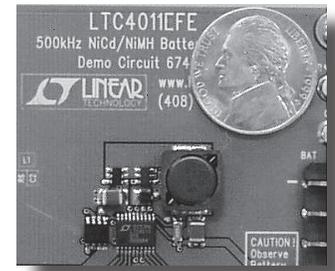


Figure 5. NiCd/NiMH charger layout

use of space-efficient magnetics and a smaller output filter capacitor. The pseudo-constant off-time architecture eliminates the need for cumbersome slope compensation and allows full continuous operation over a wide  $V_{IN}/V_{OUT}$  range without generation of audible noise, even when using ceramic capacitors. Typical operating frequency is 550KHz. An example of the LTC4011 with a 2A PWM implementation is shown in Figure 5.

### PowerPath Control

PowerPath™ control is a vital part of proper termination when charging nickel batteries. Because the differences being sensed for  $-\Delta V$  termination are so small, the series resistance of the battery can easily cause premature termination if varying load current is drawn from the battery during charging.

The LTC4011 provides integrated PowerPath support for an input PFET transistor between the DC input ( $DCIN$ ) and the host's unregulated system supply ( $V_{CC}$ ). This FET then acts as an ideal rectifier with a regulated forward drop as low as 50mV, requiring less operating head room and capable of producing less heat than a conventional blocking diode. The LTC4011 can provide up to 6V of gate drive to this pass device. Select an input FET with a low enough  $R_{DS(ON)}$  at this gate drive level so that the combination of full charge current and full application load current does not cause excessive power dissipation.

As shown in Figure 4, the PFET between  $BAT$  and  $V_{CC}$  then serves to automatically disconnect the battery from the system load as long as a DC input is present. A Schottky diode

*continued on page 23*

# Tiny Controller Makes It Easy to Charge Large Capacitors

by David Ng

## Introduction

Emergency warning beacons, inventory control scanners, professional photoflash and many other systems operate by delivering a pulse of energy to a transducer. This energy typically comes from a large capacitor that has been charged to some predetermined voltage.

The LT3750 is a current-mode flyback controller optimized for charging large value capacitors to a user selected target voltage. This target voltage is set by the turns ratio of the flyback transformer and just two resistors in a simple, low voltage network, so there is no need to connect components to the high voltage output. The charging current is set by an external sense resistor and is monitored on a cycle-by-cycle basis. The LT3750 is available in a space saving MSOP-10 package.

The device is compatible with a wide range of control circuitry, being equipped with a simple interface consisting of a CHARGE command input bit and an open drain DONE status flag. Both of these signals are compatible with most digital systems, yet tolerate voltages as high as 24V.

## Simple 300V, 400 $\mu$ F Charger

Figure 1 shows the schematic of a LT3750 circuit that charges a 400 $\mu$ F capacitor to a target voltage of 300V. The 1:10 turns ratio of T1 and the R1, R2 resistors set the target voltage to 300V, while the R4 power resistor sets the peak charging primary current to 7.5A.

Operating from a 12V power source, this circuit charges the 400 $\mu$ F capacitor to 300V in 1.04 seconds, as shown in Figure 2.

## Design Considerations

The architecture balances a high degree of integration with flexibility—leaving key parameters definable by the user. The important issues to

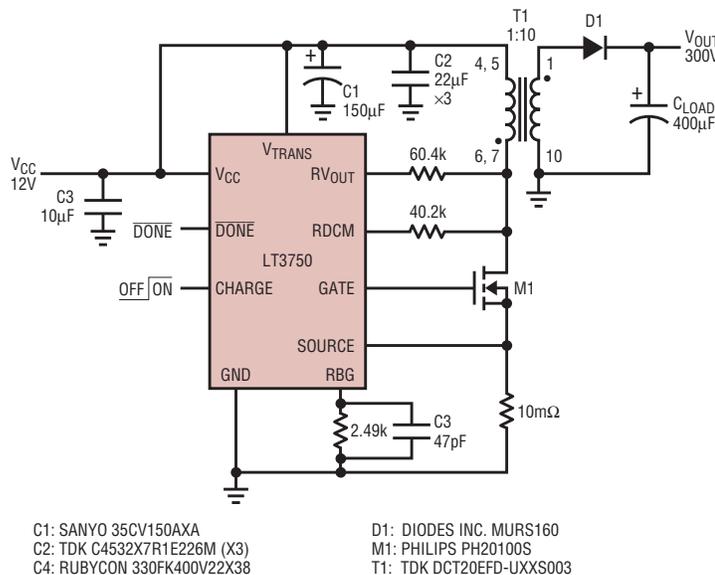


Figure 1. Simple circuit charges a 400 $\mu$ F capacitor.

consider in completing a design are input capacitor sizing, transformer design and output diode selection.

## Power Stage Input Capacitor

Every switching cycle, the LT3750 measures the voltage at its RV<sub>OUT</sub> pin to determine the transformer, T1, flyback voltage. It also measures the signal at its V<sub>TRANS</sub> pin, which is the voltage at the input of the power switching stage. The difference of these two signals, accounting for the T1 transformer turns ratio and the D1 rectifying diode, yields the output voltage. In order to get an accurate result, it is important that the signal at the LT3750's V<sub>TRANS</sub> input

optimally reflects the DC potential of the power stage input. Consequently, the capacitance at the input of the power switching stage must be chosen such that the ripple voltage at the V<sub>TRANS</sub> input is not excessive. The capacitor bank in the circuit represented by Figure 1 is actually made of five capacitors. C1 is a single 150 $\mu$ F electrolytic capacitor to provide bulk energy, C2 is three low ESR 22 $\mu$ F ceramic capacitors to accommodate the high switching currents, and C3 is low ESR 10 $\mu$ F ceramic capacitor that provides local decoupling to the LT3750. For best results, place C1 and C2 as close as possible to T1, and C3

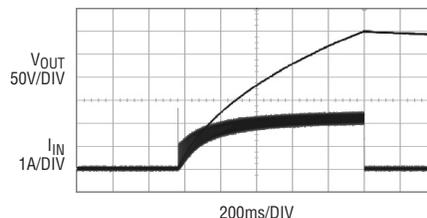


Figure 2. Output voltage and input current waveforms of LT3750 capacitive charging circuit

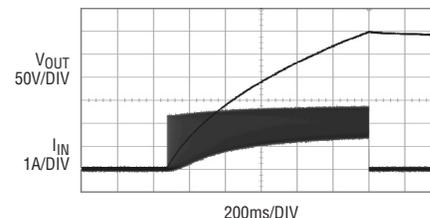


Figure 3. A transformer with a 51 $\mu$ H primary inductance has a longer charge time and larger input current ripple than a transformer with a 10 $\mu$ H primary inductance.

as close as possible to the  $V_{\text{TRANS}}$  pin on the LT3750.

### Transformer

Other than the turns ratio, there are two issues to remember when selecting a transformer. The first is that the transformer secondary must be constructed to withstand potentials of both the positive and negative voltages associated with charging the capacitor. This withstand voltage is not the same as the isolation voltage rating. In the case of the circuit shown in Figure 1, there is no isolation voltage requirement, as the primary and secondary of T1 are tied to the same ground reference. The secondary winding, however, is subjected to the output potential, or 300V, and care must be taken in selecting for parameters relevant to such high voltages, such as pin spacing and wire insulation.

The other transformer parameter to keep in mind is the primary inductance. The primary inductance determines the operating frequency range, input current ripple and core loss, all of which contribute to the capacitor charge time and efficiency. The charging profile shown in Figure 2 is for a circuit using a transformer with a primary inductance of  $10\mu\text{H}$ . Figure 3 shows the charging profile for the same circuit, but the primary inductance is much larger,  $51\mu\text{H}$ . Note that the  $51\mu\text{H}$  transformer has a longer charge time than the  $10\mu\text{H}$  transformer.

Table 1. Summary of input charging current and charge times for LT3750 circuits for transformers with different primary inductances

| Transformer                | Primary Inductance | Input Charging Current | Input Charging Current Ripple | Charge Time |
|----------------------------|--------------------|------------------------|-------------------------------|-------------|
| TDK<br>DCT20EFD-UXXS003    | $10\mu\text{H}$    | 2.2A                   | 0.5A                          | 1040ms      |
| Coiltronics<br>CTX02-17314 | $15\mu\text{H}$    | 2.2A                   | 0.4A                          | 1000ms      |
| Coiltronics<br>CTX02-17144 | $51\mu\text{H}$    | 2A                     | 1.4A                          | 1120ms      |

Table 1 gives a summary of the input charging current and charge times for LT3750 circuits for three different T1 primary inductances, with the  $15\mu\text{H}$  device giving the best result.

### Output Diode

Finally, it is important to consider the high AC voltages when selecting the output rectifying diode. The circuit in Figure 1 has a 300V output, but the output rectifying diode must withstand the sum of the output voltage and the voltage across the transformer secondary when the MOSFET Q1 is on. In this case, that is about 500V. This is a high voltage, but there are many manufacturers that produce switching diodes suitable for this application.

While it is important to minimize board space, the designer must choose a device that does not cause a violation of the spacing requirements for both safety and producibility. According to

table 6-1, "Electrical Conductor Spacing," of *IPC-2221, Generic Standard on Printed Circuit Board Design* (February 1998 release), the minimum spacing between conductors that have a potential up to 500V must be no less than 2.5mm on an uncoated printed circuit board operated below an altitude of 3050m. The output diode must be chosen to ensure that the minimum spacing between the diode pads is at least 2.5mm.

The circuit shown in Figure 1 uses a MURS160, which is offered by a number of manufacturers such as Diodes Inc and Vishay. It is an ultrafast recovery rectifier and has a peak repetitive reverse voltage rating of 600V. The diode comes in an SMB package, which allows the edge-to-edge separation between the pads to be as much as 3mm. 

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LTC4011, continued from page 21

can be used in place of this MOSFET, if the additional voltage drop can be tolerated when running the application from the battery.

### Micropower Features Support Extended Battery Use

The LTC4011 has a typical shutdown supply current of  $3\mu\text{A}$  and normally draws much less than  $1\mu\text{A}$  from the SENSE/BAT pin combination when the DC input supply has been removed. In addition, the  $V_{\text{CDIV}}$  pin offers a means of disconnecting the

$V_{\text{CELL}}$  resistor divider in the shutdown state, eliminating the current drawn by that circuit when charging is not possible. These features greatly minimize the load applied to the battery by the charger when disconnected from a DC power source, increasing the useable run time of the battery in portable applications.

### Conclusion

The LTC4011 is a nickel chemistry charger that integrates a complete high voltage PWM controller, allow-

ing it to efficiently charge batteries from a 34V input without the need for additional current source control ICs. True standalone operation and flexible control greatly simplify charger design. The PWM operates at a high frequency, enabling the use of surface mount components to save space. Reliable, robust charge termination algorithms backed by solid safety features make the LTC4011 an excellent choice for a wide range of fast charge implementations, providing long life for rechargeable nickel batteries. 

# MOSFETs Make Sense for Tracking and Sequencing Power Supplies

by Thomas DiGiacomo

## Introduction: Charge MOSFETs with the Task of Supply Control

In electronic systems with multiple supplies, the need for tracking and/or sequencing is well established. On the one hand, core and I/O power might be required to ramp up and down together with less than a diode's voltage drop between them to avoid potentially destructive latch-up. Coincident tracking, as shown in Figure 1a, solves this problem. On the other hand, in a distributed supply chain, some supplies might need to be fully operational before others. Supply sequencing, as shown in Figure 1d, solves that problem. Other systems may require simultaneous completion of supply ramps (Figure 1b), voltage offsets or time delays (Figure 1c), or combinations of such profiles.

Linear's line of no-MOSFET tracking and sequencing control products, the LTC2923, LTC2925, and LTC2927, work outstandingly well with DC/DC converters and other supply generators that allow access to the feedback nodes that set their output voltage. In many applications, however, MOSFET control of power supply tracking and sequencing is necessary. Supply modules provide no access to their feedback node, and some linear regulators also resist the current-injection control method employed by the LTC2923 family.

MOSFET-controlled tracking and sequencing can improve power system segmenting and allow reuse, which reduces parts count and board area. A single-output supply generator can power different rails of the same voltage (e.g., analog power, digital power, and housekeeping power) because each rail's tracking profile can be set independently. Multiple-output modules can replace several single-input modules without the need for complex ON/OFF pin signaling to implement

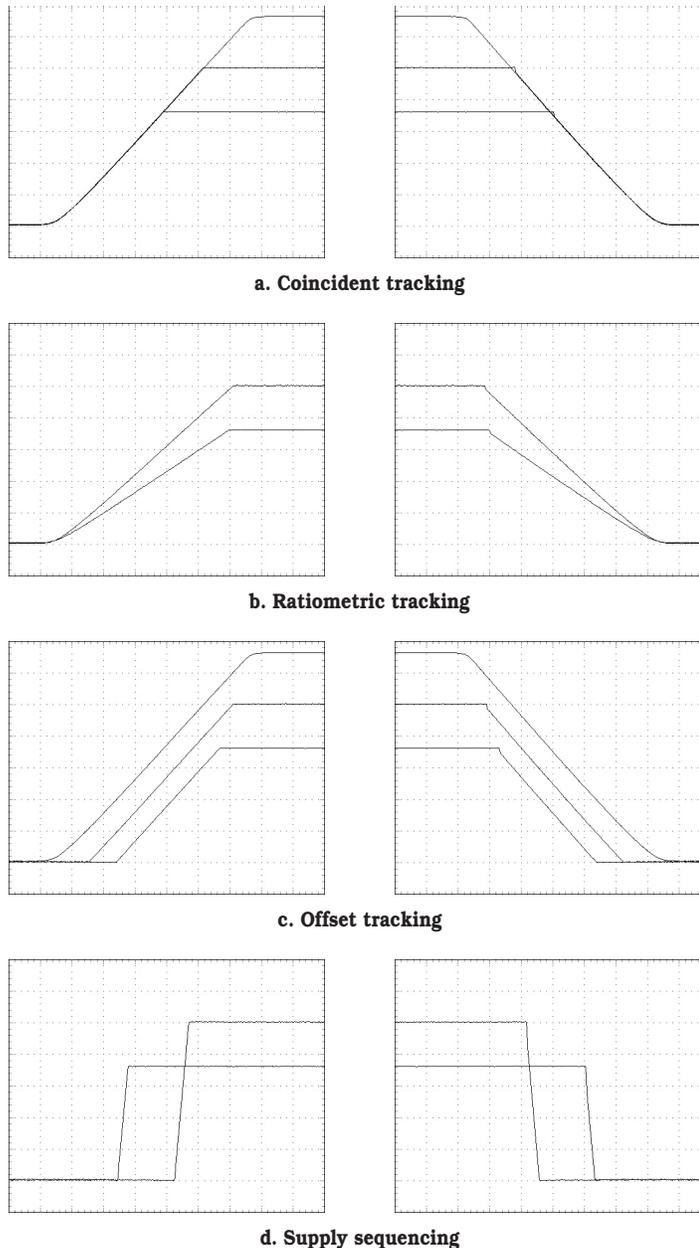


Figure 1. Power supply voltage tracking profiles

sequencing or tracking. Furthermore, a series MOSFET can be shut off, which guarantees that the load is disconnected when so desired.

The LTC2926 MOSFET-controlled power supply tracker provides exceptionally flexible control of supply tracking and sequencing that can

realize all of the profiles in Figure 1, and combinations of them. Each of two "slave" supplies can be configured independently to track a "master" ramp signal using just an N-channel MOSFET and a few resistors per supply. A single capacitor sets the slope of a voltage ramp that may be employed

as the master ramp signal (Figure 2), or may be used to ramp a third supply using an external MOSFET (Figure 3). The LTC2926 is interoperable with Linear's no-MOSFET tracking and sequencing products, and even offers no-MOSFET control itself in some applications (Figure 4); see "Direct Supply Generator Control: ¡No Más FETs, Mi Amigo!" in this article.

The LTC2926 also features automatic remote sense switching that compensates for voltage drops across the controlling MOSFETs, and two I/O signals that transmit tracking status and receive control input from upstream and downstream devices. The LTC2926 is available in 20-lead DFN (4mm x 5mm) and 20-lead narrow SSOP packages.

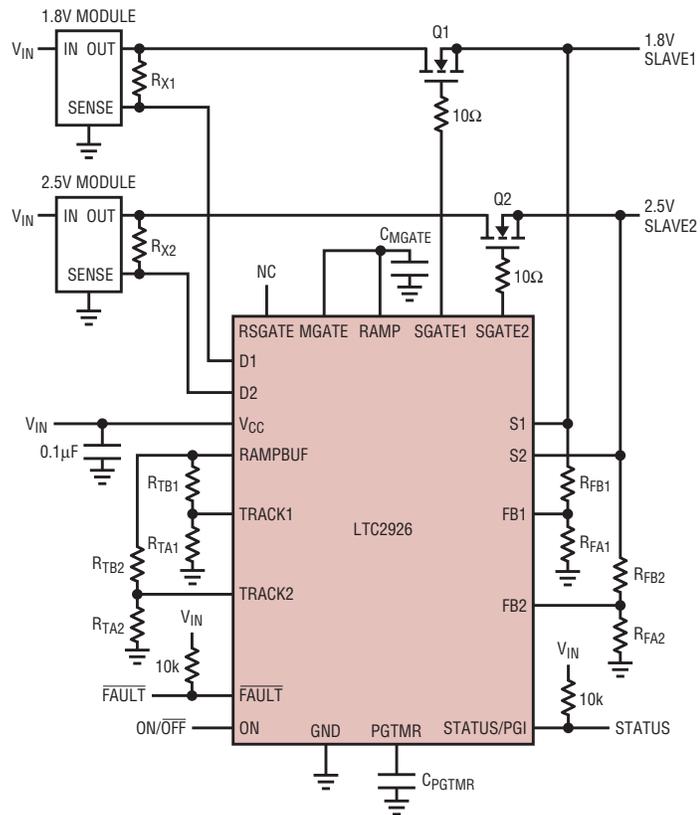
**How It Works:**

**Injection Controls Your Ramp-age and Keeps You on Track**

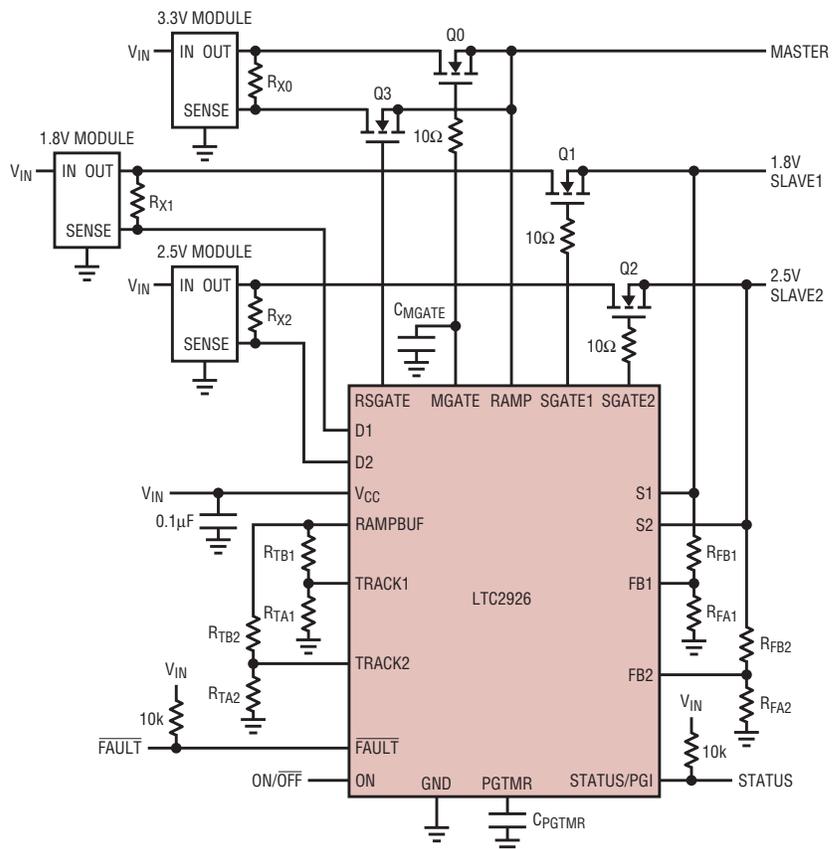
The LTC2926 achieves supply tracking and sequencing by influencing the feedback node that sets a supply voltage, as do the LTC2923, LTC2925, and LTC2927. In all four products, a tracking cell converts the master ramp voltage into a ramping current that is injected into the aforementioned feedback node. Whereas the latter products control supply generators themselves (those with accessible feedback nodes, like DC/DC converters), the LTC2926 controls rudimentary voltage regulators whose inputs are the supply voltages and whose outputs are the tracked and sequenced supply rails.

In Figure 5, the integrated gate controller cell, the external N-channel power MOSFET ( $Q_{EXT}$ ), and a resistive voltage divider ( $R_{FA}$  and  $R_{FB}$ ) form the basic voltage regulator. In regulation, the slave supply voltage equals the reference voltage times  $(1 + R_{FB}/R_{FA})$ . In drop out mode, the MOSFET becomes a closed switch, and the slave supply voltage equals the input supply voltage.

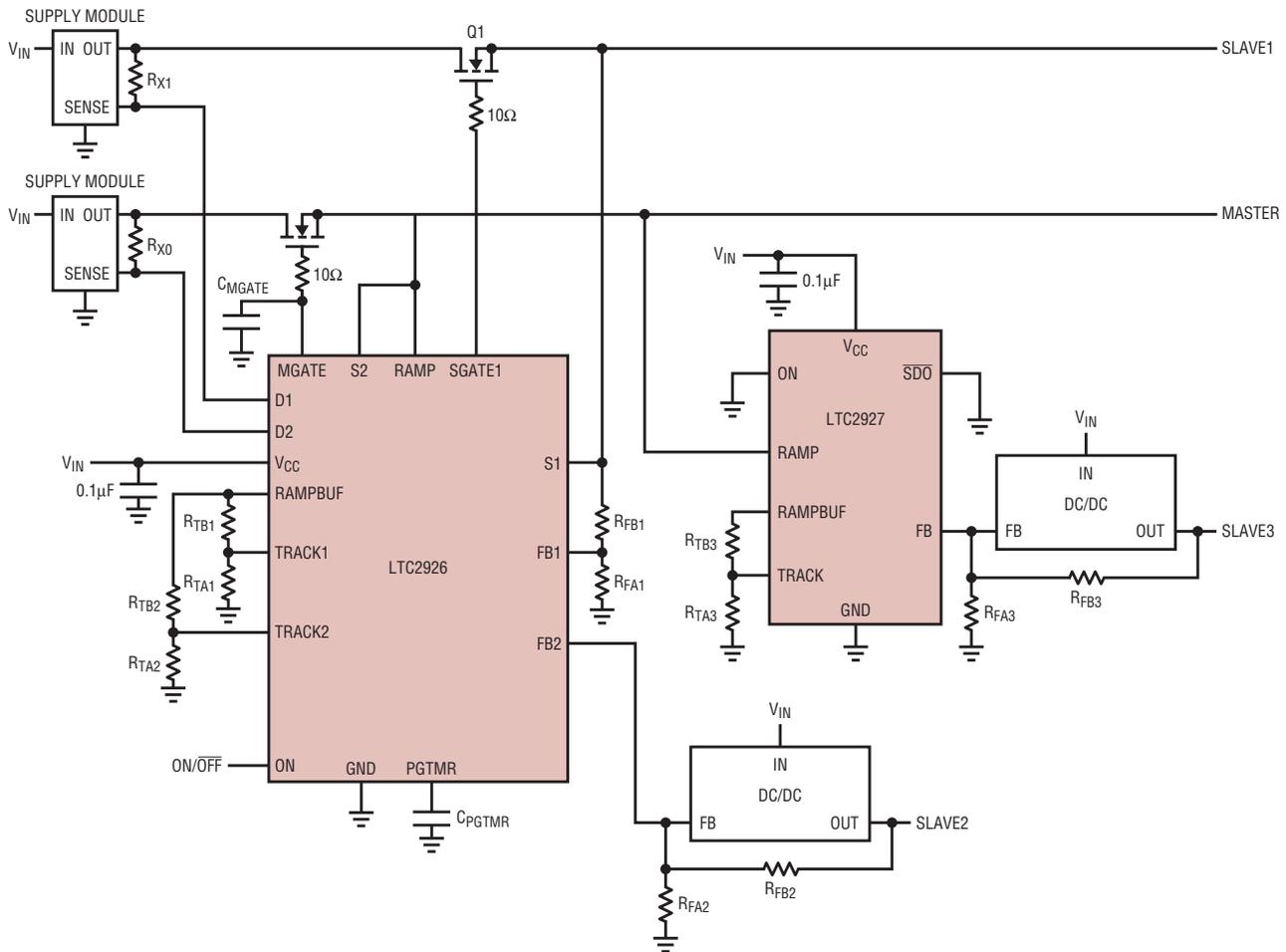
The injection of current at the feedback node of the gate controller regulator reduces the effective value of its reference voltage. As the master ramp rises, the fixed ratio of



**Figure 2. Typical 2-supply tracking application. The master ramp signal is created by connecting a capacitor from the MGATE and RAMP pins to ground.**



**Figure 3. Typical 3-supply tracking application. MOSFET Q0 creates a ramping master supply that doubles as the master ramp signal.**



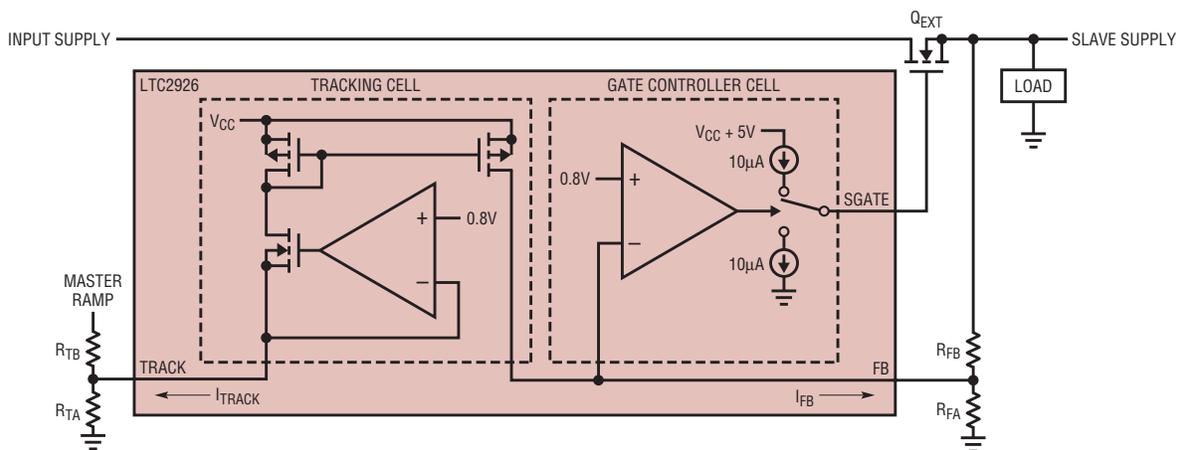
**Figure 4. LTC2926 and LTC2927 4-rail application. The second slave channel of the LTC2926 requires no MOSFET in this example.**

the feedback resistors multiplies the increasing reference voltage to create a rising slave supply voltage that is limited by the input supply voltage at the drain of the MOSFET. With proper selection of the feedback resistor ratio, the gate controller cell drives

the SGATE pin to  $V_{CC} + 5V$  when the slave supply reaches its maximum. The logic-level MOSFET becomes a simple closed switch, able to pass input supply voltages of from  $0V$  to  $V_{CC}$ .

The relationship between the master ramp and the slave voltage is

called the tracking profile, and it is a function of the input supply voltage, the master ramp voltage, the track resistors ( $R_{TA}$ ,  $R_{TB}$ ), and the feedback resistors ( $R_{FA}$ ,  $R_{FB}$ ). All of the profiles in Figure 1 can be realized by properly selecting the track and feedback resis-



**Figure 5. Simplified tracking cell and gate controller cell combination**

tors. Combinations are also possible because each channel's profile is set independently.

**MOSFETs Make Remote Sense, Too: Whip a Problem with a Switch**

Even with the selection of a low  $R_{DS(ON)}$  MOSFET as the tracking control device, the load current causes a voltage

difference between the supply generator and the load. Worst yet, dynamic load current produces a dynamic voltage error. Without modification, the standard solution, to let the supply generator remotely sense the load voltage and compensate for the drop, does not work. During tracking up or down, the load voltage is deliberately

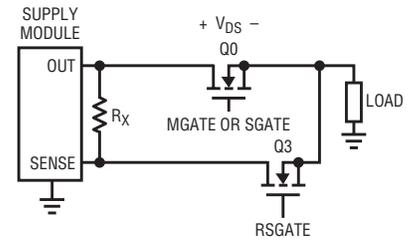


Figure 6. Functional schematic for remote sensing the load

**Tracking and Sequencing Supply Rails in Three Easy Steps**

Any of the profiles shown in Figure 1 can be achieved by using the following simple design procedure. Figure 3 shows a basic 3-supply application circuit.

**1. Set the ramp rate of the master signal.**

Solve for the value of  $C_{MGATE}$  based on the desired ramp rate (volts per second) of the master ramp signal,  $S_M$ , and the MGATE pull-up current.

$$C_{MGATE} = \frac{I_{MGATE}}{S_M} \quad (1)$$

where  $I_{MGATE} \approx 10\mu A$

If the gate capacitance of the MOSFET is comparable to  $C_{MGATE}$ , reduce the value of  $C_{MGATE}$  to account for it. If the master ramp signal is not a master supply, tie the RAMP pin to the MGATE pin

**2. Choose the feedback resistors based on the slave supply voltage and slave load.**

It is important that the feedback resistors are significantly larger than the load resistance. Determine the effective slave load resistance,  $R_L$  (not shown), to satisfy the following equation:

$$\begin{aligned} R_{FB} &\geq 100 \cdot R_L \text{ (recommended),} \\ R_{FB} &\geq 23 \cdot R_L \text{ (required)} \end{aligned} \quad (2)$$

The LTC2926 must be able to fully enhance the slave control MOSFET at the end of ramping. Select  $R_{FA}$  based on the resistor tolerance,  $TOL_R$ , and the absolute maximum slave supply voltage,  $V_{SLAVE(max)}$ :

$$R_{FA} < R_{FB} \cdot \left( \frac{1 - TOL_R}{1 + TOL_R} \right) / \left( \frac{V_{SLAVE(max)}}{V_{FB(REF)(min)}} - 1 \right) \quad (3)$$

where  $V_{FB(REF)(min)} = 0.784V$

Note: Design with a value of  $V_{SLAVE(max)}$  that covers the maximum possible slave supply voltage by a good margin. If the slave generator exceeds that voltage during operation, an overvoltage shutdown can occur. The gate controller cell will turn off the MOSFET in an attempt to reduce the over-range supply voltage, which activates the STATUS/PGI pull-down, and thus a fault can occur if the power good timeout period has passed.

If no-MOSFET operation is desired and conditions for it are met, let the generator's design set  $R_{FA}$  and  $R_{FB}$ , substitute the generator's reference voltage for  $V_{FB(REF)}$  in step 3.

**3. Solve for the tracking resistors that set the desired ramp rate and voltage offset or time delay of the slave supply.**

Choose a ramp rate for the slave supply,  $S_S$ . If the slave supply tracks the master coincidentally or with only a fixed offset or delay, then the slave ramp rate equals the master ramp rate. Calculate the upper track resistor,  $R_{TB}$ , from:

$$R_{TB} = R_{FB} \cdot \left( \frac{S_M}{S_S} \right) \quad (4)$$

Choose a voltage difference based on the type of profile to be implemented:

$$\Delta V = \text{a voltage difference (offset tracking),} \quad (5a)$$

or

$$\Delta V = S_M \cdot t_{DLY} \text{ (supply sequencing),} \quad (5b)$$

where  $t_{DLY}$  is a delay time,

or

$$\Delta V = 0V \text{ (coincident or ratiometric tracking)} \quad (5c)$$

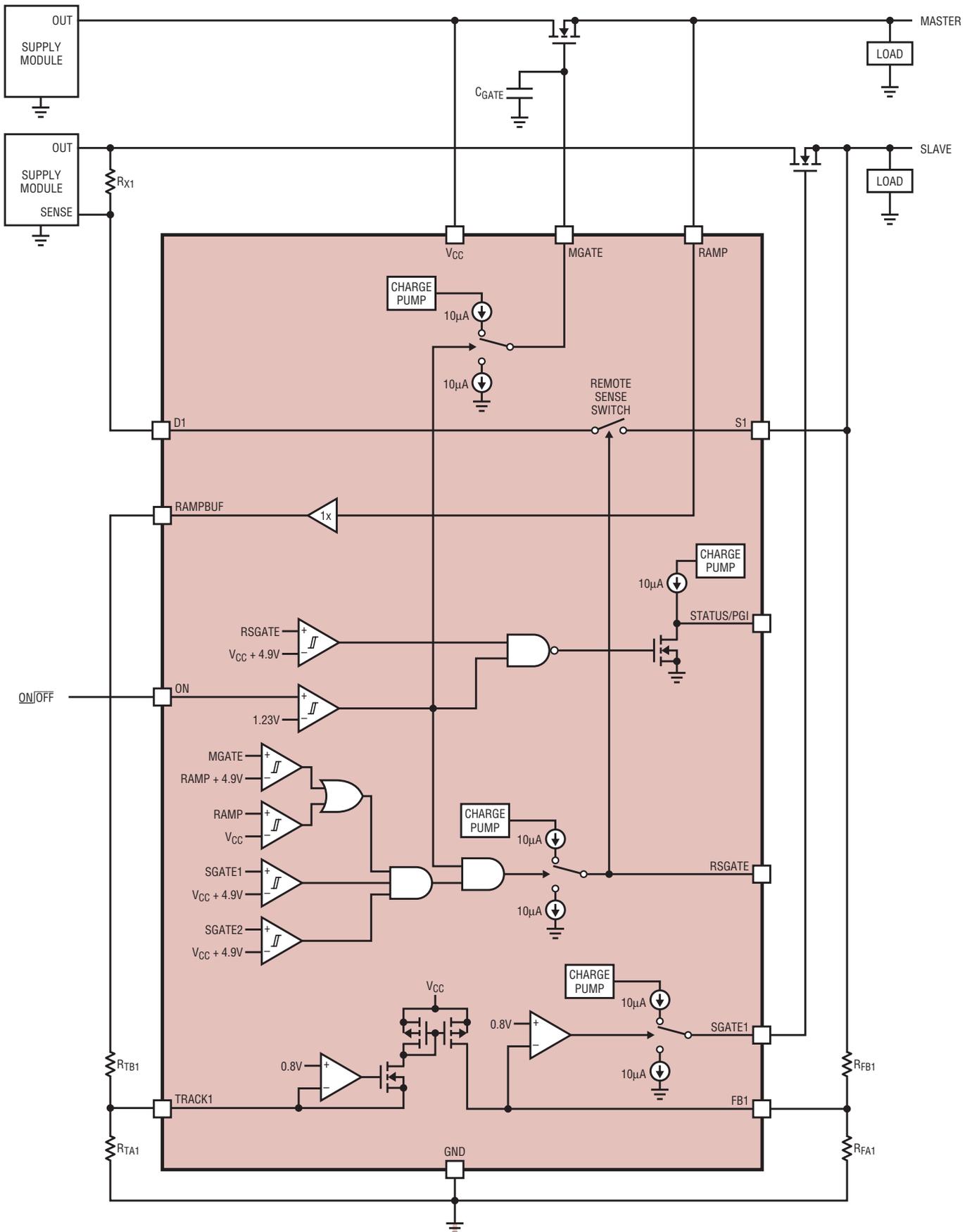
Be sure that the slave ramp rate and its offset or delay allow the slave voltage to finish ramping before the master ramp reaches its final value; otherwise, the slave supply voltage will be held below its intended level.

Finally, determine the lower track resistor,  $R_{TA}$ :

$$R_{TA} = \frac{V_{TRACK}}{\frac{V_{FB(REF)}}{R_{FB}} + \frac{V_{FB(REF)} - V_{TRACK}}{R_{FA}} - \frac{V_{TRACK}}{R_{TB}} + \frac{\Delta V}{R_{TB}}} \quad (6)$$

where  $V_{TRACK} = V_{FB(REF)} = 0.8V$

Note that large ratios of slave ramp rate to master ramp rate,  $S_S/S_M$ , may result in negative values for  $R_{TA}$ . In such cases the offset or delay must be increased, or the slave ramp rate must be reduced.



**Figure 7. Simplified functional block diagram for the LTC2926**

not equal to the generator voltage, and the feedback would send the generator voltage higher and higher attempting to equalize them.

The LTC2926 solves the voltage drop problem with automatic remote sense switching. In Figure 6, one of the two integrated N-channel MOSFET remote sense switches connects the load to the supply generator's sense input. During ramp up and ramp down, the switch is open, and resistor  $R_x$  provides local feedback to the sense input. After tracking has completed, the RSGATE signal closes the remote sense switch, and the supply generator dynamically compensate out the power MOSFET's voltage drop. The RSGATE signal is available on a pin so that additional external switches may be controlled if necessary.

**Tracking Typical Behavior: Supplies Inclined to Marry Loads; Separation on the Decline**

The operation of the LTC2926 in an application can be understood by considering the simplified block diagram with external components in Figure 7. Assume that the supply generators' outputs and the  $V_{CC}$  supply have reached their nominal values, and that the ON input is low. In that case, the STATUS/PGI pin is pulled-down, the remote sense switch is open, and the MGATE pin is pulled to ground, which means the master load is disconnected from the master supply. Track resistor  $R_{TB1}$  is grounded by the ramp buffer

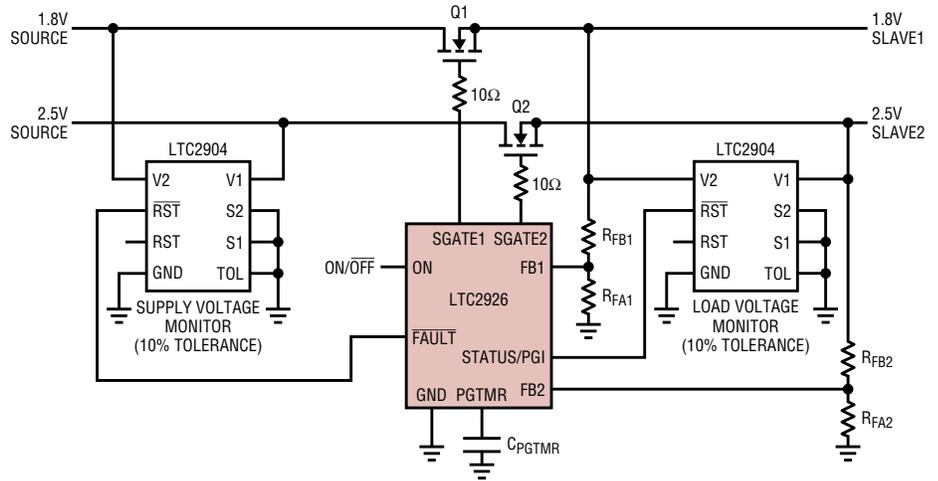


Figure 8. External monitors control the LTC2926 via I/O pins

output, so the injected feedback current (a duplicate of the track current) is at its maximum, which forces the FB1 pin voltage above 0.8V. Thus the SGATE1 pin is pulled low, so the slave supply is also disconnected.

When the ON pin voltage is brought high, the MGATE pin sources current into an external capacitor that sets the incline rate of the master ramp signal (see Figure 2). The master ramp may be used to create a master supply with the addition of an N-channel MOSFET (see Figure 3). The buffered ramp output (RAMPBUF pin) allows tracking resistors to be driven without loading the MGATE pin current, and keeps track currents from back feeding the master load. As the master ramp rises, the track current decreases, and the gate controller brings up the

slave supply voltage until it reaches the slave generator voltage, after which point the MOSFET is fully enhanced. As tracking has completed, the remote sense switch then closes, and finally the STATUS/PGI pin is asserted.

When ON is brought low, the tracking profile runs in reverse. The STATUS/PGI pull-down activates, and the RSGATE pin pulls down, which opens the remote sense switches. Next, the MGATE pin sinks current, which reduces the master (supply) ramp and slave supply voltages in reverse order. As the master and slave supplies near ground, the slave supplies (and master supply if implemented) are disconnected, which completes the ramp-down process.

**I/O an Explanation: It's My Fault That You've Separated ...**

The LTC2926 communicates with other devices in the system via the ON

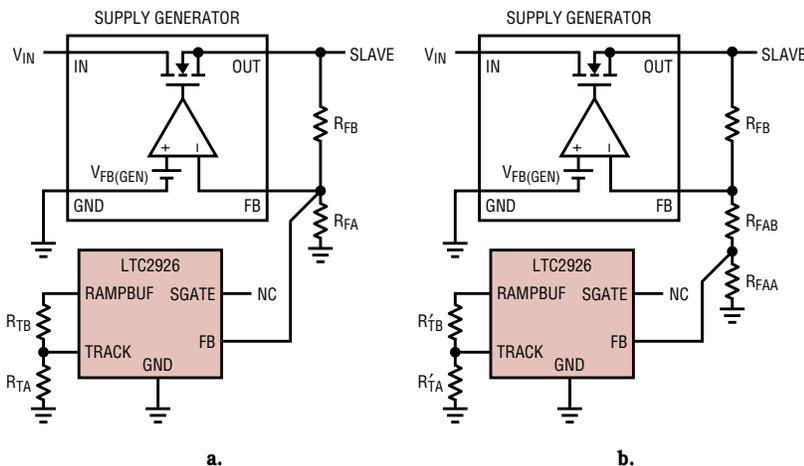


Figure 9. Slave supply control without a MOSFET (a) generator reference  $V_{FB(GEN)} \leq 0.75V$ , and (b) generator reference  $V_{FB(GEN)} > 0.75V$

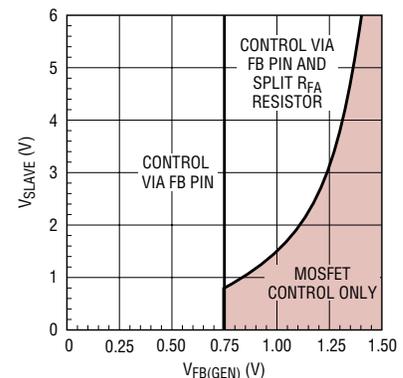


Figure 10. Regions of possible slave control without a MOSFET

input signal that initiates ramp up and ramp down, and two input/output signals,  $\overline{\text{FAULT}}$  and STATUS/PGI. Each of the two I/O signals reports an aspect of tracking status as its output, and each accepts a shut-down command as its input. Both the  $\overline{\text{FAULT}}$  and the STATUS/PGI pins include strong N-channel MOSFET pull-down transistors, and weak pull-up currents, which facilitates wired-OR signaling.

A high output at the STATUS/PGI pin indicates that tracking/sequencing and automatic remote sense switching have completed. It is typically connected to the  $\overline{\text{RST}}$  inputs of downstream devices such as an FPGA, a micro-controller, or a load voltage monitor (Figure 9). The weak pull-up hangs from a charge-pumped rail, which allows the STATUS/PGI output to control external MOSFET switches, as well as become a logic signal with the addition of a pull-up resistor.

The input function of the STATUS/PGI pin allows downstream devices and the LTC2926 itself to force open the remote sense switches and bring about supply disconnect if the pin voltage is low and the power good timeout period has expired. The MGATE, SGATE1, SGATE2, and RSGATE pins that control MOSFET gates are all pulled low to effect immediate supply disconnect and open the remote sense switches. In addition, an internal fault latch is set, which keeps the loads cut off until it is reset and re-armed via the ON pin. When connected as in Figure 8, the LTC2904 supply monitor forces supply disconnect if the programmed 10% load voltage tolerance is exceeded after the timeout period (set by  $C_{\text{TIMER}}$ ) expires.

The  $\overline{\text{FAULT}}$  pin's input aspect allows upstream devices to set the fault latch, open the remote sense switches, and cause supply disconnect without a timeout period when the pin is pulled low. In addition, the STATUS/PGI pull-down is activated, which informs downstream devices of the fault. Under normal conditions, a weak pull-up keeps the  $\overline{\text{FAULT}}$  pin voltage within a diode drop of  $V_{\text{CC}}$ —the internal Schottky diode allows the pin to be pulled above  $V_{\text{CC}}$  safely. Again,

the loads remain cut off until the fault latch is reset and re-armed by toggling the ON pin. The  $\overline{\text{FAULT}}$  pin might typically be connected to the  $\overline{\text{RST}}$  output of upstream supply devices such as voltage, current, or temperature monitors (Figure 8). Automatic fault retry is possible by tying the ON and  $\overline{\text{FAULT}}$  pins together.

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***MOSFET-controlled tracking and sequencing can improve power system segmenting and allow reuse, which reduces parts count and board area. A single-output supply generator can power different rails of the same voltage (e.g., analog power, digital power, and housekeeping power) because each rail's tracking profile can be set independently.***

---

### **Direct Supply Generator Control: ¡No Más FETs, Mi Amigo!**

The LTC2926 can even set a tracking profile without MOSFETs just like the LTC2923, under certain conditions. As is the case for no-MOSFET tracking with the LTC2923 family, the supply generator must allow access to the feedback node that sets its output voltage, and its reference voltage must be ground-based. (MOSFET control is required for many three-terminal regulators, for example, because their references are relative to their output node.)

For tracking control when the slave generator's reference voltage is low enough,  $V_{\text{FB(GEN)}} \leq 0.75$ , simply connect the LTC2926's FB pin to the supply generator's FB pin (Figure 9a). Choose the track resistors based on the tracking profile and the generator's feedback resistors. When the master ramp signal is low, the tracking current is high, and it keeps the slave generator's output low. When the master ramp signal reaches its maximum, the LTC2926's FB pin current is zero, and it has no effect on the output

voltage accuracy, transient response, or stability of the generator.

A generator with  $V_{\text{FB(GEN)}} > 0.75\text{V}$  may be controlled without a MOSFET if the slave voltage is large enough; see Figure 10. The  $R_{\text{TA}}$  resistor must be split to create a new injection point for FB pin current, and the track resistor values must be scaled, as well (Figure 9b); consult the LTC2926 Data Sheet for details.

### **Conclusion: No Joke, It's a Great Product**

The LTC2926 solves a host of tracking and sequencing headaches and can simplify design by means of MOSFET control. MOSFET control separates supply generator start-up and shut-down details from specific tracking profile requirements, which allows for supply segmenting and generator consolidation. Because the LTC2926 creates its own regulator to ramp the rails, a multitude of supply generators can now be tracked and sequenced, including modules and 3-terminal linear regulators.

The LTC2926 is interoperable with Linear's no-MOSFET tracker/sequencers, and even provides that functionality itself, which can keep device count down and reduce parts assortment. Its integrated automatic remote sense switching eliminates a problem associated with series MOSFET control, and intelligent I/O lets this device broadcast status as well take shut-down commands from upstream and downstream devices. All of these features and fine control of start-up and shut-down of power supply rails in a single package make the LTC2926 powerful solution for tracking and sequencing. 

**For further information on any of the devices mentioned in this issue of *Linear Technology*, use the reader service card or call the LTC literature service number:**

**1-800-4-LINEAR**

**Ask for the pertinent data sheets and Application Notes.**

# High Voltage Boost/LED Controller Provides 3000:1 PWM Dimming Ratio

by Eugene Cheung

## Performance, Accuracy, Versatility: LEDs and Beyond

The LTC3783 is a current-mode boost controller optimized for constant-current True Color PWM™ dimming of high-powered LEDs. Proprietary techniques provide extremely fast, true PWM load switching with no transient undervoltage or overvoltage issues. High dimming ratios of 3000:1 (at 100Hz), important for such applications as video projectors and LCD backlights, can be achieved digitally, maintaining the color integrity of white and RGB LEDs. The LTC3783 also provides an analog input for an additional 100:1 dimming (300,000:1 total).

This versatile part can also be used in a boost, buck, buck-boost, SEPIC, or flyback converter, and as a constant-current, constant-voltage regulator. No  $R_{SENSE}$ ™ operation uses a MOSFET's on-resistance to eliminate the current-sense resistor, increasing efficiency. Applications for the LTC3783 include high voltage LED arrays and LED backlighting, as well as voltage regulators in telecom, automotive, and industrial control systems.

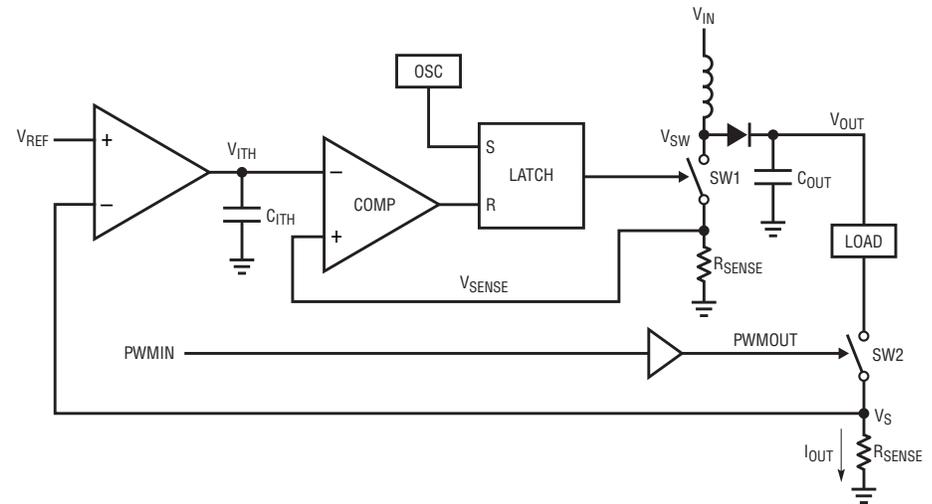


Figure 1. Simplified conventional boost converter with PWM dimming

The LTC3783 operates from input supplies ranging from 3V to 36V, and provides output overvoltage protection while regulating output current. When a sense resistor is used, the maximum output voltage is limited only by external components. The controller includes integrated drivers for power and PWM MOSFET switches, and a variable feedback voltage (0V to 1.23V) allows the designer full control over load current accuracy vs efficiency. These features make the part especially attractive for higher-power

LED lighting applications. One resistor sets operating frequency from 20kHz to 1MHz, and, to reduce switching noise interference, the LTC3783 is synchronizable to an external clock. Programmable soft start limits inrush current during startup, preventing input current spikes. In addition to boost operation ( $V_{OUT} > V_{IN}$ ), the controller offers an alternate constant-current, constant-voltage operating mode for buck-boost or buck applications. In these cases, the achievable PWM dimming ratios are generally lower.

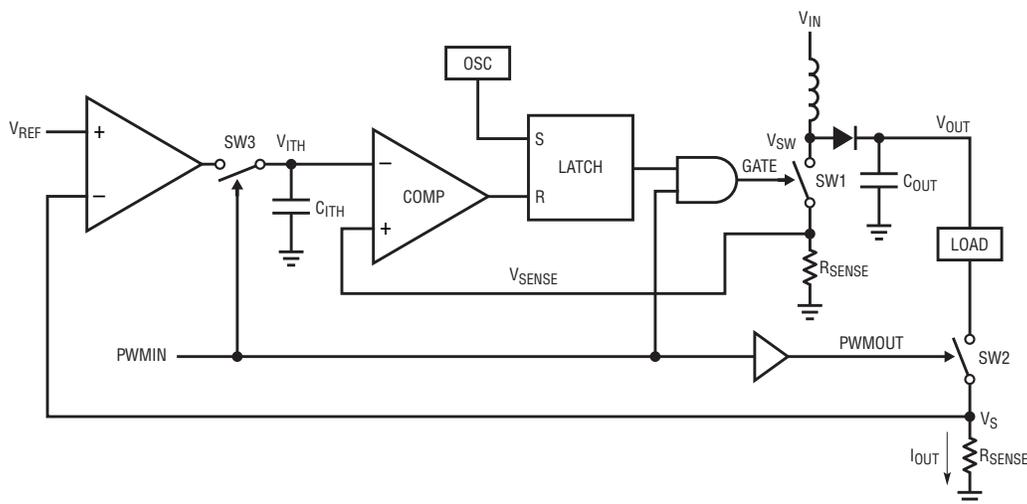


Figure 2. Simplified boost converter with True Color PWM dimming



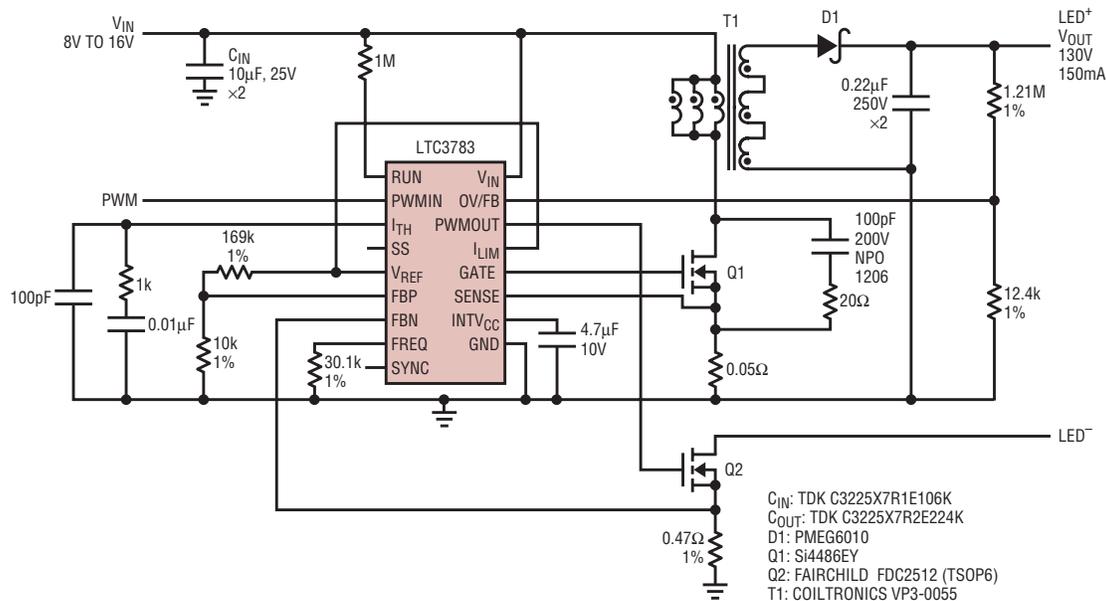


Figure 5. PWM-dimmed flyback LED application

resistor, as compared to 430mW for a 1.23V sense voltage. A worst-case  $V_{FB}$  offset of <3mV ensures better than 3% load current accuracy as well. Additional analog dimming could be accomplished by replacing  $R_1$  and  $R_2$  with a potentiometer or other variable voltage source.

Resistor  $R_T$  on the  $FREQ$  pin determines  $GATE$  switching frequency. The 6.04k $\Omega$  value chosen sets the system up for 1MHz switching, which permits a higher PWM dimming ratio than the standard 300kHz switching frequency allows. In case the LEDs are disconnected while the supply is running, resistors  $R_3$  and  $R_4$  set the maximum output overvoltage shutdown threshold, nominally at  $V_{OV/FB} = 1.32V$ . Overvoltage protection is essential in current-source boost applications because with an open-load fault, capacitor and FET drain voltages can easily exceed maximum device ratings.

Because of the True Color PWM topology, and the 1MHz clock rate, this boost application circuit can achieve a PWM dimming ratio in excess of 3000:1.

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### Buck-Boost PWM LED Driver

In some LED applications, the desired  $V_{IN}$  and  $V_{OUT}$  overlap, thus requiring buck-boost or SEPIC functionality. Figure 4 depicts such a system. In this setup, LED current is returned to  $V_{IN}$ , and the LEDs actually see a voltage of  $V_{OUT} - V_{IN}$ , allowing a nominally boost configuration to function as a buck-boost. In contrast, a SEPIC configuration would require a 2-inductor- or transformer-based solution, resulting in increased complexity and lower efficiency. However, a true SEPIC would also provide for a grounded load, which may be desirable in some applications.

In this mode, PWM dimming is available through the PWM input, albeit not at a dimming ratio comparable to the one in the boost configuration. Lack of a PWMOUT-controlled load switch means transient response cannot be as rapid, since the output voltage is then allowed to sag when PWMIN is low, necessitating some recovery period when PWMIN goes high again.

The  $I_{LIM}$  pin provides analog dimming, as the  $I_{LIM}$  range ( $0.12V < V_{ILIM} < 1.23V$ ) controls the  $(V_{FBP} - V_{FBN})$  differential proportionally from 10mV to 100mV. This allows the LED current to be linearly varied by an additional 10:1 ratio.

### High Voltage (130V OVP) Flyback LED Driver

The 130V application shown in Figure 5 is similar to that of Figure 3, but because of the extremely high boost ratio, a 3:1 transformer is added in order to reduce the  $GATE$  duty cycle such that the part's maximum duty cycle is not violated.

This circuit is capable of driving a string of LEDs at 150mA, which can add up to less than 130V total forward voltage, at which point the  $OV/FB$  pin is activated to stop all switching. This prevents a potential overvoltage condition at the output.

As presented, the application circuit can provide a PWM dimming ratio of 500:1.

### Other Functionality

In the 130V application above, because  $V_{FBP} > 2.5V$ , the LTC3783 is in constant-current, constant-voltage operation, meaning the control loop seeks to regulate the load sense resistor voltage ( $V_{FBP} - V_{FBN}$ ) at 100mV. This is distinct from the pure voltage mode of the boost application, in which  $V_{FBP} = V_{FBN}$ . Also, in constant-current, constant-voltage mode the  $OV/FB$  pin becomes a linear feedback input, which regulates  $V_{OV/FB}$  at 1.23V if  $(V_{FBP} - V_{FBN}) < 100mV$ . 

# 3A Monolithic Buck Regulator in 4mm × 4mm QFN

by Theo Phillips

## Introduction

The LTC3412A is much more than a drop-in replacement for the popular LTC3412 monolithic buck switching regulator. Though still offered in a thermally enhanced 16-lead TSSOP, the LTC3412A is also squeezed into a smaller footprint 4mm × 4mm QFN, reducing the package height to 0.75mm from 1.1mm. At the same time, the maximum load current has risen to 3A from the LTC3412's 2.5A, and the minimum input voltage has been pared down to 2.25V from the earlier 2.625V. The LTC3412A can still deliver efficiency as high as 95%, accept input voltages up to 5.5V, and switch at frequencies up to 4MHz, making it a compact and efficient solution for portable electronics that require low supply voltages (down to 0.8V) converted from typical battery voltages.

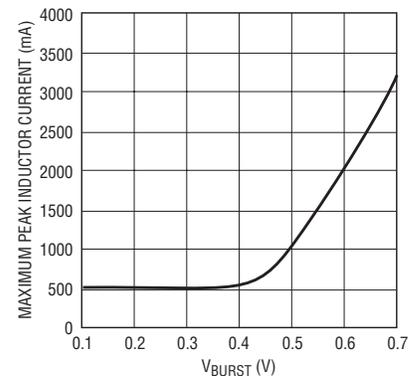
Like its predecessor, the LTC3412A employs a constant frequency, current-mode architecture. The switching frequency can be set between 300kHz and 4MHz by an external resistor, or

each switching cycle can commence with the falling edge of an external clock signal fed into the Sync/Mode pin. The LTC3412A's high switching frequency permits the designer to use tiny, low value inductors while holding output voltage ripple to a minimum.

## Choice of Operating Modes

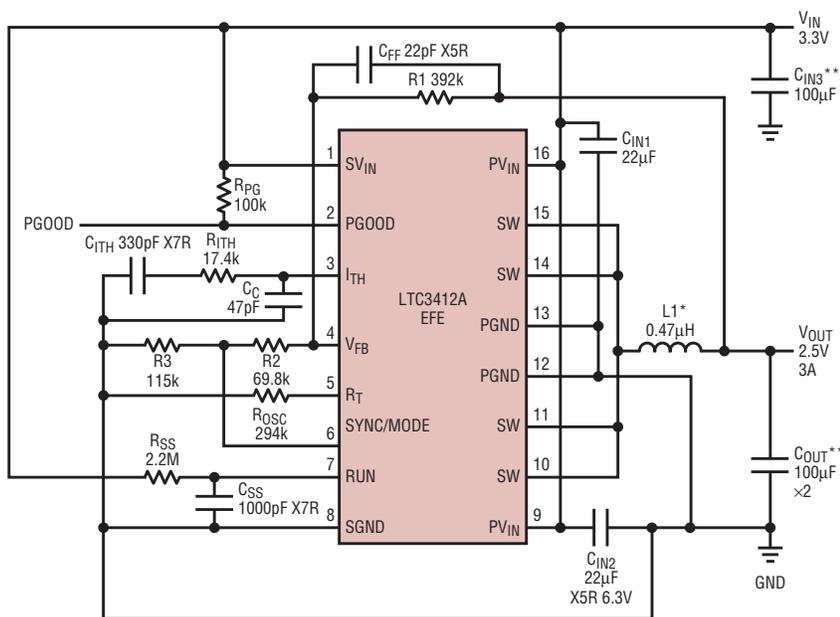
The LTC3412A can be configured for Burst Mode operation, forced continuous operation, or pulse skipping. In mobile applications where battery life is of paramount importance, Burst Mode operation boosts efficiency by reducing gate charge losses at light loads, and so reducing supply current to just 64μA at no load. Forced continuous operation switches at constant frequency regardless of load current; this simplifies filtering of the switch noise. Pulse skip mode provides a good compromise between light load efficiency and output voltage ripple.

During Burst Mode operation, switching cycles are skipped during light loads to reduce switching losses. The LTC3412A provides for external



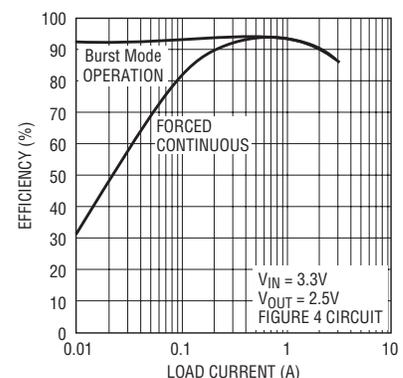
**Figure 1.** By tying the Sync/Mode pin to a point on the feedback voltage divider, as in Figure 2, the designer can freely adjust the peak current of the bursts (See Figure 4).

control of these cycles' peak current (the burst clamp level) by varying the DC voltage at the Sync/Mode pin within a 0V–1V range. Figure 1 shows the relationship between this DC voltage (which is generally tapped off of the feedback resistor network) and the burst clamp level. Higher peak currents deliver more energy, so fewer bursts are required to maintain the output voltage. If the minimum peak inductor current delivers more energy than the load current demands, the control loop causes the internal power switches to skip more cycles. Lower burst frequencies can improve efficiency at light load, at the expense



\*VISHAY IHL P-2525CZ-01  
\*\*TDK 4532X5R0J107M

**Figure 2.** A 2.5V, 4A step-down regulator in Burst Mode operation



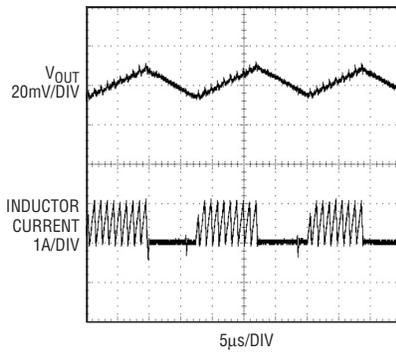
**Figure 3.** Efficiency vs load current for the circuit of Figure 2,  $V_{IN} = 3.3V$ ,  $V_{OUT} = 2.5V$  (Burst Mode operation). If Sync/Mode were tied to ground, the efficiency would be lower (pulse skip mode), but output voltage ripple would be greatly reduced.

of a slight increase in output voltage ripple. Conversely, lowering the minimum peak inductor current increases the burst frequency and reduces the output voltage ripple.

Burst Mode operation dissipates minimal power in light load applications, but sometimes noise suppression takes priority over efficiency. To reduce noise and RF interference, the LTC3412A can be set up for forced continuous operation by connecting the Sync/Mode pin to the Signal Input Voltage pin. This mode maintains a constant switching frequency regardless of output load, dovetailing with noise sensitive applications in which it is necessary to avoid switching harmonics in a particular signal band.

In pulse skip mode, the burst clamp is set to zero current, which limits the minimum peak inductor current to a level set by the minimum on-time of the control loop. Pulse skip mode is implemented by connecting the Sync/Mode pin to GND. Pulse skipping has lower ripple than Burst Mode operation and has better light-load efficiency than forced continuous mode.

As the battery voltage decreases toward the output voltage, the duty cycle and the on-time increase. Fur-



**Figure 4. Burst Mode operation, showing output voltage ripple associated with bursts of inductor current. The peak currents are held to 1.1A because the Sync/Mode voltage is set to 0.49V.**

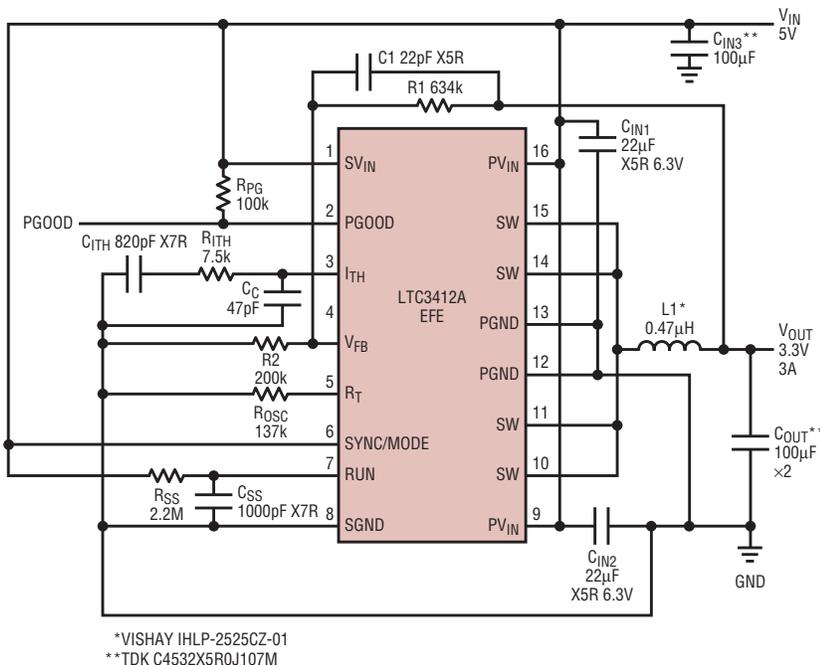
***The LTC3412A can deliver efficiency as high as 95%, accept input voltages up to 5.5V, and switch at frequencies up to 4MHz, making it a compact and efficient solution for portable electronics that require low supply voltages (down to 0.8V) converted from typical battery voltages.***

ther reduction in the battery voltage forces the internal P-channel MOSFET to remain on for more than one cycle, and ultimately to remain on 100% of the time. This dropout state extends the useful operating input voltage over the run-time of the battery. Output voltage simply follows the input voltage as the battery continues to discharge, reduced by drops across the inductor and P-channel MOSFET.

**A High Efficiency 2.5V, 3A Step-Down Regulator with All Ceramic Capacitors**

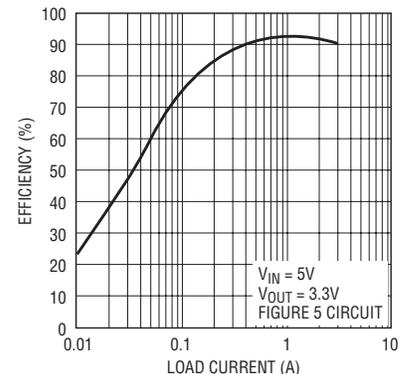
Figure 2 shows a 2.5V step-down DC/DC converter that is configured for Burst Mode operation. This circuit provides a regulated 2.5V output at up to 3A from a 3.3V input. Figure 3 shows that efficiency peaks at 94%, and remains high across the load spectrum. The measured output voltage ripple is around 25mV<sub>P-P</sub> at loads from 10mA to 200mA, and drops to around 5mV at heavier loads. Lower ripple (5mV–10mV) can be maintained at the lightest loads with pulse skip mode, with some sacrifice in light load efficiency. The switching frequency for this circuit is set at 1MHz by a single external resistor, R<sub>OSC</sub>. Operating at frequencies this high allows the use of a low value (and physically small) inductor.

In this application, Burst Mode operation maintains the high efficiency at light loads. This powers down the majority of the internal circuitry during the intervals between switching cycles. The peak inductor current is set by the R2-R3 voltage divider, which generates

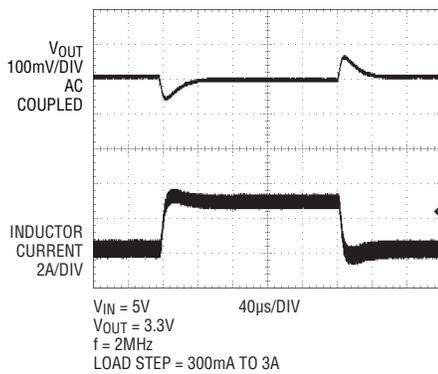


\*VISHAY IHLP-2525CZ-01  
\*\*TDK C4532X5R0J107M

**Figure 5. A 2MHz regulator, 5V to 3.3V at 3A, operating in forced continuous mode**



**Figure 6. Efficiency of the circuit in Figure 5 reaches well into the 90s at moderate loads.**



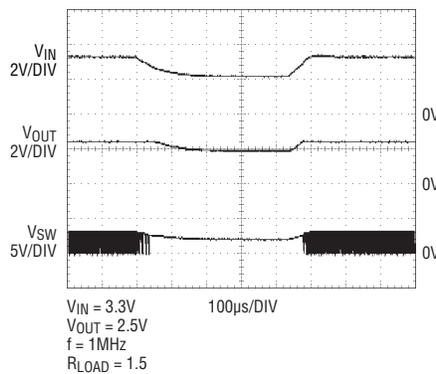
**Figure 7.** The circuit of Figure 5 delivers a clean transient response when the load is stepped from 300mA to 3A.

a 0.49V reference at the Sync/Mode pin. This corresponds to approximately 1.1A minimum peak inductor current, as shown in Figure 1.

Figure 4 illustrates how Burst Mode operation produces a burst of inductor current pulses that are repeated periodically. Each inductor current pulse increases to approximately 1.1A during each switching period before the main power MOSFET is shut off. The process repeats for multiple switching cycles until the charge on the output capacitor is refreshed. Once this is accomplished, both the main and synchronous power MOSFETs are held off while the load current is supplied solely by the charge on the output capacitor. This sleep state continues until the output voltage drops low enough to initiate another burst cycle. Varying the voltage on the Sync/Mode pin affects the amplitude of the group of current bursts as well as the frequency at which they are repeated.

## 2MHz, High Efficiency 3.3V, 3A Step-Down Regulator with All Ceramic Capacitors

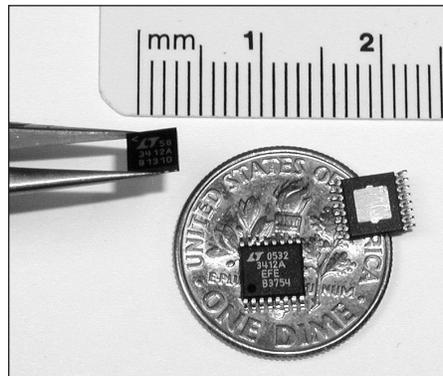
Figure 5 shows a 3.3V step-down DC/DC converter using all ceramic capacitors. Switching at 2MHz, this circuit provides a regulated 3.3V output at up to 3A from a 5V input voltage. This converter is an ideal choice for opera-



**Figure 8.** If the circuit of Figure 2 experiences a dip in  $V_{IN}$ , a regulated output is maintained until the LTC3412A goes smoothly into dropout. Below that level,  $V_{OUT}$  follows  $V_{IN}$  anywhere above the undervoltage lockout. For output voltages programmed below the UVLO, the LTC3412A can maintain its output voltage even when the input sinks to 2.25V.

tion near an AM radio receiver, since it operates above the broadcast band and the switch noise can be filtered in a predictable manner. Efficiency for this circuit, shown in Figure 6, is as high as 95% at moderate loads.

Ceramic capacitors offer low cost and low ESR, but many switching regulators have difficulty operating with them because the extremely low ESR can lead to loop instability. The phase margin of the control loop can drop to inadequate levels without the aid of the zero that is normally generated from the higher ESR of tantalum, niobium, or special polymer capacitors. The LTC3412A, however, includes OPTI-LOOP compensation, which allows it to operate properly with ceramic input



**Figure 9.** The LTC3412A is offered in two thermally enhanced packages: the 16-lead TSSOP (both sides shown) and the ultra-thin 4mm x 4mm QFN (shown in tweezers).

and output capacitors. The LTC3412A allows loop stability to be achieved through a wide range of loads and output capacitors with proper selection of compensation components on the  $I_{TH}$  pin. Figure 7 shows the stable transient response associated with the circuit of Figure 5.

## Lower Minimum Input Voltage

Sagging input voltages are handled well by the LTC3412A. Figure 8 shows the response of  $V_{OUT}$  to a substantial hit to  $V_{IN}$ . Until  $V_{IN}$  drops to  $V_{OUT}$ , the effect on  $V_{OUT}$  is negligible; below that point the P-channel FET turns on 100% of the time (dropout), and  $V_{OUT}$  follows  $V_{IN}$  right down to the guaranteed 2.25V undervoltage lockout. Output voltages set below the UVLO can be maintained while maximizing battery life, or where input rails are just loosely regulated.

## Conclusion

The LTC3412A is a monolithic, synchronous step-down DC/DC converter that is well suited for applications requiring up to 3A of output current. OPTI-LOOP compensation allows diverse transient responses to be optimized with ceramic capacitors. For excellent thermal handling, the LTC3412A is offered in two tiny packages, each with an exposed pad to facilitate heat sinking (Figure 9). Its high switching frequency, low undervoltage lockout and internal low  $R_{DS(ON)}$  power switches make the LTC3412A an excellent choice for compact, high efficiency power supplies. 

For further information on any of the devices mentioned in this issue of *Linear Technology*, use the reader service card or call the LTC literature service number:

1-800-4-LINEAR

Ask for the pertinent data sheets and Application Notes.

# 3A Converter Drives LEDs with 500:1 Dimming

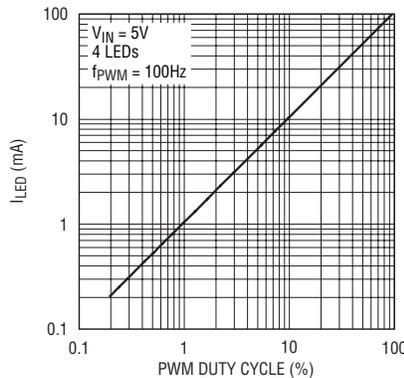
by Jaino Parasseril

## Introduction

For LED applications where a wide dimming range is required, two competing methods are available: analog dimming and PWM dimming. The easiest method is to simply vary the DC current through the LED—analog dimming—but changing LED current also changes its chromaticity (color shift), undesirable in many applications (such as LCD backlights).

The better method is PWM dimming, which switches the LED on and off, using the duty cycle to control the average current. PWM dimming offers several advantages over analog dimming and is the method preferred by LED manufacturers. By modulating the duty cycle of the PWM signal, the average LED current changes proportionally as illustrated in Figure 1. The chromaticity of the LEDs remains unchanged in this scheme since the LED current is either zero or at programmed current. Another advantage of PWM dimming over analog dimming is that a wider dimming range is possible.

The LT3477 is a 3A DC/DC converter that is ideally suited for LED applications. For the LT3477, analog dimming offers a dimming ratio of about 10:1; whereas, PWM dimming



**Figure 1. The average LED current changes proportionally with PWM duty cycle. Many LED manufacturers specify PWM dimming because it offers wider dimming ranges and better LED performance than analog dimming.**

with the addition of a few external components results in a wider dimming range of 500:1. The technique requires a PWM logic signal applied to the gate of both NMOS transistors (refer to Figure 2). When the PWM signal is taken high the part runs in normal operation and  $I_{LED}$  of 100mA runs through the LEDs. When the PWM input is taken low the LEDs are disconnected and turn off. This unique external circuitry produces a fast rise time for the LED current (see

**PWM dimming offers several advantages over analog dimming and is the method preferred by LED manufacturers. With PWM dimming, the chromaticity of the LEDs remains unchanged and a wider dimming range is possible.**

Figure 3), resulting in a wide dimming range of 500:1 at a PWM frequency of 100Hz.

The LED current can be controlled by feeding a PWM signal with a broad range of frequencies. Dimming below 80Hz is possible but not desirable due to perceptible flashing of LEDs at lower frequencies. The LED current can be controlled at higher frequencies, but the dimming range decreases with increasing PWM frequency.

In high temperature applications, the leakage of the Schottky diode D1 increases, which in turn, discharges the output capacitor during the PWM “off” time. This results in a smaller

### DESIGN IDEAS

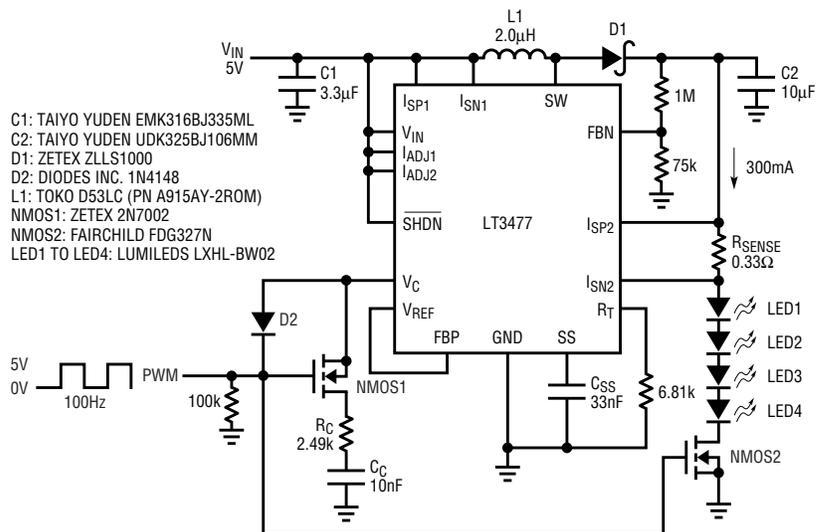
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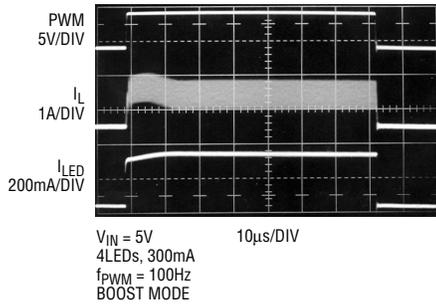
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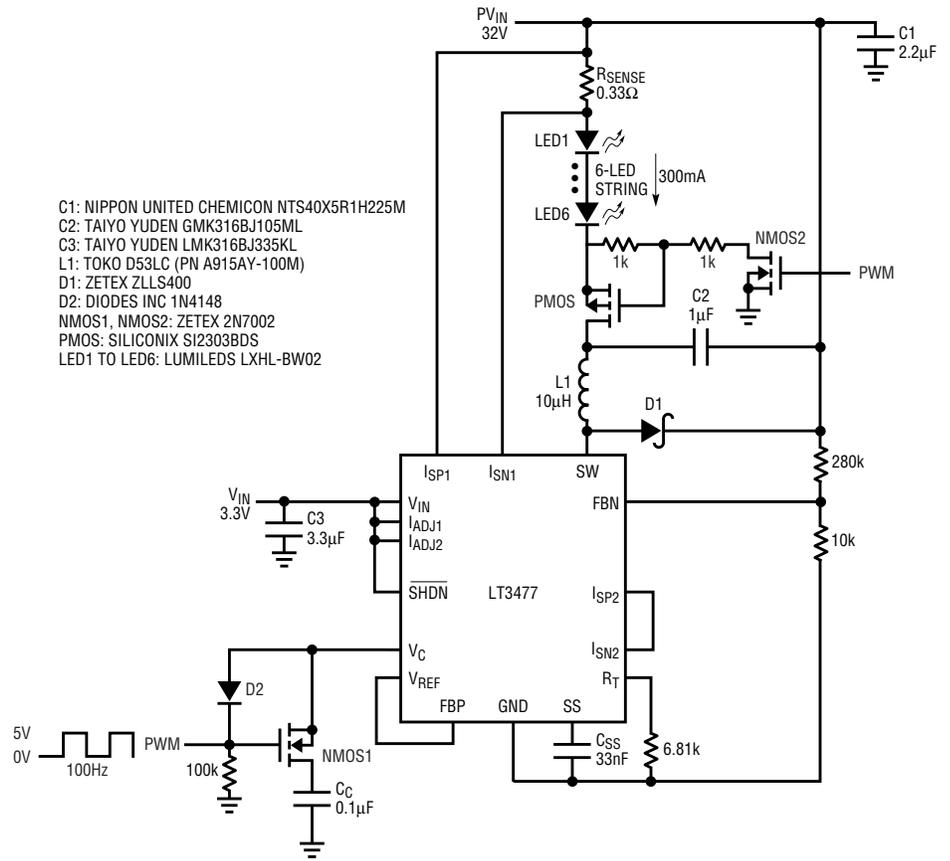
**Figure 2. A 5V input drives four white LEDs in boost mode with PWM dimming**



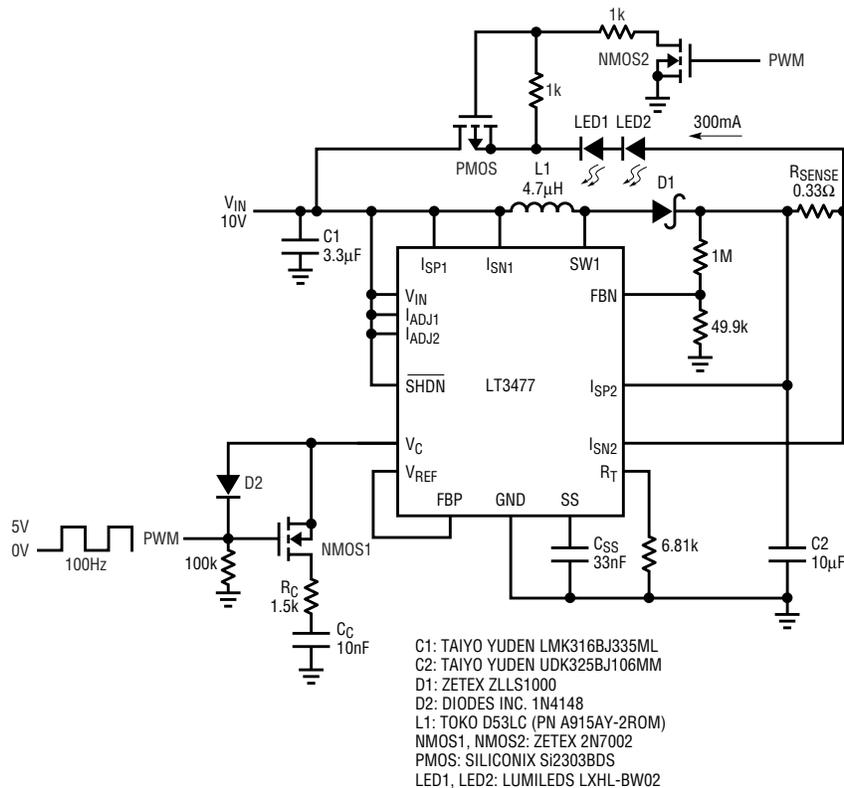
**Figure 3.** Rising LED current for the circuit in Figure 2 settles in under 20 $\mu$ s, thus allowing short pulse widths, and high dimming ratios.

effective LED dimming ratio. Consequently, the dimming range decreases to about 200:1 at 85°C.

PWM dimming can be used in boost mode (Figure 2), buck mode (Figure 4) and buck-boost mode (Figure 5). For the typical boost topology, efficiency exceeds 80%. Buck mode can be used to increase the power handling capability for higher current LED applications. A buck-boost LED driver works best in applications where the input voltage fluctuates to higher or lower than the total LED voltage drop.



**Figure 4.** Buck mode converter drives six white LEDs with PWM dimming from a 32V input



**Figure 5.** Buck-boost mode converter drives two white LEDs with PWM dimming from a 10V input

# 40nV<sub>p-p</sub> Noise, 0.05μV/°C Drift, Chopped FET Amplifier

by Jim Williams

Figure 1's circuit combines the 5V rail-to-rail performance of the LTC6241 with a pair of extremely low noise JFETs configured in a chopper based carrier modulation scheme to achieve extraordinarily low noise and DC drift. This circuit's performance suits the demanding transducer signal conditioning situations such as high resolution scales and magnetic search coils.

The LTC1799's output is divided down to form a 2-phase 925Hz square wave clock. This frequency, harmonically unrelated to 60Hz, provides excellent immunity to harmonic beating or mixing effects which could cause instabilities. S1 and S2 receive complementary drive, causing the A1-based stage to see a chopped version of the input voltage. A1's square wave output is synchronously demodulated by S3 and S4. Because these switches

are synchronously driven with the input chopper, proper amplitude and polarity information is presented to DC output amplifier A2. This stage integrates the square wave into a DC voltage, providing the output. The output is divided down (R2 and R1) and fed back to the input chopper where it serves as a zero signal reference. Gain, in this case 1000, is set by the

R1-R2 ratio. Because the input stage is AC coupled, its DC errors do not affect overall circuit characteristics, resulting in the extremely low offset and drift noted.

Figure 2, noise measured over a 50 second interval, shows 40nV in a 0.1Hz to 10Hz bandwidth. This low noise is attributed to the input JFET's die size and current density. 

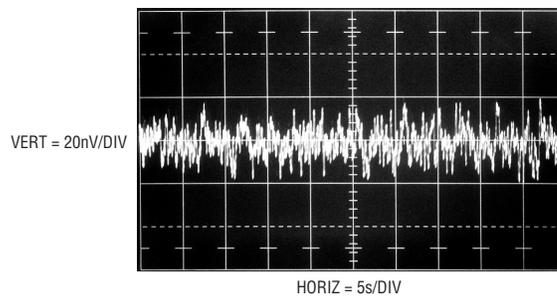


Figure 2. Noise measures 40nV<sub>p-p</sub> in 50s sample period

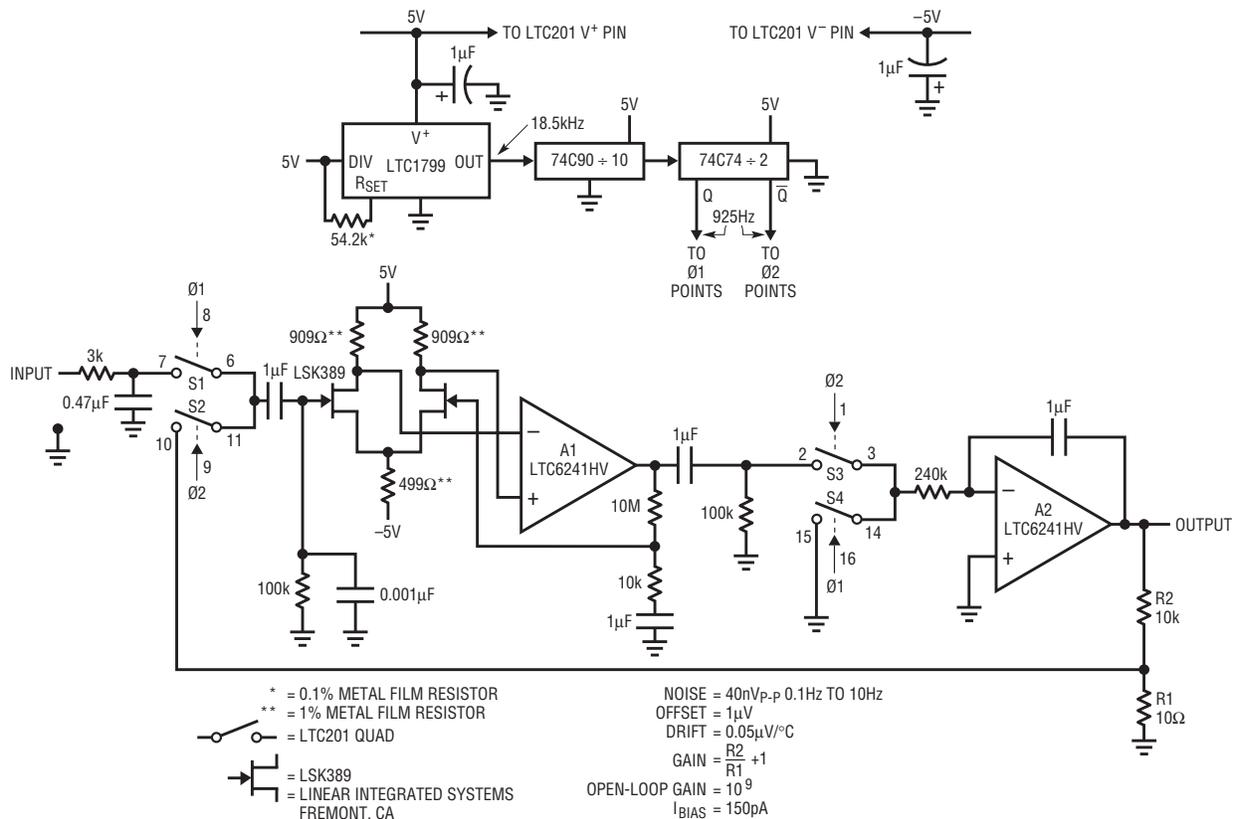


Figure 1. 40nV noise chopper amplifier

# SC70 LED Driver Drives Six White LEDs from a Single Li-Ion Battery

by Mayur Kenia

## Introduction

The highly integrated LT3491 provides a compact, simple solution for driving backlight circuits in battery-powered portable devices, such as cellular phones, PDAs, and portable GPS devices. It features internal compensation, open-LED protection, a 32V power switch and a 32V Schottky diode all inside a tiny SC70 package.

Specifically, the LT3491 is a fixed frequency step-up DC/DC converter that drives up to six white LEDs in series from a Li-Ion cell. Series connection of the LEDs provides identical LED currents resulting in uniform brightness without the need for ballast resistors. In addition, the 2.3MHz switching frequency allows the use of tiny inductors and capacitors.

Figure 1 shows how easy it is to drive six white LEDs from a Li-Ion battery. Figure 2 shows the efficiency of the six white LED application circuit.

## High Side Sense

The LT3491 features a unique high side LED current sense that enables the part to function as a “one wire” current source—one side of the LED string can be returned to ground anywhere, allowing a simpler “one wire” LED connection. Traditional LED drivers use a grounded resistor to sense LED current requiring a 2-wire connection to the LED string. High

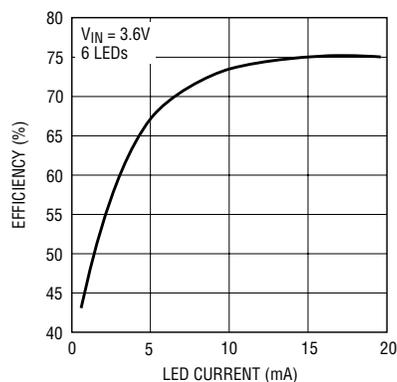


Figure 2. Efficiency of the circuit in Figure 1

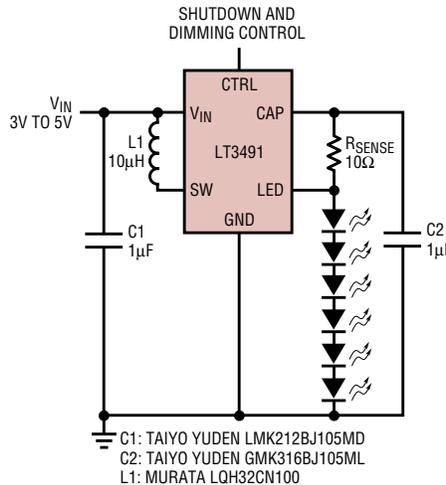


Figure 1. Li-Ion powered driver for six white LEDs

side sense moves the sense resistor to the top of the LED string.

Figure 3 shows the advantage of high side sense in a cell phone where the LEDs are placed some distance away from the driver. The technique eliminates the return wire thereby reducing the number of wires running through the hinge. Also, it allows the LEDs to be placed further away from the converter without compromising performance.

## Dimming & Shutdown Control

A single pin performs both shutdown and accurate LED dimming control. The dimming range of the part extends

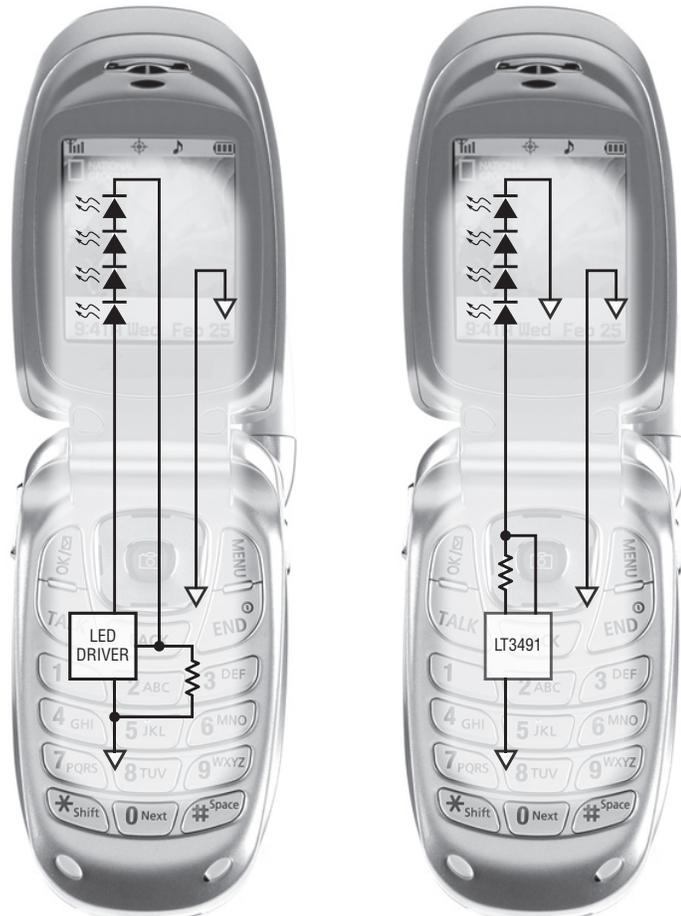
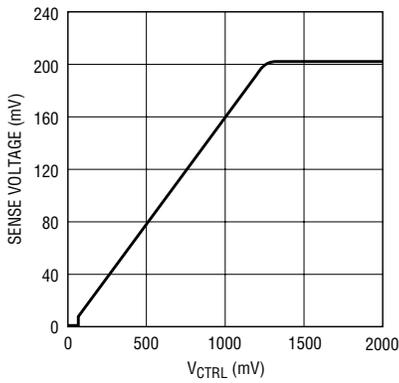


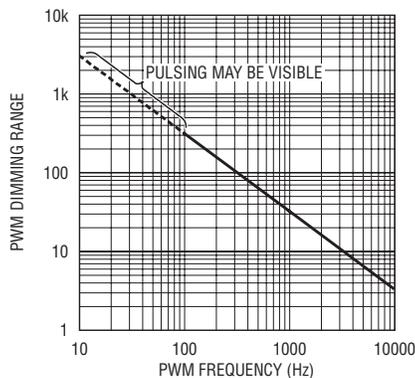
Figure 3. Traditional sense (left) and high side sense (right) implemented solutions in a cell phone. The high side solution reduces the number of connections through the hinge.



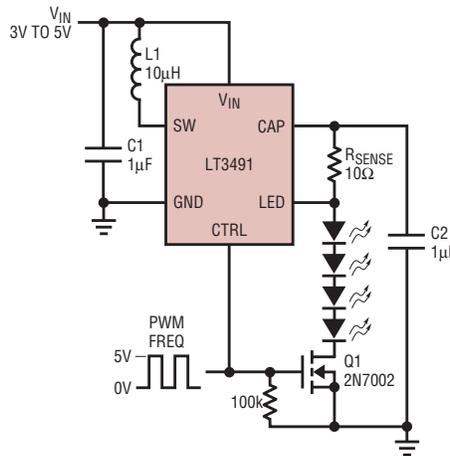
**Figure 4. LED sense voltage versus CTRL pin voltage**

from 1.5V at the CTRL pin for full LED current down to 100mV. The CTRL pin directly controls the regulated sense voltage across the sense resistor that sets the LED current. Figure 4 shows the regulated sense voltage versus CTRL pin voltage.

In addition to using a DC voltage at the CTRL pin, either a filtered PWM signal or a direct PWM signal can be used to control the LED current. Direct PWM dimming achieves wider dimming compared to using a filtered PWM or a DC voltage. Direct PWM dimming uses a MOSFET in series with the LED string to quickly connect and disconnect the LED string. Figure 5 presents direct PWM dimming in a Li-Ion to four white LED application. The PWM signal controls both the turn on and turn off of the part through the CTRL pin and the MOSFET. Figure 6 shows the linearity of PWM dimming. The available dimming range depends on the settling time of the application



**Figure 7. Dimming range vs frequency**



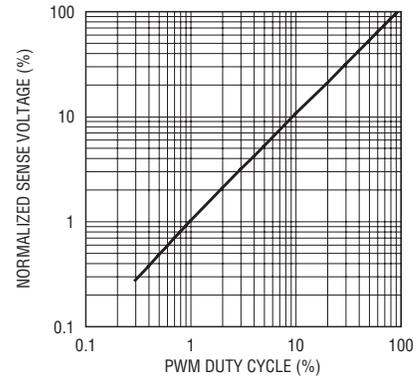
**Figure 5. Li-Ion to four white LEDs with direct PWM dimming.**

and the PWM frequency used. The application in Figure 5 achieves a dimming range of 300:1 using a 100Hz PWM frequency. Figure 7 shows the available dimming range for different PWM frequencies.

### Torch and Flash Mode LED Control

White LEDs are quickly gaining popularity as the illumination source for camera phones. White LEDs provide a simple compact solution for flash and torch lighting in cell phone applications. The LT3491 provides a small overall solution to flash and torch control.

Torch and flash applications typically use a single high power white LED. The LED driver cannot be setup

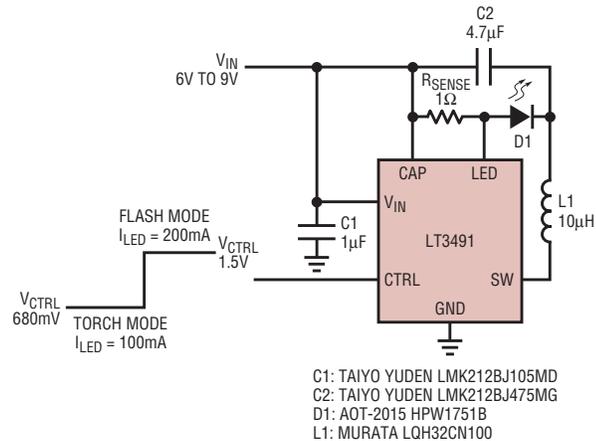


**Figure 6. Linearity of PWM dimming for a 100Hz PWM frequency and the application of Figure 5**

as a boost because the input voltage in camera phones is very close to, if not higher, than the forward voltage of the LED. A higher input voltage creates a DC path to ground that will drain the battery. High side sensing allows the LT3491 to drive a single LED from higher inputs, thus avoiding this problem. Figure 8 shows the application circuit for torch and flash control powered from two Li-Ion cells. The voltage at the control pin can be moved between two DC levels to toggle between torch and flash operation.

### Conclusion

The LT3491 provides a highly integrated solution to drive backlight applications up to six LEDs from a Li-Ion cell input with the added advantage of high side sense in a tiny SC70 package. 



- C1: TAIYO YUDEN LMK212BJ105MD
- C2: TAIYO YUDEN LMK212BJ475MG
- D1: AOT-2015 HPW1751B
- L1: MURATA LQH32CN100

**Figure 8. A 2-Cell Li-Ion driver for torch and flash mode control**

For more information on parts featured in this issue, see <http://www.linear.com/designtools>

# A Simple Digitally Tunable Active RC Filter

by Philip Karantzalis

## Introduction

The tuning of the cutoff frequency ( $f_{\text{CUTOFF}}$ ) of an active RC filter can be implemented using switched-capacitor circuits or continuous time circuits. In applications that require infinite tuning resolution of an any-order filter in a single IC package, a switched-capacitor approach is preferable (simply changing the clock frequency tunes  $f_{\text{CUTOFF}}$ ). In applications that require tuning a continuous time filter to just a few cutoff frequencies, tuning can be implemented using op amps, CMOS switches and resistor or capacitor arrays.

Continuous time filters can also be tuned with high resolution over a large frequency range via digital control by using DACs to multiply the RC time constant of op-amp-based integrators (for example, an 8-bit DAC-based tuner allows for 256 frequency steps). Figure 1 shows a simple, low order and low cost continuous time filter circuit.

It can be tuned to a few cutoff frequencies via a Serial Peripheral Interface (SPI)<sup>1</sup>. This is a simpler alternative to using switches with resistor or capacitor arrays or multiple DACs that require a large number of active and passive components.

Digital control through an SPI is useful in a variety of applications to control band-limiting for sensor and transducer signals. Typical applications are: accelerometers for vibration analysis, hydrophones for sonar detection, LVDTs for linear motion measurements and microphones for sound reception and recording.

## An SPI-Tunable Second Order Filter

The Figure 1 circuit is a state-variable second order filter using two ICs, a low noise CMOS quad op amp (LTC6242) and a low noise dual Programmable Gain Amplifier, PGA (LTC6912-X). The gains of the two LTC6912-X

amplifiers (GA and GB) are independently programmed via SPI control. The SPI controlled gain settings of an LTC6912-1 are 1, 2, 5, 10, 20, 50 and 100 and for an LTC6912-2 1, 2, 4, 8, 16, 32 and 64. The Figure 1 filter has three inverting outputs providing a highpass, bandpass and lowpass frequency responses. An optional inverting amplifier connected to one of the three outputs provides for a noninverting or a differential filter output. The filter's second order transfer function is a function of the circuit's resonant frequency,  $f_0$  and Q values. The  $f_0$  frequency is equal to the integrator's RC constant, the dual PGA gain and the ratio of resistors R4 and R2 (if  $R4 = R2$  and  $G_A = G_B = \text{Gain}$  then  $f_0 = \text{Gain}/2\pi RC$ ). The filter's Q value is equal the ratio of resistors R3 and R2 and the two PGA gains (if  $R4 = R2$  and  $G_A = G_B$  then  $Q = R3/R2$ ). The filter's passband gain is equal to the ratio of  $R4/R1$ ,  $R3/R1$  and  $R2/R1$

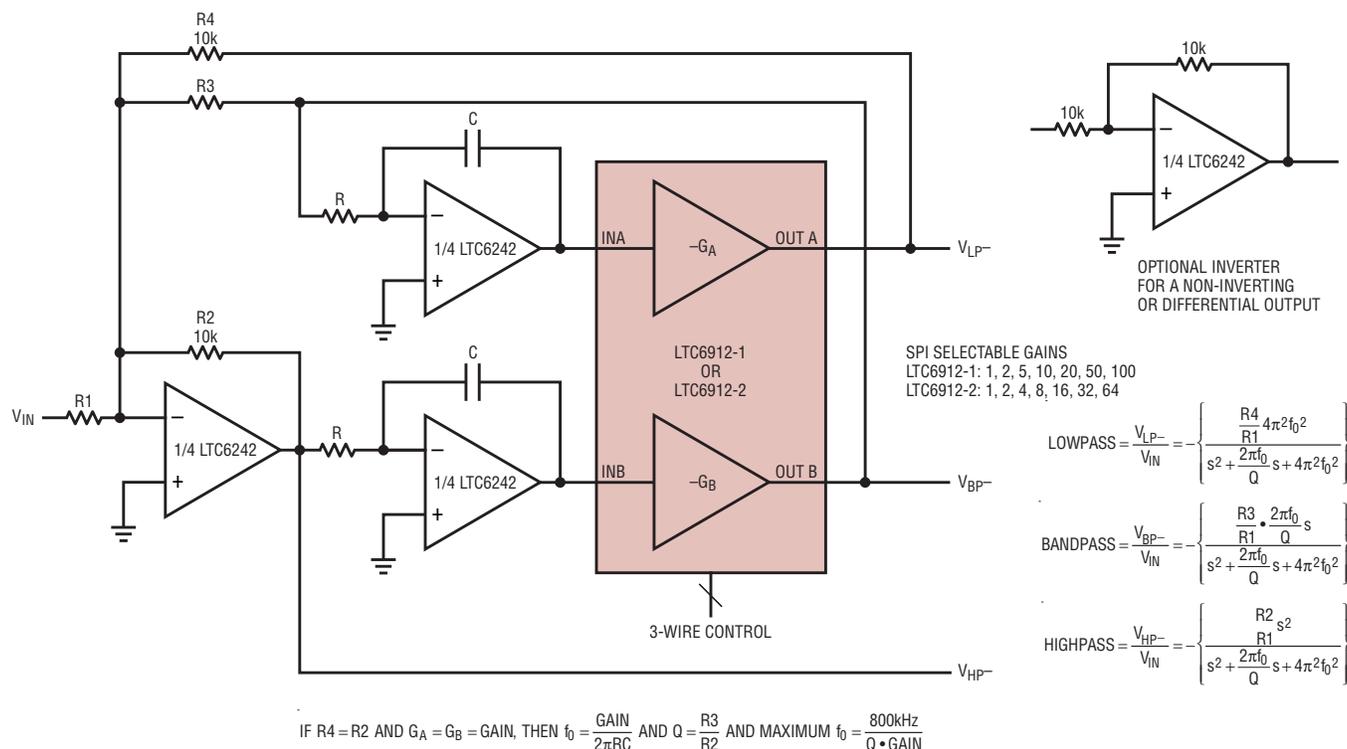


Figure 1. An SPI tunable second order active RC filter

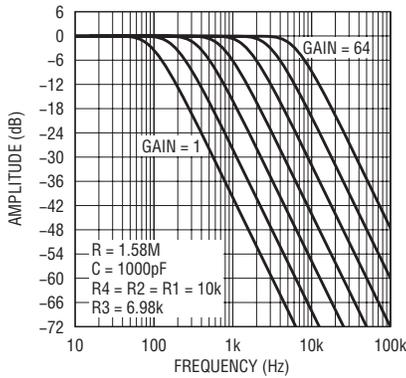


Figure 2. Tunable second order Butterworth lowpass response using the LTC6912-2

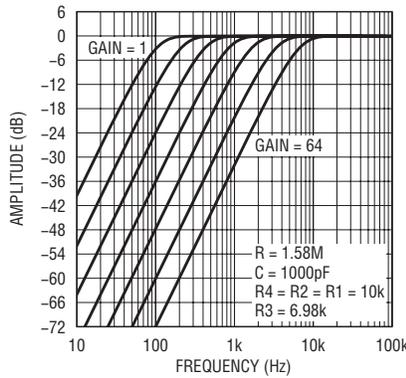


Figure 3. Tunable second order Butterworth highpass response using the LTC6912-2

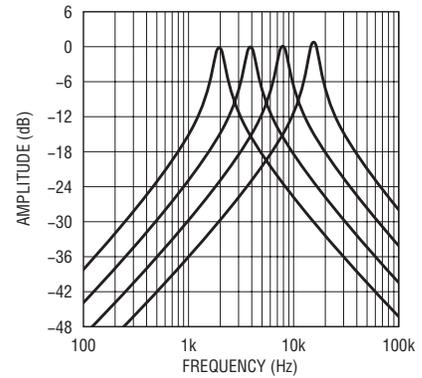


Figure 4. Tunable second order bandpass filter using an LTC6912-1 with gains 1-8

for a lowpass, bandpass and highpass filters respectively.

### A Tunable Lowpass or Highpass Filter

The shape of the amplitude response of the second order depends on the  $f_0$  frequency relative to the cutoff frequency and the  $Q$  value. In a second order Butterworth highpass or lowpass response the  $f_0$  frequency is equal to  $f_{CUTOFF}$  ( $f_{-3dB}$ ) and the filter's  $Q$  value is equal to 0.707. In a second order Bessel highpass or lowpass response

the  $f_0$  frequency is equal to  $1.274 \cdot f_{CUTOFF}$  and the filter's  $Q$  value is equal to 0.577. Figure 2 shows the tunable range of a Butterworth lowpass filter using an 100Hz integrator frequency ( $R = 1.58M\Omega$ ,  $\pm 1\%$  and  $C = 1000pF$ ,  $\pm 5\%$ ) and an LTC6912-2 to tune the filter's  $f_{CUTOFF}$  from 100Hz to 6.4kHz. Figure 3 shows the tunable range of a Butterworth highpass filter that is the mirror opposite of the lowpass filter response of Figure 2. The output response to a step change is approximately equal to  $5/f_{CUTOFF}$ , (if the step

change is to a 1kHz  $f_{CUTOFF}$  then the filter settles five milli-seconds after a step change). The maximum tunable  $f_0$  frequency is a function of the gain-bandwidth product of the op amps and the circuit's sensitivity to the highest PGA gain that is used for tuning. For the amplifiers shown, based on empirical data, a maximum  $f_0$  of  $800kHz/[Q \cdot \text{Gain}]$  limits gain error to  $\leq 2dB$ . For example, if only the lowest 1, 2, 5 and 10 gains of an LTC6912-1 are used for tuning, a second order Butterworth lowpass filter ( $f_0 = f_{CUTOFF}$ )

*continued on page 45*

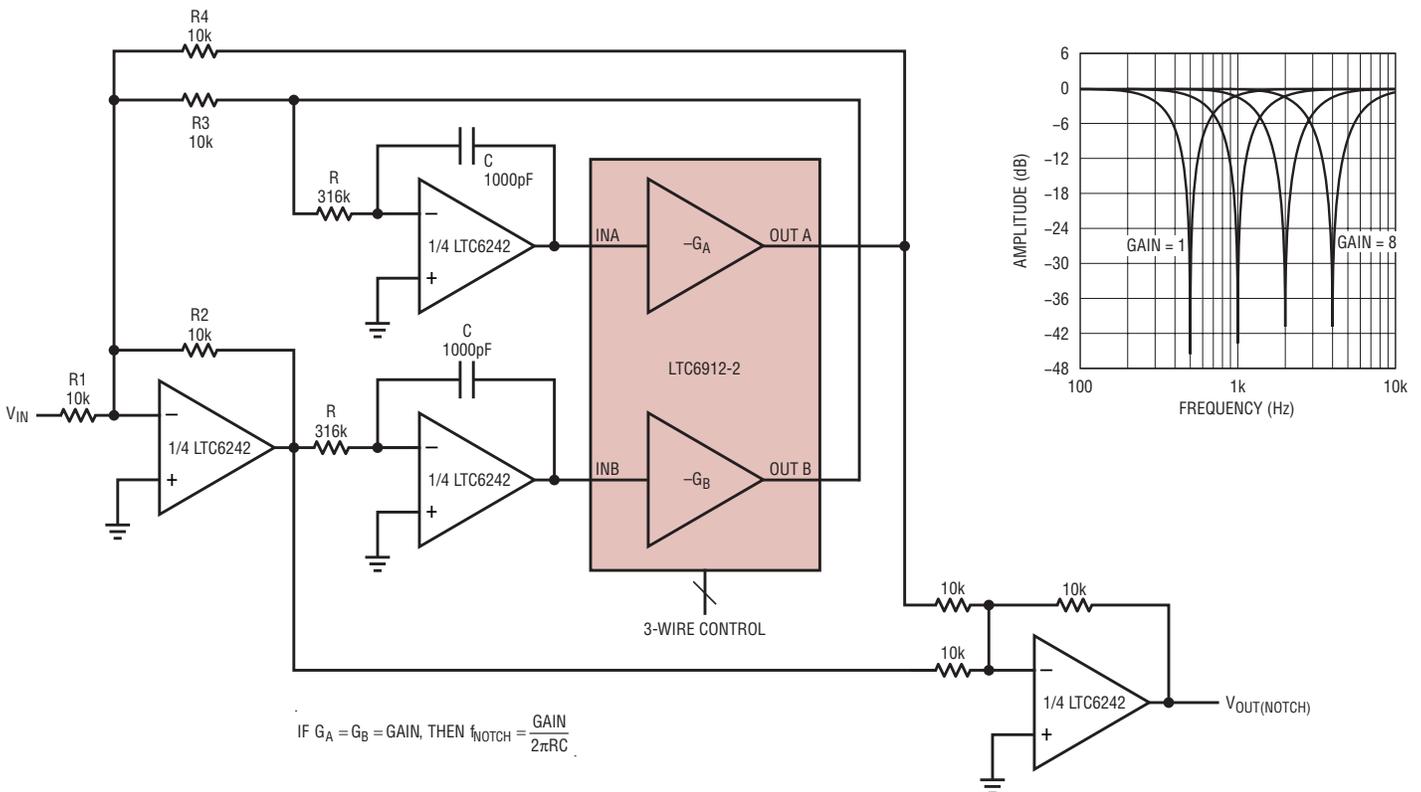


Figure 5. An SPI-tunable second order notch filter

# Save Board Space with a High Efficiency Dual Synchronous, 400mA/800mA, 2.25MHz Step-Down DC/DC Regulator

by Damon Lee

## Introduction

The ever shrinking nature of cell phones, pagers, PDAs and other portable devices drives a corresponding demand for smaller components. One way to shrink DC/DC regulator circuitry is to increase the switching frequency of the regulator, thus allowing the use of smaller and cheaper capacitors and inductors to complete the circuit. Another way is to combine the switcher and MOSFETs in one small, monolithic package. The LTC3548 DC/DC regulator does both.

The LTC3548 is a 10-lead MSOP/DFN, dual, synchronous, step-down, current mode, DC/DC regulator, intended for low power applications. It operates within a 2.5V to 5.5V input voltage range and has a fixed 2.25MHz switching frequency, making it possible to use low-profile capacitors and inductors that are only 1mm high. The LTC3548 is the latest in the LTC3407 and LTC3407-2 family of dual regulators and features an improved Burst Mode ripple and two outputs of 400mA and 800mA. It is available in small MSOP and DFN packages, allowing



Figure 1. Two DC/DC regulators occupy less than 0.2in<sup>2</sup> of board space

two DC/DC Regulators to occupy less than 0.2 square inches of board real estate, as shown in Figure 1.

The outputs of the LTC3548 are independently adjustable from 0.6V to 5V. For battery-powered applications that have input voltages above and below the output voltage, the LTC3548 can be used in a single inductor, positive buck-boost converter configuration (see data sheet for details). Two built in 0.35Ω switch provides high efficiency at maximum output current. Internal compensation minimizes external components and board space.

Efficiency is extremely important in battery-powered applications, and the LTC3548 keeps efficiency high with an automatic, power saving Burst Mode operation, which reduces gate charge losses at low load currents. With no load, both converters together draw only 40μA, and in shutdown, the device draws less than 1μA, making it ideal for low current applications. The LTC3548 features an improved Burst Mode ripple voltage, which is only about one third of the ripple for the LTC3407 and LTC3407-2, as shown in Figure 2 and Figure 3.

The LTC3548 uses a current-mode, constant frequency architecture that benefits noise sensitive applications. Burst Mode is an efficient solution for low current applications, but sometimes noise suppression is a higher priority. To reduce noise problems, a pulse-skipping mode is available, which decreases the ripple noise at low currents. Although not as efficient as Burst Mode at low currents, pulse-skipping mode still provides high efficiency for moderate loads, as seen in Figure 4. In dropout, the internal

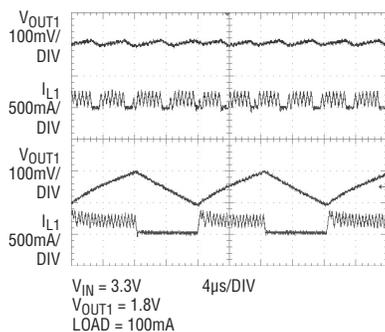


Figure 2. Comparison of ripple for Burst Mode operation of the LTC3548 and LTC3407-2.

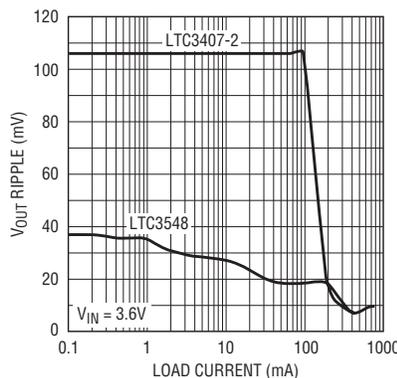


Figure 3. Burst Mode operation output voltage ripple vs load current for the LTC3548 and LTC3407-2.

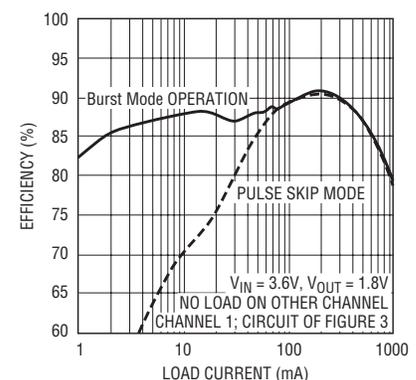


Figure 4. Efficiency of Burst Mode operation and pulse skip mode

P-channel MOSFET switch is turned on continuously, thereby maximizing the usable battery life.

A Power-On Reset output is available for microprocessor systems to insure proper startups. Internal overvoltage and undervoltage comparators on both outputs will pull the  $\overline{\text{POR}}$  output low if the output voltages are not within  $\pm 8.5\%$ . The  $\overline{\text{POR}}$  output is delayed by 262,144 clock cycles (about 175ms) after achieving regulation, but will be pulled low immediately when either output is out of regulation.

### A High Efficiency 2.5V and 1.8V Step-Down DC/DC Regulator with all Ceramic Capacitors

The low cost and low ESR of ceramic capacitors make them a very attractive choice for use in switching regulators. In addition, ceramic capacitors have a benign failure mechanism unlike tantalum capacitors. Unfortunately, the ESR is so low that it can cause loop stability issues. A solid tantalum capacitor's ESR generates a loop zero at 5kHz–50kHz that can be instrumental in giving acceptable loop phase margin. Ceramic capacitors, on the other hand, remain capacitive to beyond 300kHz and usually resonate

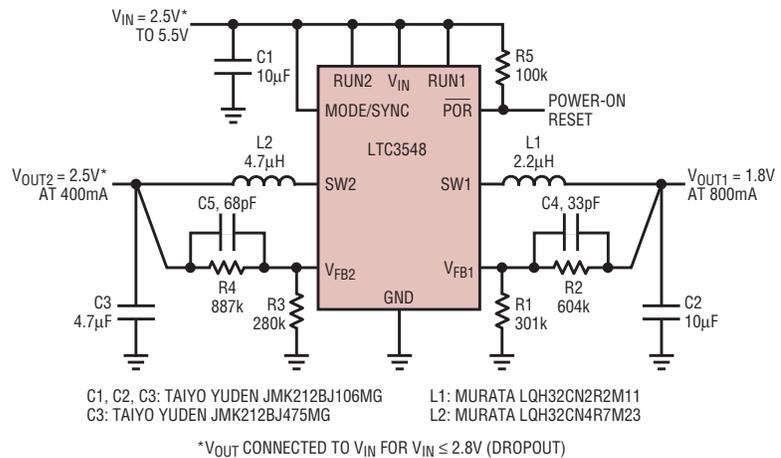


Figure 5. Dual output step-down application yields 1.8V at 800mA and 2.5V at 400mA.

with their ESL before the ESR becomes effective. Also, inexpensive ceramic capacitors are prone to temperature and voltage effects, requiring the designer to check loop stability over the operating temperature range. For these reasons, great care is usually needed when using only ceramic input and output capacitors. The LTC3548 was designed with ceramic capacitors in mind and is internally compensated to handle these difficult design considerations. High quality X5R or X7R ceramic capacitors should be used to minimize the temperature and voltage coefficients.

Figure 5 shows a typical application for the LTC3548 using only ceramic capacitors. This circuit provides a regulated 2.5V output and a regulated 1.8V output, at up to 400mA and 800mA, from a 2.5V to 5.5V input.

### Conclusion

The LTC3548 is a dual monolithic, step-down regulator that switches at 2.25MHz, minimizing component costs and board real estate requirements for DC/DC regulators. The small size, efficiency, low external component count, and design flexibility of the LTC3548 make it ideal for portable applications. 

Digi-Tune Filters, continued from page 43

can be tuned to 110kHz (maximum  $f_0 = 800\text{kHz}/[0.707 \cdot 10]$ ).

### A Tunable Bandpass Filter

The  $-3\text{dB}$  bandwidth of a second order filter is equal to the center frequency ( $f_{\text{CENTER}}$ ) divided by the  $Q$  value (bandwidth =  $f_{\text{CENTER}}/Q$ ). The sensitivity of the second order bandpass filter to the tolerance of the integrator's RC values is proportional to the filter's  $Q$ . Typically with a  $Q \leq 4$ , using a  $\pm 1\%$  R and a  $\pm 5\%$  C for the filter's two integrators is practical for a second bandpass filter. The sensitivity of the second order bandpass filter with  $Q > 4$  increases rapidly for each unit of  $Q$  increase and the filter's two integrators should use  $\pm 1\%$  RC components.

Figure 4 shows the bandpass filter of Figure 1 tuned from 2kHz to 16kHz using a 2kHz integrator frequency ( $R = 205\text{k}, \pm 1\%$  and  $C = 390\text{pF}, \pm 5\%$ ) and an LTC6912-2 with gain settings 1, 2, 4, and 8. The tuned center frequencies responses of Figure 4 are 2.73% lower than the design values of 2kHz, 4kHz, 8kHz and 16kHz and equal to the error of the circuit's RC values of the two integrators (measured values of approximately 206k for each R and 403pF for each C). The gain error at 16kHz is due to the filter's  $f_0$  frequency approaching the maximum  $f_0$  for a  $Q = 4$  and a PGA gain equal to 8 (maximum  $f_0 = 25\text{kHz} = 800\text{kHz}/[4 \cdot 8]$ ). The maximum  $f_0$  frequency is a function

of the gain-bandwidth product of the LTC6912-X op amps.

### Other Filter Options

Figure 5 shows an example of a second order notch filter. The notch filter's integrator frequency is 500Hz ( $1/[2\pi \cdot 316\text{k}\Omega \cdot 1000\text{pF}]$ ) and with PGA gains 1, 2, 4 and 8 the notch frequency is tuned to 500Hz, 1kHz, 2kHz and 4kHz respectively. Any of the filters discussed above can be made into SPI-tunable fourth order filters by cascading two second order circuits. 

Notes

<sup>1</sup> SPI is a synchronous communication protocol using a 3-wire interface between a microprocessor and a peripheral device

# New Device Cameos

## Wide Dynamic Range RF/IF Log Detector

The LT5537 is a wide dynamic range RF/IF detector, which operates from below 10MHz to 1000MHz. The lower limit of the operating frequency range can be extended to near DC by the use of an external capacitor. The input dynamic range at 200MHz with  $\pm 3$ dB nonlinearity is 90dB (from  $-76$ dBm to 14dBm, single-ended 50 $\Omega$  input). The detector output voltage slope is nominally 20mV/dB, and the typical temperature coefficient is 0.01dB/ $^{\circ}$ C at 200MHz.

The LT5537 is available in a tiny 8-Lead (3mm  $\times$  2mm) DFN package.

## Dual Output Synchronous DC/DC Controller Draws Only 80 $\mu$ A Quiescent Current in an Automotive System

The LTC3827 is a low quiescent current, 2-phase dual output synchronous step-down DC/DC controller. The LTC3827 draws only 80 $\mu$ A when one output is active and only 115 $\mu$ A

when both outputs are active, making it ideally suited for automotive applications, such as navigation systems, where one or more supplies remains active while the engine is off. The LTC3827's input supply range of 4V to 36V is wide enough both to protect against high input voltage transients and to continue to operate during automotive cold crank. The LTC3827 features a  $\pm 1\%$  internal reference and can provide output voltages from 0.8V up to 10V, making it perfect for the higher voltage supplies typically required for audio systems, analog tuners, and CD/DVD players in many automobiles. Each output can deliver up to 20A of current at efficiencies as high as 95%. The LTC3827 is rated for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C, and has a maximum operating junction temperature of  $125^{\circ}$ C.

The LTC3827's constant frequency, current mode architecture provides excellent line and load regulation, and its 2-phase operation reduces input capacitance requirements. The LTC3827

smoothly ramps each output voltage during startup using separate adjustable soft-start and tracking input pins. It operates at a selectable frequency between 250kHz and 550kHz, and can be synchronized to an external clock from 140kHz to 650kHz using its phase-locked loop (PLL). Output overvoltage and overcurrent (short circuit) protection are provided internally. With both outputs shut down, the LTC3827 draws a mere 8 $\mu$ A.

The LTC3827 is offered in two packages: a 28-lead SSOP (LTC3827-1) and a 32-pin 5mm  $\times$  5mm QFN (LTC3827).

**For further information on any of the devices mentioned in this issue of *Linear Technology*, use the reader service card or call the LTC literature service number:**

**1-800-4-LINEAR**

**Ask for the pertinent data sheets and Application Notes.**

*LTC2970, continued from page 5*

registers allow the user to define instantaneous and/or latched faults in the event one of the input voltages deviates outside an acceptable window. The GPIO\_0 and FAULT pins can be configured to assert if a fault occurs.

## Tracking Two or More Supplies with the LTC2970-1

The LTC2970-1 enables power supply tracking with the addition of a few external components. A special global address and synchronization command allow multiple LTC2970-1s to track and sequence multiple pairs of power supplies.

A typical LTC2970-1 tracking application circuit is shown in Figure 7. The GPIO\_0 and GPIO\_1 pins are tied directly to their respective DC/DC converter RUN/SS pins. When GPIO\_CFG is pulled-up to  $V_{DD}$ , the LTC2970-1 automatically holds off

the DC/DC converters after power-up. N-channel FETs Q10 and Q11 and diodes D10 and D11 form unidirectional range switches around R30A and R31A while GPIO\_CFG is high, which allow the  $V_{OUT0}$  and  $V_{OUT1}$  pins to drive the converter outputs all the way to/from ground through resistors R30B and R31B. When GPIO\_CFG pulls low, FETs Q10 and Q11 turn off. R30A and R31A then combine in series with R30B and R31B for normal margin operation. The 100k $\Omega$ /0.1 $\mu$ F lowpass filter in series with the gates of Q10 and Q11 minimizes charge injection into the feedback nodes of the DC/DC converters when GPIO\_CFG pulls low.

## Conclusion

The LTC2970 dual power supply monitor and controller combines the necessary features essential for digitally managed, high availability

power applications into one easy-to-use device. A multiplexed, differential input 14-bit delta-sigma and a low drift on-chip reference deliver less than  $\pm 0.5\%$  total unadjusted error. Two continuous-time, 8-bit, voltage-buffered IDACs can also be programmed through the I<sup>2</sup>C and SMBus compatible interface to servo power-supplies to the desired voltages. Extensive, user configurable fault monitoring and a built-in servo algorithm reduce the burden on system computing resources and shorten software development time. The LTC2970 and LTC2970-1 are available in a 24-lead QFN package.



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