

**IN THIS ISSUE . . .**

**COVER ARTICLE**

**LTC®1409/LTC1415 High Speed, Low Power 12-Bit ADCs** ..... 1  
Kevin R. Hoskins

**Issue Highlights** ..... 2

**LTC in the News** ..... 2

**DESIGN FEATURES**

**LTC1553 Synchronous Regulator Controller Powers Pentium® Pro and Other Big Processors** ..... 3  
Y.L. Teo, S.H. Lim and Craig Varga

**The LT®1575/LT1577 UltraFast™ Linear Regulator Controllers Eliminate Bulk Output Capacitors** ..... 9  
Anthony Bonte

**LTC1479 PowerPath™ Controller Simplifies Portable Power Management Design** ..... 14  
Tim Skovmand

**New Rail-to-Rail Amplifiers: Precision Performance from Micropower to High Speed** ..... 18  
William Jett and Danh Tran

**High Efficiency, Low Dropout Lithium-Ion Battery Charger Charges Up to Five Cells at 4 Amps or More** ..... 23  
Fran Hoffart

**LTC1069-X: a New Family of 8th Order Monolithic Filters** ..... 27  
Nello Sevastopoulos and Philip Karantzalis

**DESIGN IDEAS**

**Micropower ADC and DAC in SO-8 Give PC 12-Bit Analog Interface** ..... 30  
Kevin R. Hoskins

**High Efficiency, Low Power, 3-Output DC/DC Converter** ..... 33  
John Seago

**Synchronizing LTC1430s for Reduced Ripple** ..... 34  
Craig Varga

**DESIGN INFORMATION**

**New Voltage References Are Smaller and More Precise** ..... 35  
John Wright

**New Device Cameos** ..... 38

**Design Tools** ..... 39

**Sales Offices** ..... 40

## LTC1409/LTC1415 High Speed, Low Power 12-Bit ADCs

by Kevin R. Hoskins

### High Speed, Less Power

Expanding the family of high speed, low power dissipation 12-bit ADCs that began with the LTC1410, LTC recently introduced the LTC1409 and the LTC1415, increasing the number of high speed, low power ADCs available to designers of high speed data acquisition systems. With these new choices, a designer can pick an ADC that is optimized for his or her particular application. The LTC1409 and LTC1415 are ideal solutions for applications such as ADSL, HDSL, modems, direct downconversion, CCD imaging, DSP-based vibration analysis, waveform digitizers and multiplexed systems.

The new LTC1409 and LTC1415 have much lower power dissipation and higher performance than other 12-bit ADCs currently on the market. The LTC1409 and LTC1415 dissipate just 80mW and 60mW, respectively. Package size is also a major advantage of the LTC1409 and LTC1415, since they are available in

28-pin SO and SSOP packages. Some of the other key features of these new devices are shown in Table 1.

### Performance Enhancing Features

#### Differential S/H and Wideband CMRR

Like the LTC1410, the LTC1409 and LTC1415 have fully differential inputs. The differential inputs have a very good CMRR: 60dB or better over a 0-to-10MHz bandwidth. The bandwidth of the input sample-and-hold is typically 30MHz. All of these features combine to create improved solutions for present and future data- or signal-acquisition systems.

Figure 1 is a block diagram of the LTC1409 and LTC1415. The outstanding conversion speed and accuracy of these parts is the result of the high performance differential sample-and-hold and the extremely

*continued on page 20*

**Table 1. LTC1409/LTC1415 key features**

	LTC1409	LTC1415
Conversion Throughput	800ksps	1.2Msps
Low Power Dissipation	80mW ( $\pm 5V$ supply)	60mW (+5V supplies)
NAP and SLEEP Modes	✓	✓
Small Package— 28-pin SSOP	✓	✓

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# Issue Highlights

This issue of *Linear Technology* is loaded with new products. Our cover article introduces a pair of new high speed, low power 12-bit ADCs, the LTC1409 and LTC1415. These new parts offer conversion rates of 800ksps and 1.2Msps respectively and have much lower power dissipation than other ADCs currently on the market. This makes them ideal for applications such as ADSL, HDSL, modems, CCD imaging and the like.

Power products feature prominently in this issue: the LTC1553, a synchronous switching regulator controller, is designed to convert 5V/12V "silver box" supplies to the low voltages required by the Intel Pentium processor and other big CPUs. An onboard 5-bit DAC conforms to the requirements of the Intel Pentium Pro processor power supply specification, making the LTC1553 a perfect fit in these applications. The LTC1553, like the LTC1430, provides current-limit and short-circuit protection without the use of an external sense resistor.

Also featured in this issue is the new LT1575/LT1577 family of controller ICs. These new, easy-to-use devices drive discrete N-channel MOSFETs as source followers to produce extremely low dropout, UltraFast transient response regulators. These circuits completely eliminate expensive tantalum or bulk electrolytic capacitors in the most demanding microprocessor applications. For example, a 200MHz Pentium processor can operate with only the twenty-four 1 $\mu$ F ceramic capacitors that Intel already requires for the microprocessor.

Another power control device for computer applications is introduced in this issue: The LTC1479 PowerPath™ controller eliminates power-management nightmares that plague the dual rechargeable battery systems found in most notebook computers and other portable equipment.

Finally, we have the LT1620, an IC designed to be used with a current mode PWM controller (such as the LTC1435) to increase the output volt-

## LTC in the News...

### Linear Technology Corp. Reports Steady Sales and Profits for Q1 1997 in a Tight Semiconductor Environment

Linear Technology Corporation's net sales for its first quarter, ended September 29, 1996, were \$90,063,000, an increase of 4% over the first quarter of the previous year.

The Company also reported net income for the quarter of \$31,358,000 or \$0.40 per share, an increase of 3% over \$30,520,000 or \$0.39 per share, reported for the first quarter of last year. A cash dividend of \$0.05 per share will be paid on November 13, 1996 to shareholders of record on October 25, 1996.

According to Robert H. Swanson, president and CEO, "Despite a sluggish semiconductor environment, we were able to maintain our net sales and profitability. Our return on sales of approximately 35% continues to lead the industry. We generated approximately \$10 million in cash even after paying approximately \$16 million to repurchase shares of our own stock. However, in the short term we con-

tinue to be in an unpredictable environment whereby reduced backlog and shorter lead times cause the business to be very dependent on orders that are received and shipped in the same quarter."

A detailed look at the best-performing stock index of them all—the Nasdaq 100—reveals that Linear Technology Corp. is ranked high again this year among the best-run, most effective and highest-valued companies in the nation. Coming in well above such familiar names as Altera (70th), Maxim (71st), Micron (83rd) and Cirrus Logic (84th), Linear Technology Corp. is listed 52nd on the Nasdaq 100, with a market capitalization of more than \$2.2 billion as of press time.

The financial performance of LTC has been so good that one major-fund manager who prefers bonds to stocks says that he would make an exception for LTC. Quoted by Kathleen Gallagher in her syndicated column "Street Smart," Thomas M. Wargin, president of Liberty LaSalle Financial Group, Inc., says that he "likes Linear Technology, a specialty chip maker whose stock price dropped (this summer). He expects its earnings to grow 21% annually for the next five years." **LT**

age range and optimize the circuit for battery charging applications. In this article, the LT1620 and LTC1435 are featured in a high current, high performance constant-voltage/constant-current battery charger for lithium-ion and other battery types.

Several new additions to LTC's family of rail-to-rail op amps are presented herein. These include the LT1498/LT1499 C-Load™ op amps, which feature a 10MHz gain-bandwidth product, 4V/ $\mu$ s slew rate and the ability to drive 10,000pF; the low current LT1466-69, with quiescent current of only 50 $\mu$ A; and the high precision LT1218A/LT1219A, featuring  $V_{OS}$  trimmed to 100 $\mu$ V max.

Filters are represented in this issue

by the LTC1069-X, a family of semicustom filters that can integrate any single 8th order or dual 4th order classical filter approximation, or any application-specific filter response, in an SO-8 package.

This issue includes a modest collection of Design Ideas: a 12-bit analog interface for the PC, based on the LTC1298 ADC and LTC1446 DAC, with sample code; a low power, 3-output DC/DC converter built around the LTC1435; and a technique for synchronizing two LTC1430 buck regulators for reduced output ripple. We conclude with Design Information on the LT1460 and LT1236 voltage references, and a page of New Device Cameos. **LT**

# LTC1553 Synchronous Regulator Controller Powers Pentium® Pro and Other Big Processors

by Y.L. Teo, S.H. Lim and Craig Varga

## Introduction

Over the past few years, the operating voltages of Pentium class and other modern microprocessors have dropped from 5V to 3.3V and below, while operating currents have steadily increased. Voltage regulation requirements have also tightened as the safety margin between proper operation and chip destruction has decreased along with feature size. To complicate matters further, the newest Pentium Pro processors from Intel® require a digitally adjustable power supply, so that the processor itself can determine the power supply voltage. The “silver box” power supplies provide only 5V/12V, with the exception of a few supplies also capable of delivering 3.3V. Due to the extreme accuracy and exceptionally fast load transient response required by today’s processor supplies, the supply has been forced onto the computer’s motherboard. To fit this niche, Linear Technology introduces the LTC1553, a synchronous switching regulator controller designed to convert the 5V/12V “silver box” rails to the lower 1.80V–3.5V required by the CPU. An onboard 5-bit DAC conforms to the requirements of the Intel Pentium Pro processor power supply specification, making the LTC1553 a perfect fit in these applications.

The LTC1553 is the newest member of the LTC switching regulator family. It shares many performance features with the popular LTC1430, including excellent ( $\pm 1\%$ ) output regulation over temperature, line voltage and load current variations. The LTC1553, like the LTC1430, provides current-limit and short-circuit protection without the use of an external sense resistor. This is accomplished by measuring the voltage drop across the external high-side MOSFET dur-

ing its on-time. To compliment the main voltage-feedback loop, the LTC1553 includes two additional feedback loops to provide good large-signal transient response. The LTC1553

adds additional internal circuits to conform to the Intel Pentium Pro processor power converter requirements while minimizing the number of external components. An on-chip 5-bit

Table 1. Output voltage vs VIDn code

VID4	VID3	VID2	VID1	VID0	(VDC)
0	1	1	1	1	*
0	1	1	1	0	*
0	1	1	0	1	*
0	1	1	0	0	*
0	1	0	1	1	*
0	1	0	1	0	*
0	1	0	0	1	*
0	1	0	0	0	*
0	0	1	1	1	*
0	0	1	1	0	*
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05
1	1	1	1	1	No CPU
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

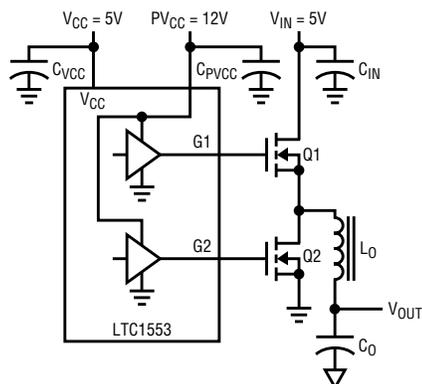
\*Reserved for future expansion

digital-to-analog converter (DAC) provides digital output voltages conforming to Intel's specifications. This allows the LTC1553 to read the code sent by the processor and provide it with the requested voltage. The LTC1553 also provides a power-good indication (PWRGD) to the system. There is also an on-chip overvoltage protection circuit that latches the regulator in an off state if the output voltage ever rises 15% or more above the DAC-requested voltage. Over-temperature protection is available with only two external components (a resistor and a thermistor) connected to the OUTEN pin.

In applications with other processors, the four DAC inputs can be routed to a jumper block, zero ohm resistors or a DIP switch, or hard wired, to set the desired output voltage. This allows the output voltage to be programmed easily in steps while eliminating the need to stock an assortment of precision resistors. This flexibility in output voltage setting is cheap insurance against last-minute power supply voltage changes by microprocessor manufacturers.

## LTC1553 Overview

The LTC1553 runs at a fixed switching frequency, nominally 300kHz, without any external oscillator components. The on-chip, 5-bit digital-to-analog converter (DAC) allows the output voltage to be adjusted from 1.80V to 3.5V, as shown in Table 1. Voltage mode control eliminates the need for a current sense resistor.



**Figure 1a. Typical LTC1553 circuit with PV<sub>CC</sub> powered from a 12V supply and main V<sub>IN</sub> powered from a high power 5V supply**

Current limiting is maintained by sensing the voltage drop across the R<sub>DS(ON)</sub> of the high-side MOSFET. The output enable pin employs a multi-level voltage threshold scheme that permits overtemperature sensing as well as providing the normal enable function.

The LTC1553 is designed to be used with an all-N-channel MOSFET, synchronous buck regulator topology. The gate drive is able to significantly exceed the main power supply voltage. This allows the high-side N-channel MOSFET(s) to be fully enhanced, ensuring low R<sub>DS(ON)</sub> and maximum efficiency. The driver outputs can source and sink enough current to drive multiple, paralleled power MOSFETs if desired, in order to obtain very low conduction losses. Low loss operation eliminates the need for a heat sink in most applications and results in very high efficiency. A soft-start circuit is included on the chip, permitting the rate of rise of the output voltage at turn-on to be controlled.

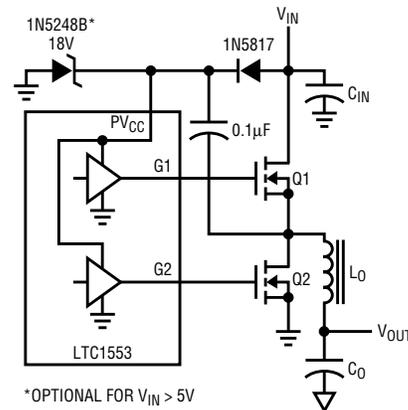
## Internal DAC and Output Voltage Accuracy

An on-chip 5-bit DAC is used to set the output voltage. No external feedback resistors are required. Five TTL inputs (VID0, VID1, VID2, VID3 and VID4) program the internal DAC (see Table 1). Each of the VID<sub>n</sub> pins has an internal pull-up resistor to ensure a high state if it is not connected. When all the VID<sub>n</sub> pins are in the high state, the LTC1553 shuts down, forcing the output voltage to zero and dropping the quiescent current to approximately 150μA. The ten lowest voltage codes are disabled at this time, allowing for future expansion. The DAC accuracy, initial reference voltage tolerance and internal feedback resistor tolerances result in a maximum initial output voltage error of ±1% of the selected output voltage. The line and load regulation plus temperature drift over the 0°C to 70°C temperature range will contribute another ±1% to the output error budget. This gives a total static operating error of less than ±2%, providing sufficient head-

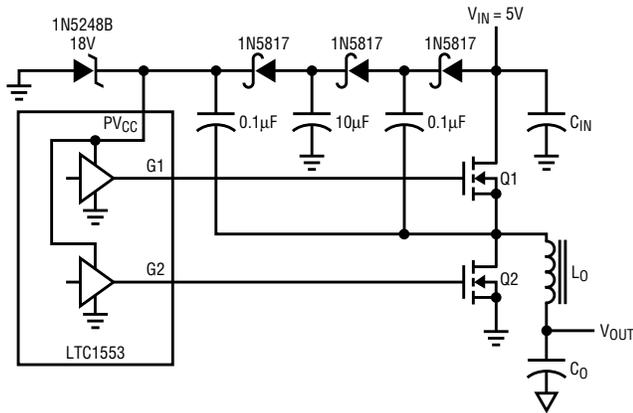
room (3%) for the dynamic response to remain within a ±5% output voltage tolerance, while still requiring a reasonable amount of output capacitance.

## External MOSFET Drivers

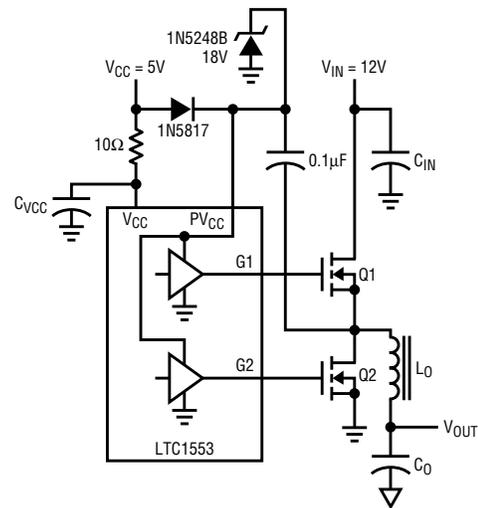
The on-chip output drivers are powered from the PV<sub>CC</sub> pin, which is specified with a 20V maximum supply voltage. The PV<sub>CC</sub> supply should be at least 5V higher than the main V<sub>IN</sub> supply to allow the G1 output driver to fully enhance a high-side N-channel MOSFET. A major advantage of the LTC1553 over some competing devices results from its CMOS implementation: full rail-to-rail gate drive provides as much as 2V more drive than would a bipolar design. This results in a 20%–25% lower R<sub>DS(ON)</sub> for a given MOSFET. Figure 1a shows a typical LTC1553 circuit with PV<sub>CC</sub> powered from a 12V supply and the main V<sub>IN</sub> powered from a high power 5V supply. This provides 7V of enhancement for the high-side switch. The amount of current required of the 12V supply varies with the amount of MOSFET gate capacitance and will typically be less than 50mA. If a 12V supply is not available, the gate drive voltage can be generated with a simple charge-pump. Figure 1b shows a doubler charge-pump used to generate the PV<sub>CC</sub> voltage in a 5V-only system. A tripler charge-pump (Figure 1c) may be used in circuits where a higher voltage is required to fully enhance the external MOSFETs.



**Figure 1b. A doubler charge pump generates the PV<sub>CC</sub> voltage for a system powered from a single 5V supply.**



**Figure 1c.** A tripler charge pump provides more gate drive for the external MOSFETs.



**Figure 1d.** An alternate 17V charge pump circuit prevents PV<sub>CC</sub> from exceeding its 20V limit.

Note that if  $V_{IN}$  is 10V or higher, a standard doubling charge-pump will cause the PV<sub>CC</sub> pin to exceed its 20V limit. Such circuits should use an alternate 17V charge-pump circuit (see Figure 1d). In any circuit where transient spikes at the PV<sub>CC</sub> pin may approach the 20V maximum rating, an 18V Zener diode is recommended from PV<sub>CC</sub> to GND (Figures 1b–1d).

### Multiple Feedback Loops Improve Transient Response

The LTC1553 uses a standard voltage feedback loop to control the output voltage (see Figure 2). The error amplifier, ERR, compares the resistor-divided output voltage at FB to the internal reference voltage,  $V_{REF}$ . This reference is controlled by the internal DAC. The resulting error voltage is amplified by the error amplifier. A pulse width modulated (PWM) signal is generated by comparing the error signal with a sawtooth waveform from the internal oscillator. This PWM and its complement signal drive the gates of power switches Q1 and Q2, respectively. Feedback loop compensation is set with an external compensation network at the COMP pin. Voltage mode control eliminates the need for a high loss, high cost, external sense resistor required by a typical current mode design.

In addition to the main feedback loop, the LTC1553 also includes two

additional “safety belt” comparators (MIN and MAX in Figure 2). In general, a control loop’s bandwidth, and hence its slew rate, is limited by stability considerations. In some instances, it may be desirable to have the ability to respond to events faster than the error amplifier is capable of slewing. The MIN/MAX comparators provide this capability. These two comparators help to prevent extreme output perturbations with fast load current transients, while allowing the main feedback loop to be optimally compensated for stability. The MAX loop responds when the output exceeds the set point by more than 5%, forcing the duty cycle to 0% and holding Q2 on until the output drops back into the acceptable range. Similarly, if the output voltage sags 5% below the set point, the MIN loop kicks in, forcing the Q1 to 85% duty cycle until the output recovers. The 95% maximum duty cycle ensures that the gate drive charge-pump (if used) is refreshed every cycle. The response times of the MIN and MAX comparators are controlled to prevent them from triggering on noise spikes.

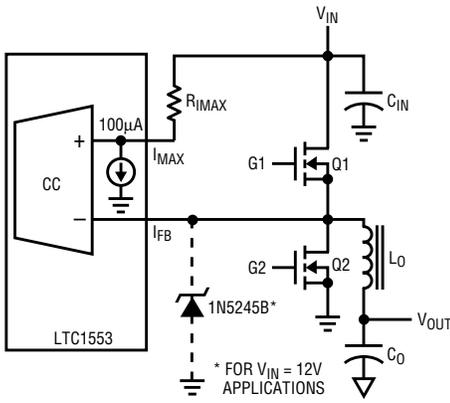
### Soft-Start and Current Limit

Just one external capacitor is needed at the SS pin to set the soft-start time. During start-up, Q1 and Q2 are switched off until the input voltage has risen to the threshold of an inter-

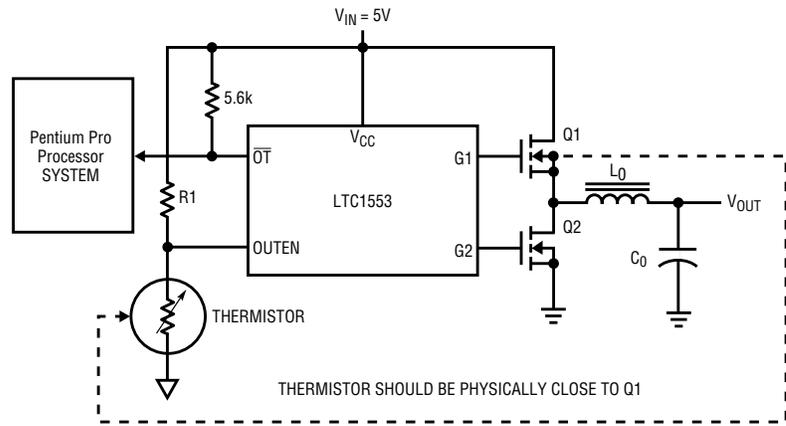
nal undervoltage lockout circuit. The soft-start capacitor is then charged by an internal 10µA current source. The soft-start function overrides the error amplifier and takes control of the pulse width modulator. As the SS pin voltage rises, the LTC1553’s G1 duty cycle increases slowly until the output voltage is in regulation, at which point control is transferred to the voltage feedback loop.

A significant advantage of employing voltage mode control in the LTC1553 is the elimination of the current sense resistor found in most other designs. With this resistor goes the simple means of providing over-current protection. Instead, the LTC1553 sets the output current limit by monitoring the voltage drop across the  $R_{DS(ON)}$  of the high-side MOSFET, Q1, during its ON state (see Figure 3). The current limit is controlled by setting the maximum voltage drop allowed across Q1 with a single external resistor,  $R_{IMAX}$ , at the I<sub>MAX</sub> pin. An internal 180µA current sink forces a voltage across  $R_{IMAX}$ . This voltage is compared to the voltage drop across Q1 during its on-time. The I<sub>FB</sub> pin connects to the source of Q1 and Kelvin senses the voltage drop across Q1. For  $V_{IN} = 12V$ , a 15V Zener diode (1N5245B or equivalent) will prevent voltage spikes at I<sub>FB</sub> from exceeding the maximum voltage rating. The current limit is designed to engage slowly





**Figure 3. Current-limit setting for the LTC1553**



**Figure 4. Using the OUTEN pin for overtemperature protection**

a shorted high-side MOSFET. Therefore, activating some form of external clamp is preferable to depending on the LTC1553 to shut the supply down, as the controller will be unable to turn off a shorted FET.

### Overtemperature Protection

The OUTEN pin is an active-high digital input that enables the G1 and G2 MOSFET driver outputs. When OUTEN is pulled to a TTL low level, both G1 and G2 pull to ground, shutting off the external MOSFETs and leaving the output in a high impedance state. OUTEN is designed with multiple thresholds to allow it to also be used for overtemperature protection. The power MOSFET operating temperature can be monitored with an external negative temperature coefficient (NTC) thermistor mounted next to the external MOSFET that is expected to run the hottest—usually the high-side device, Q1. Electrically, the thermistor should form a voltage divider with another resistor (R1) connected to V<sub>CC</sub>. Their midpoint is connected to OUTEN (see Figure 4). As the thermistor temperature

increases, the OUTEN pin voltage is reduced. Under normal operating conditions, the OUTEN pin should stay above 2V. All circuits will function normally and the  $\overline{OT}$  (overtemperature) pin will remain in a high state. If the temperature gets abnormally high, the OUTEN pin voltage will eventually drop below 2V.  $\overline{OT}$  will switch to a logic low, providing an overtemperature warning to the system. As OUTEN drops below 1.7V, the LTC1553 disables both FET drivers. This shuts the driver supply down, preventing any further heating. If the OUTEN pin is pulled below 1.2V, the LTC1553 will enter shutdown mode. All internal switching stops, the COMP, SS,  $\overline{OT}$  and PWRGD pins pull to ground and the quiescent current is reduced to 150µA. This residual quiescent current keeps the thermistor sensing circuit at OUTEN alive to allow the circuit to recover once it cools down. If the overtemperature protection circuit is not required, the OUTEN pin can be connected directly to a TTL compatible signal.

### Oscillator Synchronization

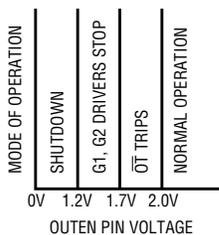
The LTC1553's internal oscillator can be synchronized to an external clock frequency higher than 300kHz. This is accomplished by connecting a TTL-level external clock signal to OUTEN. Note that if OUTEN is used for synchronization, it cannot be used for temperature monitoring. Also, if the operating frequency is forced substantially higher than 300kHz, the

gain of the main feedback loop will increase and the compensation network may have to be readjusted for optimum performance.

### Typical Application

A typical application for LTC1553 is converting 5V to 1.8V–3.5V in a Pentium Pro processor based personal computer. The supply may be in the form of a voltage regulator module (VRM) or may be implemented directly on the motherboard. The output is used to power the Pentium Pro processor and the input is taken from the system's 5V supply. The circuit shown in Figure 6 provides 1.80V–3.5V at 14A while maintaining output regulation within ±1%. The output voltage is determined by connecting the five DAC inputs to the VID pins of the processor. The power MOSFETs are sized to minimize board space and allow operation without the need of a heat sink. With proper airflow, ambient temperature conditions of up to 50° Celsius are acceptable. Typical efficiency is above 90% from 1A to 10A at 3.3V out. (see Figure 7). Achieving higher output currents from LTC1553 based designs is simply a matter of selecting appropriate MOSFETs and passive components.

It pays to look at the regulator design from two perspectives: electrical and thermal. Most processor applications operate at average currents that are approximately 80% or less of the specified peak current. As such, the thermal design can be based



**Figure 5. The OUTEN pin provides three threshold levels for temperature monitoring.**

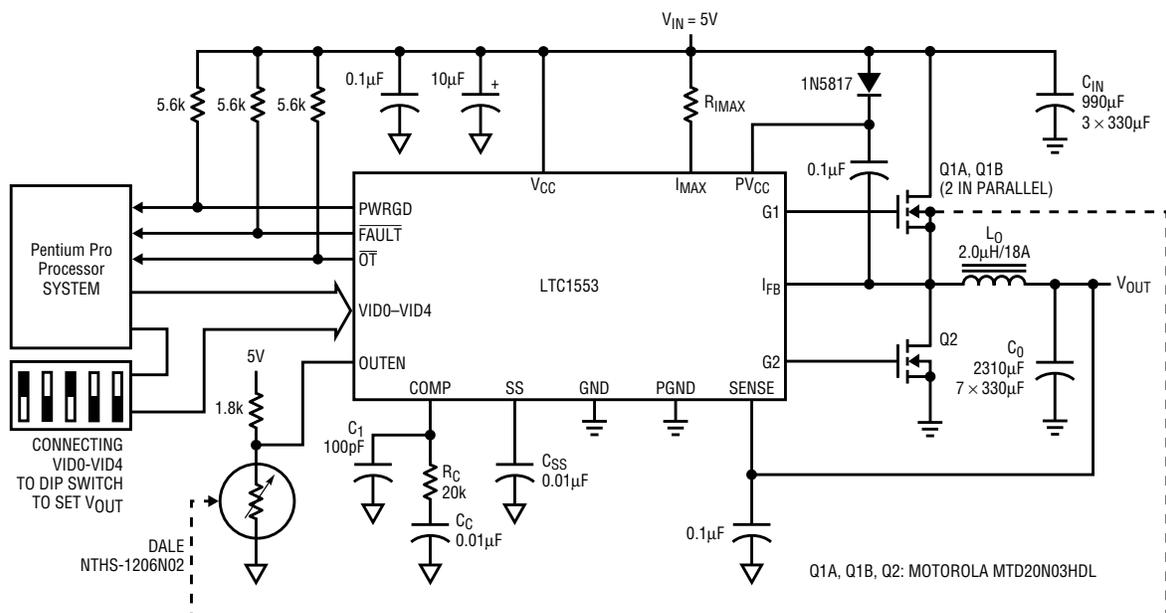


Figure 6. Typical 5V to 2.1V-3.5V/14A LTC1553 application

on the lower current level. Higher currents, while present, are typically not of sufficient duration to significantly heat the power devices. The design does, however, need to be capable of delivering the peak current without entering current limit or resulting in device failures. Keep in mind that the power dissipation in a resistive element, such as a MOSFET, varies as the square of load current. As such, raising the load current from 80% to 100% translates to approximately 56% more power dissipation ( $1/0.8^2$ ). Designing for this higher thermal load results in a huge, and most likely unnecessary, design margin. A good understanding of your system requirements can result in substantial savings in the size and cost for the power supply.

$R_{IMAX}$  sets current limit to the desired level. Add one-half of the inductor ripple current to the maximum load current to determine the peak switch current. Multiply this current by the maximum on-resistance of the selected MOSFET switch to determine the minimum current limit threshold voltage. It's a good idea to add at least a 10% margin to this limit. Also, be sure to use the hot on-resistance of the MOSFET. A multiplier of about 1.4 times the room temperature  $R_{DS(ON)}$  should be used to

determine the hot resistance. In the case of two parallel MTD20N03HDLs (Q1A and Q1B), the cold resistance is approximately  $0.035\Omega$  each; therefore, assume the hot resistance to be approximately  $0.050\Omega$ . Divide this by two because the FETs are in parallel. The threshold voltage is programmed by multiplying the  $I_{MAX}$  pin's sink current by the value of  $R_{IMAX}$ . Since we now can determine the required threshold, we need to calculate the value of  $R_{IMAX}$ . Use the specified minimum sink current,  $150\mu A$ , to calculate the resistor value.

The soft-start time is programmed by the  $0.01\mu F$  cap connected to the SS pin. The larger the value of this capacitor, the slower the turn-on ramp.

Inductor  $L_0$  is sized to handle the full load current, up to the onset of current limit, without saturating. A value of between  $2\mu H$  and  $3\mu H$  is adequate for most processor supply designs. Be careful not to overspecify the inductor. The inductor need not retain its no-load inductance up to the current-limit threshold. If the inductor still retains on the order of 25% to 30% of its initial inductance under worst-case short-circuit current conditions, the circuit should prove reliable. However, you do want

to ensure that approximately 60% to 75% of the initial inductance is retained at nominal full load. Excessive inductance roll-off will result in higher than expected output ripple voltage at high loads, along with increased dissipation in the power FETs and the inductor itself.

Proper loop compensation is critical for obtaining optimum transient response while ensuring good stability margins. The compensation network shown here gives good response when used with the inductor and the output capacitors values shown in Figure 6. Several low ESR capacitors are placed in parallel to reduce the total output ESR, resulting in lower output ripple and improved transient performance.

*continued on page 22*

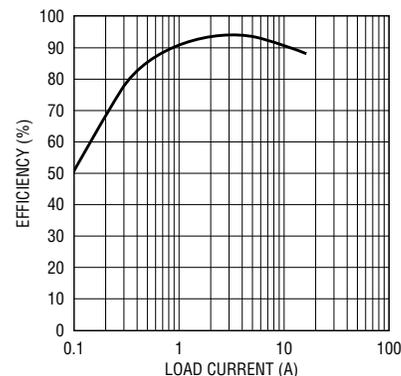


Figure 7. Efficiency plot for Figure 6's circuit

# The LT1575/LT1577 UltraFast Linear Regulator Controllers Eliminate Bulk Tantalum/Electrolytic Output Capacitors

by Anthony Bonte

## Introduction

The current generation of microprocessors places stringent demands on the input supply that powers the processor core. These microprocessors cycle load current from near zero to approximately 5 amps in tens of nanoseconds. Output voltage tolerances as low as  $\pm 100\text{mV}$  include transient response as part of the specification. Some microprocessors require only a single input supply voltage to operate both the core and the I/O circuitry. Other higher performance processors require separate power supply voltages for the processor core and the I/O circuitry. These requirements demand very accurate, very high speed regulator circuits.

Solutions employed previously include monolithic 3-terminal linear regulators, PNP transistors driven by low cost control circuits and simple buck converter switching regulators. The 3-terminal regulator achieves a high level of integration, the PNP-driven regulator achieves low dropout voltage performance and the switching regulator achieves high electrical efficiency.

However, the common trait manifested by these solutions is a transient response time measured in microseconds. This translates into an expensive

regulator output decoupling capacitor scheme. This scheme requires several hundred microfarads of very low ESR bulk capacitance comprising multiple capacitors surrounding the CPU. This bulk capacitance is in addition to the ceramic decoupling capacitor network that handles the transient load response during the first few hundred nanoseconds. The ceramic capacitors also act as a high frequency decoupling network to minimize noise associated with fast, high current spikes. The cost of the output decoupling capacitors is a significant percentage of the total power supply cost and the bulk tantalum/electrolytic capacitors comprise the majority of the capacitor cost.

## New LTC Regulator Controllers

The LT1575/LT1577 family of single/dual controller ICs are new, easy-to-use devices that drive discrete N-channel MOSFETs as source followers to produce extremely low dropout, UltraFast™ transient response regulators. These circuits achieve superior regulator bandwidth and transient load performance, and completely eliminate expensive tantalum or bulk electrolytic capacitors

in the most demanding microprocessor applications. For example, a 200MHz Pentium® processor can operate with only the twenty-four  $1\mu\text{F}$  ceramic capacitors that Intel already requires for the microprocessor. Users realize significant savings because all additional bulk capacitance is removed. The additional savings of insertion cost, inventory cost and board space are readily apparent.

Precision-trimmed adjustable and fixed-output voltage versions accommodate any required microprocessor power supply voltage. Dropout voltage can be user defined via selection of the N-channel MOSFET  $R_{\text{DS(ON)}}$ . The only output capacitors required are the high frequency ceramic decoupling capacitors. The regulator responds to transient load changes in a few hundred nanoseconds—a great improvement over regulators that respond in many microseconds. The ceramic capacitor network generally consists of ten to twenty-four  $1\mu\text{F}$  capacitors, depending on individual microprocessor requirements. The LT1575/LT1577 family also incorporates current limiting at no additional system cost, provides on/off control and can provide overvoltage protection or thermal shutdown with the

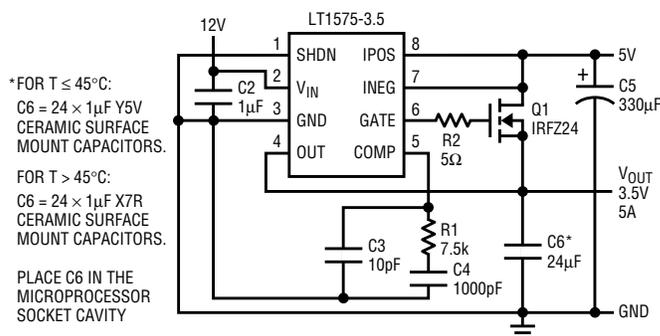


Figure 1. UltraFast transient response 5V to 3.5V, low dropout regulator

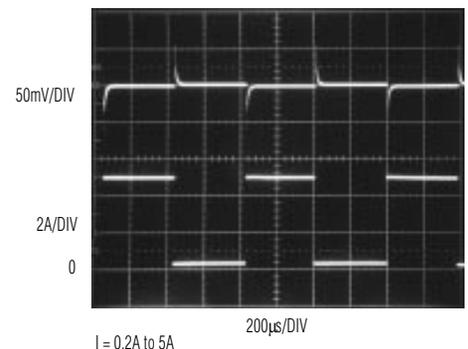


Figure 2. Transient response for 0.2A–5A output load step

addition of a few simple external components. The LT1575 is available in 8-pin SO or PDIP and the LT1577 is available in 16-pin narrow-body SO.

Figure 1 shows the basic regulator control circuit. The input voltage is a standard 5V "silver box" and the output voltage is set to 3.5V, the Pentium P54 VRE microprocessor supply voltage. The typical maximum output current is about 5A in most Pentium microprocessor applications. The output capacitor network consists of only twenty-four inexpensive 1 $\mu$ F ceramic, surface mount capacitors. Proper layout of this decoupling network is critical to proper operation of this circuit. Consult Linear Technology Application Note 69: *Using the LT1575 Linear Regulator Controller*, for details on board layout.

The photo in Figure 2 shows the transient response performance for an output load current step of 0.2A to 5A. The main loop compensation in Figure 1's regulator circuit is provided by R1 and C4 at the COMP pin. Capacitor C3 introduces a high frequency pole and provides adequate gain margin beyond the unity-gain crossover frequency of 1MHz. This compensation network limits overshoot/undershoot to 50mV under worst-case load transient conditions. With a 1% specified worst-case output voltage tolerance, the 100mV output voltage error budget for a P54 VRE microprocessor is easily met with production margin to spare. All bulk tantalum/electrolytic capacitors are completely eliminated.

The discrete N-channel MOSFET chosen is a low cost International Rectifier IRFZ24 or equivalent. The input capacitance is approximately 1000pF with  $V_{DS} = 1V$ . The specified on-resistance is 0.1 $\Omega$  at room temperature and about 0.15 $\Omega$  at 125°C. At 7A output current, the dropout voltage is only 1.05V. This eases the restriction on local input decoupling capacitor requirements because significant droop in the typical 5V input supply voltage is permitted before dropout voltage operation is reached. (Note that 5V supply tolerance

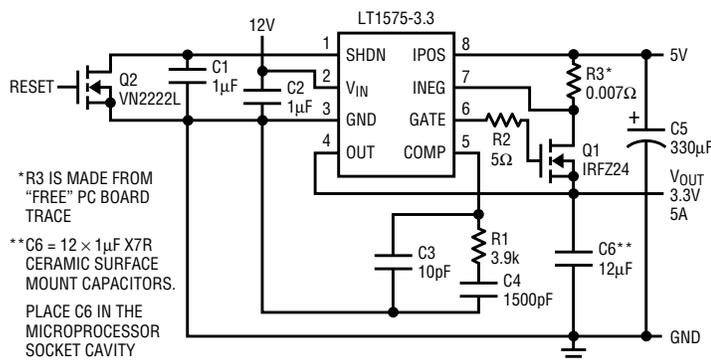


Figure 3. 5V to 3.3V regulator

restrictions are typically limited by a  $\pm 5\%$  tolerance so that 5V logic systems will operate correctly.) However, a simple LC input filter can eliminate the need for large input bulk capacitance at the regulator 5V supply for additional system cost savings.

Figure 3 shows a more complete system configuration that incorporates current limiting and current limit time-out with latch-off. Current limit is incorporated for no additional system cost by manufacturing the current limit resistor from a Kelvin-sensed section of pc board trace. In this example, current limit is set to 7A. A capacitor from the SHDN pin to ground sets a fault condition time-out period that latches off the drive to the external MOSFET if the time-out period is exceeded. The regulator is reset by pulling the SHDN pin low. The output voltage in this application is set to 3.3V. The  $\pm 5\%$  tolerance permitted in 3.3V systems translates to a  $\pm 165mV$  output-voltage tolerance. This permits a 50% reduction in the number of ceramic capacitors required from twenty-four to twelve. Loop compensation is adjusted accordingly.

Figure 4 shows an application circuit using the LT1577, a dual regulator. All functions for each regulator are identical to those of the LT1575. One section is configured for a 3.3V output and the other section is configured for a 2.8V output. This circuit provides all the power requirements for a split-plane system: 3.3V for the logic supply and 2.8V for the

processor-core supply. Both regulator sections use the resistorless current limit technique. This technique is discussed in detail below. Note that both SHDN pins are tied to a common time-out capacitor. If either or both regulators encounter a fault condition, both regulator sections are latched off after the time-out period is exceeded.

## Block Diagram Functional Description

Figure 5 is a block diagram of the fixed voltage LT1575. The primary block diagram elements comprise a simple feedback control loop and the secondary block diagram elements comprise multiple protection functions. A start-up circuit provides controlled start-up for the IC, including the precision-trimmed bandgap reference, and establishes all internal current and voltage biasing.

## Precision Reference/Output Voltage Performance

Reference voltage accuracy for the adjustable version and output voltage accuracy for the fixed-voltage versions are specified as  $\pm 0.6\%$  at room temperature and as  $\pm 1\%$  over the full operating temperature range. This places the LT1575/LT1577 family among a select group of regulators with very tightly specified output voltage tolerances. The accurate 1.21V reference is tied to the noninverting input of the main error amplifier in the feedback control loop.

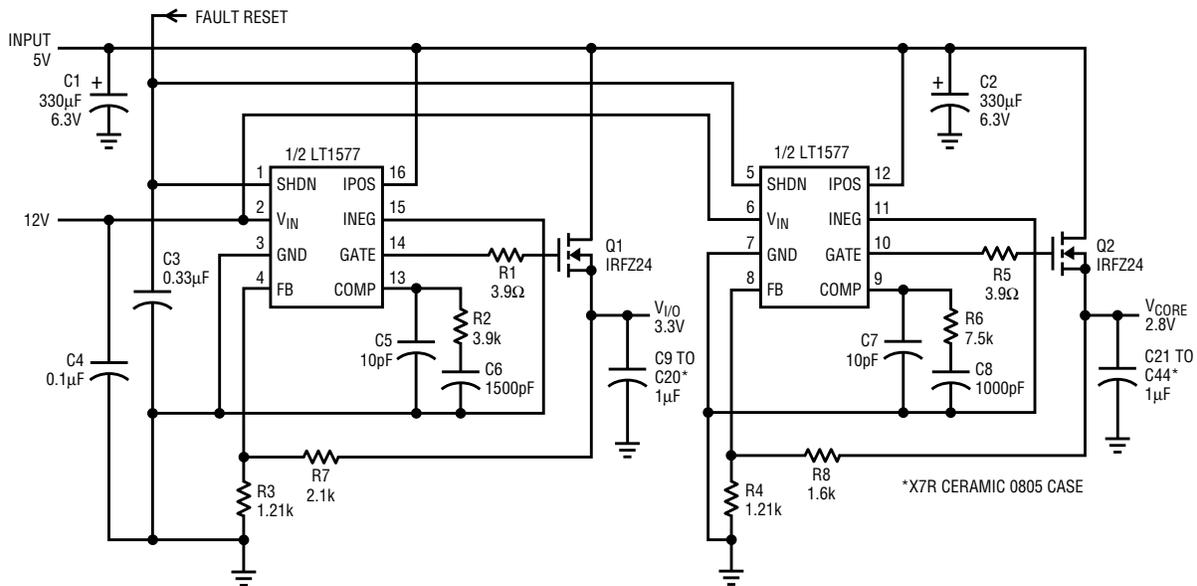


Figure 4. LT1577 dual regulator for split-plane systems

### Wide-Bandwidth Error Amplifier Permits Fast Loop Response

The error amplifier consists of a single high gain  $g_m$  stage with a transconductance equal to 15 millimhos. The inverting terminal is brought out as the FB pin in the adjustable voltage version and as the OUT pin in fixed voltage versions. The  $g_m$  stage provides differential-to-single-ended conversion at the COMP pin. The output impedance of the  $g_m$  stage is about 1M; therefore, 84dB of typical DC error amplifier open-loop gain ( $A_{VOL} = g_m R_O$ ) is realized along with a typical 75MHz uncompensated unity-gain crossover frequency. External access to the high impedance gain node of the error amplifier permits typical loop compensation to be accomplished with an RC network to ground.

A high speed, high current output stage buffers the COMP node and drives up to 5000pF of effective MOSFET gate capacitance with almost no change in load transient performance. The output stage delivers up to 50mA peak when slewing the MOSFET gate in response to load current transients. The output impedance of the GATE pin is typically 2Ω. This pushes the pole caused by the error-amplifier output impedance and the MOSFET input

capacitance well beyond the loop crossover frequency. If the capacitance of the MOSFET used is less than 1500pF, it may be necessary to add a small value series gate resistor of 2Ω–10Ω. This gate resistor helps damp the LC resonance created by the MOSFET gate's lead inductance and input capacitance. In addition, the high frequency pole formed by the gate resistor and the MOSFET input capacitance can be fine tuned.

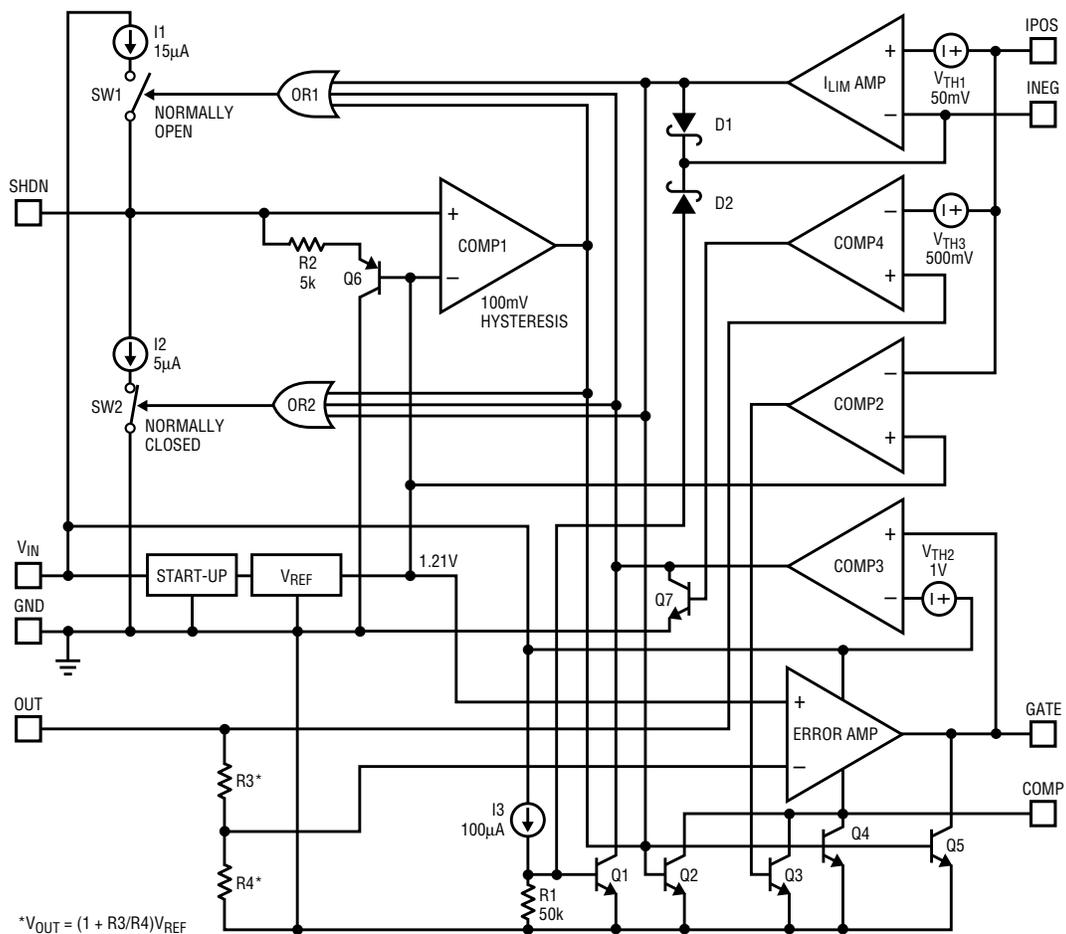
Because the MOSFET pass transistor is connected as a source follower, the power path gain is much more predictable than that of designs employing a discrete PNP transistor as the pass device. This is because of the significant production variations encountered with PNP beta. MOSFETs are also very high speed devices, and hence are more suitable than PNPs for creating a stable, wide-bandwidth control loop. An additional advantage of the follower topology is inherently good line rejection. Input supply disturbances do not propagate through to the output. The feedback loop for a regulator circuit is completed by providing an error signal to the FB pin in the adjustable voltage version and to the OUT pin in the fixed voltage version. In both cases, a resistor divider network senses the output voltage and sets the regulated DC bias point.

In general, the LT1575 regulator feedback loop permits a loop crossover frequency on the order of 1MHz while maintaining good phase and gain margins. This unity-gain frequency is a factor of twenty to thirty times the bandwidth of currently implemented regulator solutions for microprocessor power supplies. This significant performance benefit is what permits the elimination of all bulk output capacitance.

### High-Side Sense Current Limiting

Several other unique features included in the design increase its functionality and robustness. These functions comprise the remainder of the block diagram.

A high-side sense, current-limit amplifier provides active current limiting for the regulator. The current-limit amplifier uses an external low value shunt resistor connected in series with the external MOSFET's drain. This resistor can be a discrete shunt resistor or can be manufactured from a Kelvin-sensed section of free PC board trace. All load current flows through the MOSFET drain, and thus, through the sense resistor. The advantage of using high-side current sensing in this topology is that the MOSFET's gain and the main



**Figure 5. LT1575 block diagram**

feedback loop's gain remain unaffected. The sense resistor develops a voltage equal to  $I_{OUT} \times R_{SENSE}$ . The current-limit amplifier's 50mV threshold voltage is a good compromise between power dissipation in the sense resistor, dropout voltage and noise immunity. Current limit is activated when the sense resistor voltage equals the 50mV threshold.

Two events occur when current limit is activated: first, the current-limit amplifier drives Q2 in the block diagram and clamps the positive swing of the COMP node in the main error amplifier to a voltage that provides an output load current of  $50mV/R_{SENSE}$  (this action continues as long as the output current overload persists); second, a timer circuit is activated at the SHDN pin. This pin is normally held low by a 5µA active pull-down that saturates to approximately 100mV above ground. When current

limit is activated, the 5µA pull-down turns off and a 15µA pull-up current source turns on. Placing a capacitor in series with the SHDN pin to ground generates a programmable-time ramp voltage.

The SHDN pin is also the positive input of comparator COMP1. The negative input is tied to the internal 1.21V reference. When the SHDN pin ramps above  $V_{REF}$ , the comparator drives Q4 and Q5. This action pulls the COMP and GATE pins low and latches the external MOSFET drive off. This condition reduces the MOSFET power dissipation to zero. The time period until the latched-off condition occurs typically equals  $(C_{SHDN} \times 1.11V)/15\mu A$ . For example, a 1000pF capacitor on the SHDN pin yields a 74µs ramp time. In short, this unique circuit block performs a current-limit time-out function that latches off the regulator drive after a

predefined time period. The time-out period selected is a function of system requirements including start-up and safe-operating area. The SHDN pin is internally clamped to 1.85V (typical) by Q6 and R2. The comparator tied to the SHDN pin has typical hysteresis of 100mV to provide noise immunity. The hysteresis is especially useful when using the SHDN pin for thermal shutdown.

Normal operation can be restored after the load-current fault is cleared in one of two ways: recycle the nominal 12V LT1575 supply voltage (as long as an external bleed path for the shutdown pin capacitor is provided) or provide an active reset circuit that pulls the SHDN pin below  $V_{REF}$ . Pulling the SHDN pin below  $V_{REF}$  turns off the 15µA pull-up current source and reactivates the 5µA pull-down. If the SHDN pin is held below  $V_{REF}$  during a fault condition, the regulator contin-

ues to operate in current limit into a short. This action requires the ability to sink  $15\mu\text{A}$  from the SHDN pin at less than 1V. The  $5\mu\text{A}$  pull-down current source and the  $15\mu\text{A}$  pull-up current source are designed to be low enough in value that an external resistor divider network can drive the SHDN pin to provide overvoltage protection or to provide thermal shutdown with the use of a thermistor in the divider network. It is simple to diode-OR these functions together and obtain multiple functions from one pin.

### Senseless Current Limiting

If the current-limit amplifier is not used, two choices are available. The simplest choice is to tie the  $I_{\text{NEG}}$  pin directly to the  $I_{\text{POS}}$  pin. This action defeats current limit and provides the most basic circuit. An example of an application in which the current limit amplifier is not used is one in which an extremely low dropout voltage must be achieved and the 50mV threshold voltage cannot be tolerated.

A second available choice permits a user to provide short circuit protection with no external sensing. This technique is activated by grounding the  $I_{\text{NEG}}$  pin. This action disables the current limit amplifier because Schottky diode D1 clamps the amplifier's output and prevents Q2 from pulling down the COMP node. In addition, Schottky diode D2 turns off pull-down transistor Q1. Q1 is normally on and holds internal comparator COMP3's output low. This comparator circuit, which is now enabled, monitors the GATE pin and detects saturation at the positive rail. When it detects a saturated condition, COMP3 activates the shutdown timer. Once the time-out period occurs, the output is shut down and latched off. The operation of resetting the latch remains as described above.

Note that this technique does not limit the FET current during the time-out period. The output current is only limited by the input power supply and the input/output impedance. Output currents in the range of 50A–

100A are possible. Setting the timer to a short period in this mode of operation keeps the external MOSFET within its SOA (safe operating area) boundary and keeps the MOSFET's temperature rise under control.

### No Power Supply Sequencing Problems

The issue of power supply sequencing is important because the typical LT1575 application has inputs from two separate power supply voltages. A unique circuit design incorporated into the LT1575 alleviates all concerns about power supply sequencing. If the typical 12V  $V_{\text{IN}}$  supply voltage is slow in ramping up, insufficient MOSFET gate drive is present, and therefore the output voltage does not come up. If the  $V_{\text{IN}}$  supply voltage is present but the typical 5V supply voltage tied to the  $I_{\text{POS}}$  pin has not yet started, the feedback loop wants to drive the GATE pin to the positive  $V_{\text{IN}}$  rail. This will result in a very large MOSFET current as soon as the 5V supply starts to ramp up. However, undervoltage lockout circuit COMP2, which monitors the  $I_{\text{POS}}$  supply voltage, holds Q3 on and pulls the COMP pin low until the  $I_{\text{POS}}$  voltage rises above the internal 1.21 reference voltage. The undervoltage lockout circuit then smoothly releases the COMP pin and allows the output voltage to come up in dropout from the input supply voltage. An additional benefit derived from the speed of the LT1575 feedback loop is that turn-on overshoot is virtually nonexistent in a properly compensated system.

An additional circuit feature is built in to the LT1575 fixed-voltage versions. When the regulator circuit starts, it must charge the output capacitors. The output voltage typically tracks the input voltage supply as it ramps up with the input/output voltage difference defined by the dropout voltage. Until the feedback loop comes into regulation, the circuit operation results in the GATE pin being at the positive  $V_{\text{IN}}$  rail; this starts the timer if the current limit

amplifier is not used. However, internal comparator COMP4 monitors the input-output voltage differential. This comparator does not permit the shutdown timer to start until the differential voltage is greater than 500mV. This permits normal start-up.

### Fixed Voltage Versions Eliminate Precision Discrete Resistor Divider Networks

One final benefit results from using a fixed voltage version of the LT1575. Today's highest performance microprocessors dictate that precision resistors must be used with currently available adjustable-voltage regulators to meet the initial set point tolerance. The LT1575 fixed voltage versions incorporate the precision resistor divider network into the IC and still maintain a 1% output voltage tolerance over temperature. The LT1575 offers fixed voltage options of 1.5V (GTL+ termination), 2.8V (Pentium P55C), 3.3V, 3.5V (Pentium P54 VRE) and 5.0V.

### Conclusion

The unique design of the new LT1575/LT1577 family combines the benefits of low dropout voltage, high functional integration, precision performance and ultrafast transient response, as well as providing significant cost savings on the output capacitance needed in fast load-transient applications. As lower input/output differential voltage applications become increasingly prevalent, an LT1575-based solution achieves efficiency performance comparable to that of a switching regulator at appreciable cost savings.

The new LT1575/LT1577 family of low dropout regulator controller ICs steps to the next level of performance required by system designers for the latest generation of motherboards and microprocessors. The simple versatility and benefits derived from these circuits meets the power supply needs of today's high performance microprocessors with ease. 

# LTC1479 PowerPath Controller Simplifies Portable Power Management Design

by Tim Skovmand

As the computing power of portable equipment rises, increasing demands are placed on the portable power management system. The energy stored in the Li-Ion or NiMH battery packs must be transferred as smoothly and efficiently as possible to the input of the DC/DC switching regulator. These demands, coupled with the increased need for higher operating and charging currents, conspire to complicate the front end of the power management system—the so-called “power path.”

This is where the battery packs, the AC wall adapter, the battery charger and the standby system converge to create a power-management nightmare. The real world problems associated with the switching of power among these sources are often quite subtle and daunting, which may explain why the prevailing solutions are almost as varied as the portable equipment in which they reside. Many solutions require a large amount of

printed circuit board space and a considerable number of discrete components to implement—it is not uncommon to find an eclectic mixture of regulators, comparators, references, glue logic, MOSFET switches and drivers in the power path area of the circuit board.

Fortunately, some commonality has emerged among power-path switching schemes and the solutions to these real world problems have been integrated into a new family of power-management controllers that simplify the monitoring and switching of the batteries, the AC adapter, the battery charger and the standby system.

The LTC1479 PowerPath™ controller drives low loss N-channel MOSFET switches to direct power in the main power path of a dual rechargeable battery system, the type found in most notebook computers and other portable equipment.

Figure 1 is a conceptual block diagram that illustrates the main features of an LTC1479 dual-battery power management system, starting with the three main power sources and ending at the input of the DC/DC switching regulator.

Switches SWA/B, SWC/D and SWE/F direct power from either the AC adapter (DCIN) or one of the two battery packs (BAT1 and BAT2) to the input of the DC/DC switching regulator. Switches SWG and SWH connect the desired battery pack to the battery charger. These five switches are intelligently controlled by the LTC1479, which interfaces directly with the power management microprocessor.

## Back-to-Back Switches

Each of the simple SPST switches shown in Figure 1 actually consists of two back-to-back N-channel MOSFET switches. Figure 2 is a simplified schematic diagram, which shows only the three main power-path switches for

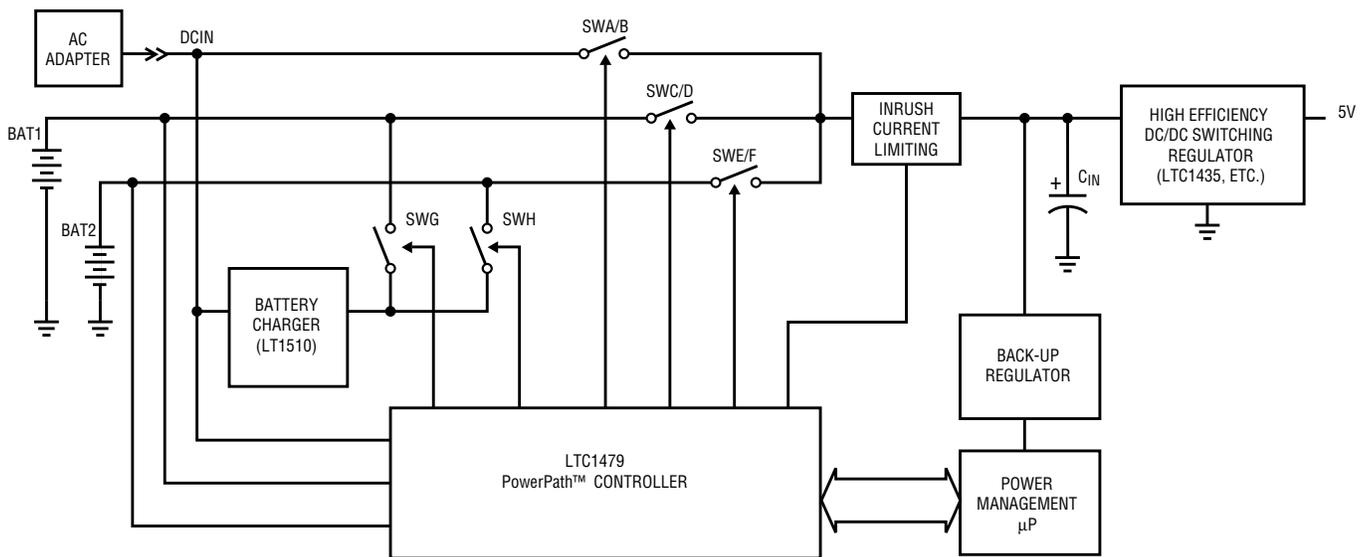


Figure 1. Dual PowerPath controller conceptual block diagram

descriptive purposes. The low loss, N-channel switch pairs are housed in 8-pin SO packaging and are readily available from a number of MOSFET manufacturers.

The back-to-back topology eliminates the problems associated with the inherent body diodes in power MOSFET switches and allows each switch pair to block current flow in both directions when the two halves are turned off.

### Inrush Current Limiting

The back-to-back topology also allows independent control of each half of the switch pair, and thus, the use of bidirectional inrush current limiting.

The voltage across a single low value resistor,  $R_{SENSE}$ , is measured to determine the instantaneous current flowing through the three main switch pairs, SWA/B, SWC/D, and SWE/F. The inrush current is then controlled by the gate drivers until the transition from one power source to another has been completed. The current flowing in and out of the three main power

sources and the DC/DC converter input capacitor is dramatically reduced.

### Tantalum Capacitors

In many applications, inrush current limiting makes it feasible to use low profile tantalum surface mount capacitors in place of bulkier electrolytic capacitors at the input of the DC/DC converter.

### Built-In Step-Up Regulator

The gate drive for all five low loss N-channel switches is supplied by a micropower step-up regulator, which continuously generates 37V. The  $V_{GG}$  supply provides sufficient headroom above the maximum 30V operating voltage of the three main power sources to ensure that the logic-level MOSFET switches are fully enhanced by the gate drivers, which supply a regulated 5.7V gate-to-source voltage,  $V_{GS}$ , when turned on.

The power for the micropower boost regulator is taken from three internal

diodes connected to each of the three main power sources—DCIN, BAT1 and BAT2. The highest voltage potential is directed to the top of an inexpensive 1mH surface mount inductor, L1.

A fourth internal diode directs the current from L1 to the  $V_{GG}$  output capacitor, C2, further reducing the external parts count. In fact, only three external components are required by the  $V_{GG}$  regulator: L1, C1 and C2.

### Typical Application Circuit

A typical dual Li-Ion battery power management system is illustrated in Figure 3. If “good” power is available at the DCIN input (from the AC adapter), both MOSFETs in switch pair SWA/B are on—providing a low loss path for current flow to the input of the LTC1538-AUX DC/DC converter. Switch pairs SWC/D and SWE/F are turned off to block current from flowing back into the two battery packs from the DC input.

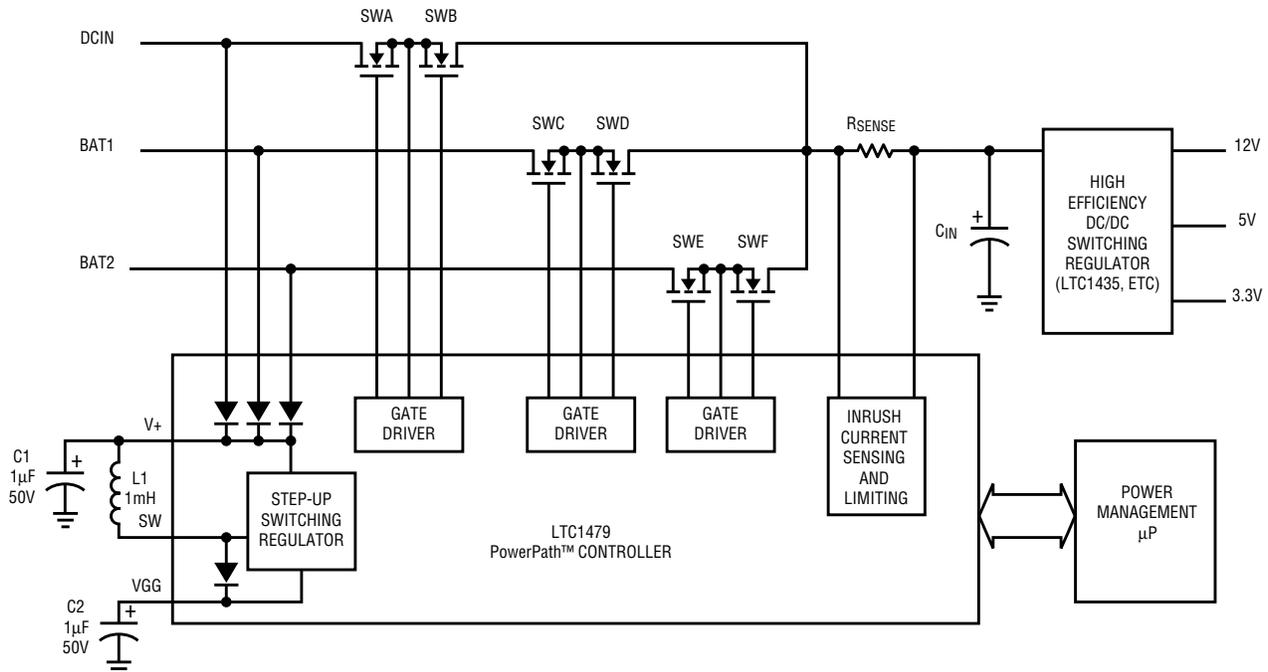


Figure 2. Dual-battery PowerPath™ controller:  $V_{GG}$  regulator, inrush limiting and switch gate drivers

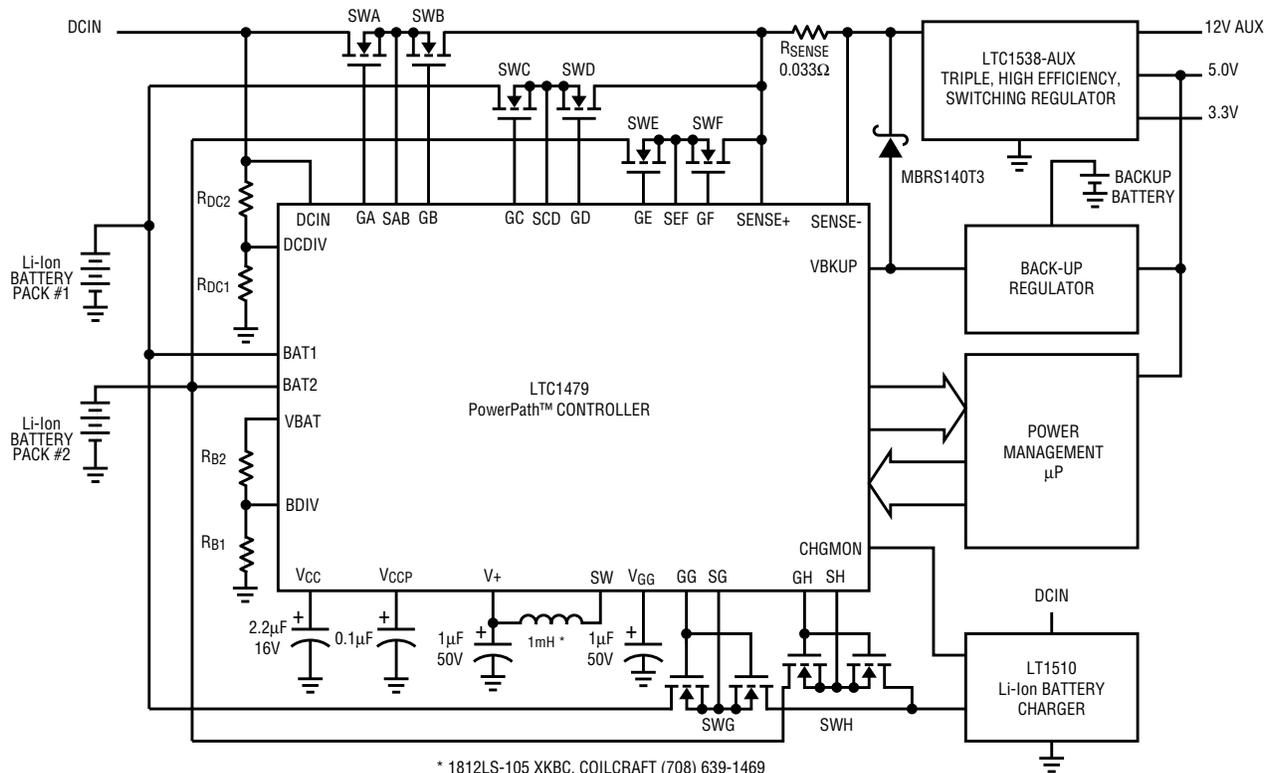


Figure 3. Dual Li-Ion battery power-management system (simplified schematic)

### Battery Charging

The LTC1479 works equally well with both Li-Ion and NiMH batteries and chargers. In this application, an LT1510 constant-voltage, constant-current (CC/CV) battery charger circuit is used to alternately charge two Li-Ion battery packs.

The power management microprocessor decides which battery is in need of recharging by either querying a smart battery pack directly or by more indirect means. After the determination is made, switch pair SWG or SWH is turned on by the LTC1479 to pass charger current to one of the batteries. Simultaneously, the selected battery voltage is returned to the voltage feedback input of the LT1510 CV/CC battery charger via a built-in switch in the LTC1479.

After the first battery is charged, it is disconnected from the charger circuit. The second battery is then connected through the other switch

pair and the second battery is charged. (The LTC1479 works equally well with the LT1511 3A CC/CV Battery Charger and LTC1435/LT1620 4A CC/CV Battery Charger.)

### Running on Batteries

When the AC adapter is removed, the LTC1479 instantly informs the power management microprocessor that the DC input is no longer “good” and the desired battery pack is connected to the input of the LTC1538-AUX high efficiency switching regulator through either switch pair SWC/D or SWE/F.

### Back-Up Power and System Recovery

Backup power is provided by a standby switching regulator, which is typically powered from a small rechargeable battery and ensures that the DC/DC input voltage does not drop below a predetermined level (for example, 6V).

### The “Three Diode Mode”

When the system is powered by the backup regulator, the LTC1479 enters a unique operating state called the “three diode mode,” as illustrated in Figure 4. Under normal operating conditions, both halves of each switch pair are turned on and off simultaneously. For example, when the input power source is switched from a good DC input (AC adapter) to a good battery pack, BAT1, both gates of switch pair SWA/B are turned off and both gates of switch pair SWC/D are turned on. The back-to-back body diodes in switch pair SWA/B block current flow in or out of the DC input connector.

In the three diode mode, only the first half of each power path switch pair, that is, SWA, SWC and SWE, is turned on; and the second half, that is, SWB, SWD and SWF, is turned off. These three switch pairs now act as three diodes connected to the three main input power sources. The power

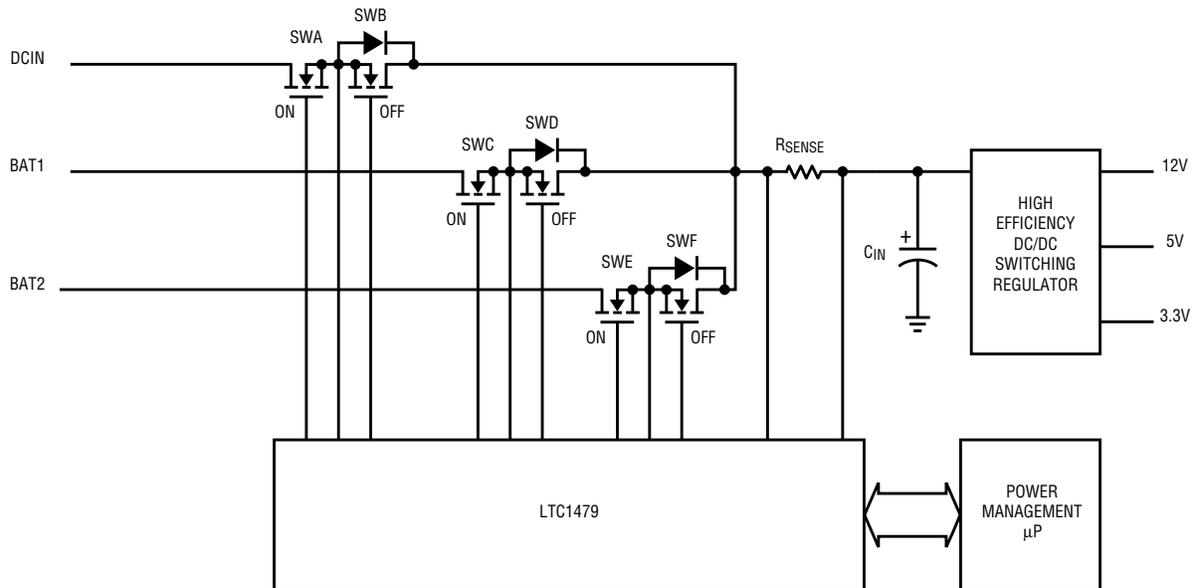


Figure 4. LTC1479 PowerPath™ controller in “three diode mode”

## The Power Management Microprocessor

The power management microprocessor provides intelligence for the overall power system, and is easily programmed to accommodate the custom requirements of each system and to allow performance updates without resorting to costly hardware changes. Many inexpensive microprocessors are available that can easily fulfill these requirements.

## Conclusion

The LTC1479 is the “heart” of a total power management solution for single- and dual-battery notebook computers and other portable equipment. It works in concert with other Linear Technology power management products, such as the LTC1435 family of high efficiency DC/DC converters and the LT1510 family of battery chargers to end your power-management nightmares. The LTC1479 is available in 36-lead SSOP packaging. 

path diode with the highest input voltage passes current through to the input of the DC/DC converter to ensure that the system cannot lock up regardless of how power is initially applied.

After “good” power is reconnected to one of the three main inputs, the LTC1479 drives the appropriate switch pair on fully as the other two are turned off, restoring normal operation.

## Interfacing to the Power Management Microprocessor

The LTC1479 takes logic level commands directly from the microprocessor and makes changes at high current and high voltage levels in the power path. Further, it provides information directly to the microprocessor on the status of the AC adapter, the batteries and the charging system.

The LTC1479 logic inputs and outputs are TTL level compatible and therefore interface directly with standard power management microprocessor. Because of the direct interface via five logic inputs and two logic outputs, there is virtually no latency (time delay) between the microprocessor and the LTC1479. In this way, time-critical decisions can be made by the microprocessor without the inherent delays associated with bus protocols and the like. These delays are acceptable in certain portions of the power management system, but it is vital that the power path switching control be made through a direct connection to the power management microprocessor. The remainder of the power management system can be easily interfaced to the microprocessor through either parallel or serial interfaces.

# New Rail-to-Rail Amplifiers: Precision Performance from Micropower to High Speed

by William Jett and Danh Tran

## Introduction

Linear Technology's latest offerings expand the range of rail-to-rail amplifiers with precision specifications. Rail-to-rail amplifiers present an attractive solution for signal conditioning in many applications. For battery-powered or other low voltage circuitry, the entire supply voltage can be used by both input and output signals, maximizing the system's dynamic range. Circuits that require signal sensing near the positive supply are straightforward using a rail-to-rail amplifier. Linear Technology's family of rail-to-rail amplifiers satisfies the need for rail-to-rail outputs and provides precision input-offset specifications. Because, for rail-to-rail applications, input offset is important across the entire common mode range, LTC's family of amplifiers uses a proprietary trim scheme that minimizes the input offset at two common mode voltages, equal to the positive and negative supplies. To make design using the devices straightforward, the offset voltage under these two conditions is clearly defined on the data sheet.

## Rail-to-Rail Op Amp Family

The latest additions to LTC's family of precision rail-to-rail op amps span the range of applications from micropower to high speed. All members of the family have both rail-to-rail input and output capability. The fastest members of the family, the LT1498/LT1499 C-Load™ op amps feature a 10MHz gain-bandwidth product, a slew rate of 4V/μs and the ability to drive 10,000pF. For low current applications, the LT1466-69 series supplies precision performance with a quiescent current of only 50μA per amplifier. Finally, the most accurate members of the family, the LT1218/LT1219, feature  $V_{OS}$  trimmed to less than 100μV, the tightest  $V_{OS}$  spec among LTC's rail-to-rail amps.

These devices combine precision with low voltage operation, operating with supplies as low as 2.2V, and are fully specified for 3V operation. The input offset voltage is less than 475μV for the LT1466 and LT1498 and less than 100μV for LT1218. In keeping with the precision nature of the parts, the open loop gain  $A_{VOL}$  is one million or greater driving a 10k load. The rail-

to-rail operation is fully specified and tested over the entire supply range. The input offset voltage and input bias currents are specified at common mode voltages equal to both  $V_{CC}$  and  $V_{EE}$ .

The LT1466-69 and the LT1218/LT1219 are offered in two versions, which differ in their frequency compensation. The LT1466 dual and LT1467 quad and the LT1218 single have conventional compensation. For use in low frequency or DC applications, the LT1468 dual, LT1469 quad, and LT1219 single are C-Load amplifiers, compensated for use with a 0.1μF capacitor at the output. In a noisy environment, the large output capacitor cleans up the output signal by improving the supply rejection and providing a low output impedance at high frequencies.

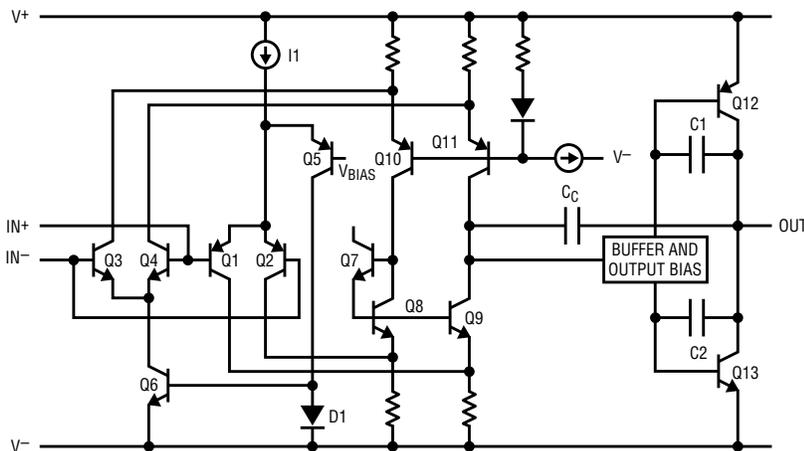


Figure 1. Rail-to-rail amplifier simplified schematic

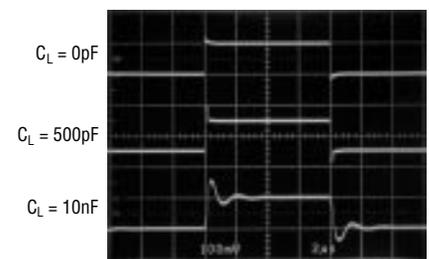


Figure 2. LT1498 small signal response



Figure 3. LT1498 large signal response

**Table 1. Amplifier performance:  $V_S = 5V$ ,  $25^\circ C$** 

Parameter	LT1466 Dual	LT1218 Single	LT1498 Dual
Supply Current per Amplifier	50 $\mu A$	400 $\mu A$ 10 $\mu A$ shutdown	1.7mA
Gain Bandwidth Product	100kHz	400kHz	10MHz
Slew Rate	0.03V/ $\mu s$	0.11V/ $\mu s$	4V/ $\mu s$
Offset Voltage, $V_{CM} = V_{EE}, V_{CC}$	<475 $\mu V$	<100 $\mu V$	<475 $\mu V$
Open Loop Gain ( $R_L = 10k$ )	1V/ $\mu V$	1V/ $\mu V$	2V/ $\mu V$
Input Bias Current, $V_{CM} = V_{EE}, V_{CC}$	5nA	25nA	250nA
Input Offset Current, $V_{CM} = V_{EE}, V_{CC}$	1nA	6nA	20nA
Output Saturation Voltage No Load $I_O = 2.5mA$	30mV 275mV	6mV 200mV	15mV 200mV
Short Circuit Current	20mA	15mA	20mA
Operating Supply Voltage Range	2.2V to 12V	2.2V to 12V	2.0V to $\pm 15V$
Specified Supply Voltages	3V, 5V, $\pm 5V$	3V, 5V, $\pm 5V$	3V, 5V, $\pm 15V$

contained in this stage. The output of the second stage is then buffered and applied to the output devices Q12 and Q13. Capacitors C1 and C2 form local feedback loops around the output devices, lowering the output impedance at high frequencies. Capacitor  $C_C$  sets the amplifier bandwidth.

## Performance

Table 1 summarizes the performance of the newest rail-to-rail amplifiers. As mentioned earlier, input offset voltage and bias currents are tested with the input common mode voltages at both  $V_{EE}$  and  $V_{CC}$ .

## The LT1498/LT1499—10MHz Bandwidth and C-Load Performance

The LT1498/LT1499 are the highest frequency members of the LTC's precision rail-to-rail amplifier family, featuring a 10MHz gain-bandwidth and a 4V/ $\mu s$  slew rate. Designed for ease of use, the LT1498/LT1499 are C-Load amplifiers, stable at unity gain when loaded with up to 10nF. Both the small signal and large signal transient response with a capacitive load are well behaved. Figures 2 and 3 illustrate the stability of the devices for small signal and large signal conditions.

## Applications

The ability to accommodate any input or output signal that falls within the amplifier supply range makes these amplifiers very easy to use. The following applications demonstrate the versatility of the family of amplifiers. *continued on page 37*

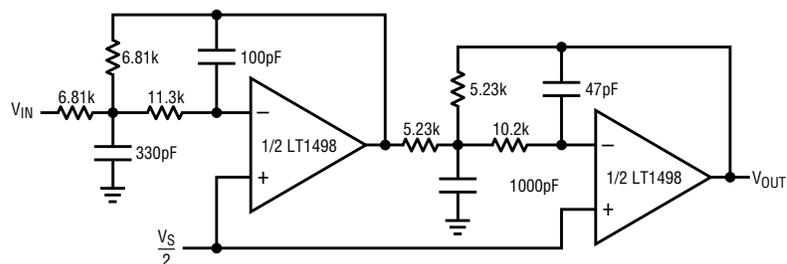
The devices are available in a variety of package options. The LT1466, LT1468 and LT1498 are dual amplifiers, available in either 8-pin SO or 8-pin miniDIP packages. The LT1467, LT1469 and the LT1499 are quad amplifiers available in the 14-pin SO only. The LT1218 and LT1219 are single amplifiers with a shutdown function, available in 8-pin SO and 8-pin miniDIP packages.

## The Rail-to-Rail Architecture

Though the new rail-to-rail amplifiers described differ in detail, they share a common approach to the input and output stages. Figure 1 shows a simplified schematic. The input stage consists of two differential amplifiers, a PNP stage Q1-Q2 and an NPN stage Q3-Q4, which are active over different portions of the input common mode range. Each input stage is trimmed for offset voltage. A complementary output configuration (Q12-Q13) is employed to create an output stage with rail-to-rail swing. The devices are fabricated on Linear Technology's proprietary complementary bipolar process, which ensures very similar DC and AC characteristics for the output devices Q12 and Q13.

First, looking at the input stage, Q5 switches the current from current source I1 between the two input stages. When the input common mode voltage  $V_{CM}$  is near the negative supply, Q5 is reverse biased, so the current from I1 becomes the tail current for the PNP differential pair Q1-Q2. At the other extreme, when  $V_{CM}$  is near the positive supply, PNPs Q1-Q2 are biased off. The current from I1 then flows through Q5 to the current mirror D1-Q6, furnishing the tail current for the NPN differential pair Q3-Q4. The switchover point between stages occurs when  $V_{CM}$  is equal to the base voltage of Q5, which is biased approximately 1.3V below the positive supply.

The collector currents of the two input pairs are combined in the second stage, consisting of Q7-Q11. Most of the voltage gain in the amplifier is

**Figure 4. 100kHz 4th order Butterworth filter**

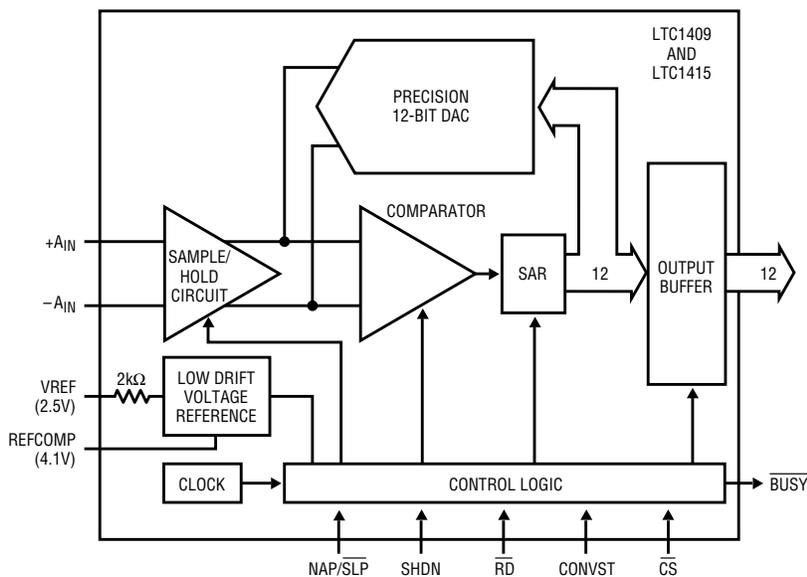


Figure 1. LTC1409 and LTC1415 block diagram

LTC1409/LTC1415, continued from page 1  
fast successive-approximation ADC. Supporting these high speed circuits is an onboard voltage reference, power-saving shutdown circuitry and an easy to use parallel digital interface. This interface easily connects to FIFOs, microprocessors and DSPs.

To increase interface flexibility, both devices have a digital  $V_{CC}$  that powers only the output-logic circuitry, easing connection to a 3V host processor. This allows the analog conversion to operate on 5V, maximizing the dynamic range and SINAD, while the conversion data's logic levels are compatible with the host processor's 3V logic.

**DC and AC Performance**

The DC specifications include a  $\pm 0.8$ LSB maximum differential linearity error and  $\pm 0.5$ LSB maximum integral linearity error guaranteed over temperature. The ADCs' gain is held constant over temperature with an on-chip 10ppm/ $^{\circ}$ C curvature-corrected bandgap reference.

The sample-and-hold used in the LTC1409 and LTC1415 determines their dynamic performance. These ADCs have a wide bandwidth and very low distortion differential sample and hold. Dynamic performance specifications include THD of  $-84$ dB for a 625kHz input and a sample-and-hold input bandwidth of 30MHz.

Figure 2 shows the wideband integrity of the LTC1409's conversion. This curve shows that the effective number bits (ENOB) is 11.8 and remains flat out to an input frequency of 200kHz. Even at 1MHz, the LTC1409 maintains 11-bit performance.

An FFT of the performance of the LTC1415 operating at full conversion rate of 800ksps is shown in Figure 3. The input signal is a full-scale 100kHz sine wave. The curve shows excellent response with a low noise floor while sampling at 800ksps.

The LTC1409 and the LTC1415 have vanishingly low bit-error rates. The error rates are so low that measuring them is very difficult. To begin to uncover the error's characteristics,

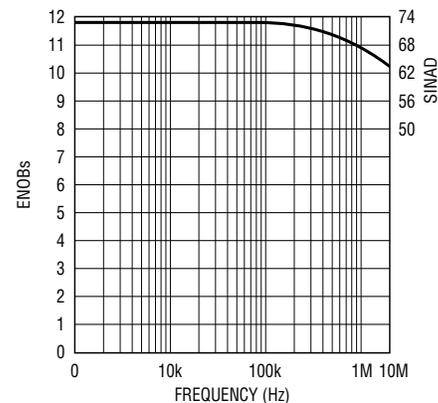


Figure 2. This curve shows that the dynamic performance of the LTC1409 remains robust out to an input frequency of 1MHz, where it maintains 11-bit performance.

measurements were made at an elevated temperature of 150 $^{\circ}$ C (bit-error rates increase with increasing temperature). Even at this high temperature, the bit-error rate was found to be less than one in 100 billion ( $10^{-11}$ ). At room temperature, the bit-error rate is projected to be less than one in 2,000,000 billion ( $2 \times 10^{-15}$ ). To understand the magnitude of this error, consider that the LTC1409 or the LTC1415, operating at full conversion rate, would be free of bit errors for at least 50 or 78 years, respectively.

**Flexible Reference**

Figure 4 shows a simplified circuit diagram of the reference circuitry found in the LTC1409 and LTC1415. The reference's temperature coefficient is 10ppm/ $^{\circ}$ C, making it suitable as a system reference. This allows other circuits using this reference to track each other over

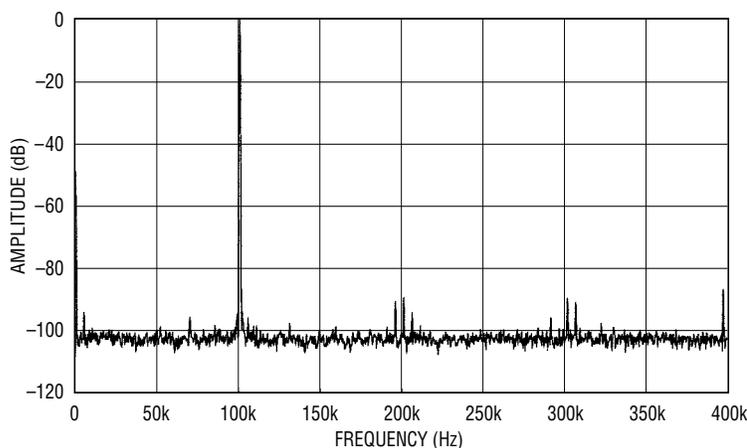


Figure 3. FFT of the LTC1415's conversion of a full-scale 100kHz sine wave shows excellent response with a low noise floor while sampling at 800ksps.

temperature. When this internal reference is used to set the full-scale range ( $\pm 2.5V$  for the LTC1409 and  $0V$  to  $5V$  for the LTC1415), pin 3 is left unconnected and a  $10\mu F$  tantalum electrolytic is connected between REFCOMP and AGND. The circuit in Figure 5 can be used to trim the full-scale (gain) error.

When an external reference is used, it can be connected in one of two ways, depending on its magnitude. If the external reference voltage is between  $2.5V$  and  $3.0V$ , the  $V_{REF}$  pin can be used. The REFCOMP pin can accept reference voltages in the range of  $2.5V$  to  $5.0V$ . The  $V_{REF}$  pin is appropriate for applications that have a fixed reference or, if the reference voltage is changed, can tolerate slow settling times. For applications such as scanners, which require fast response to changing reference voltages, the REFCOMP pin should be used as the reference input. Because the internal reference amplifier is bypassed, the settling time for changing reference voltages is limited by the size of the external bypass capacitor. When the REFCOMP pin is driven by an op amp, the filter capacitor can be eliminated. In this case, the settling time is a function of the op amp.

### Differential Inputs Cancel Wideband Common Mode Noise

Unwanted noise is a problem for most circuits. The problem of noise becomes increasingly acute when dealing with high speed, high resolution ADCs. An LSB's magnitude decreases with increasing resolution. At a resolution of 12 bits, the LSB is just  $1.22mV$  for a  $5V$  full-scale input range. Noise from fluorescent lights, electrical motors or digital circuits can quickly combine to create unwanted signals whose magnitude approaches a level that creates conversion errors. Although filtering and shielding signal lines will reduce the effects of noise, these techniques are sometimes inadequate or may limit bandwidth. The LTC1409 and the LTC1415 offer another weapon in the fight against the debili-

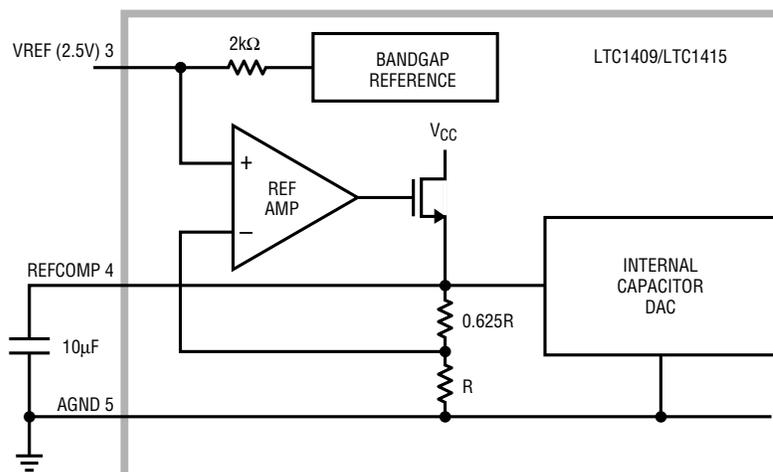


Figure 4. Flexible reference allows use of internal or external reference source

tating effects caused by noise: differential inputs.

Figure 6 shows a typical single-ended sampling system whose input signal is contaminated by ground noise. This noise may be a combination of  $60Hz$ , digital clock noise and/or EMI. This ground noise adds directly to the input signal. When the single-ended system samples this signal, the final conversion result is a combination of the actual desired signal and the unwanted noise.

The single-ended system cannot differentiate between the desired signal and the noise. The resulting conversion result is not correct.

Figure 7 shows the differential inputs of the LTC1409 and the LTC1415. These differential inputs overcome this problem of ground noise. Since the differential inputs are connected across the signal source, ground noise is common

mode. The ADC's excellent common mode rejection ratio (CMRR) rejects the common mode ground noise and the perturbations it creates in the conversion result. The CMRR is constant over the entire Nyquist bandwidth ( $f_s/2$ ) and drops  $3dB$  at  $5MHz$ . This ability to reject high frequency common mode signals is very helpful in sampling systems where noise often has high frequency components caused by switching transients. Additionally, the differential inputs reject in-band common mode noise, something that is much more difficult to achieve with filters, and preserve the LTC1409's and LTC1415's wide bandwidth capabilities.

The LTC1409 and LTC1415 are especially appropriate for applications that require low power and high conversion rates. To conserve additional power, the typical power dissipation of  $80mW$  (LTC1409) or  $60mW$

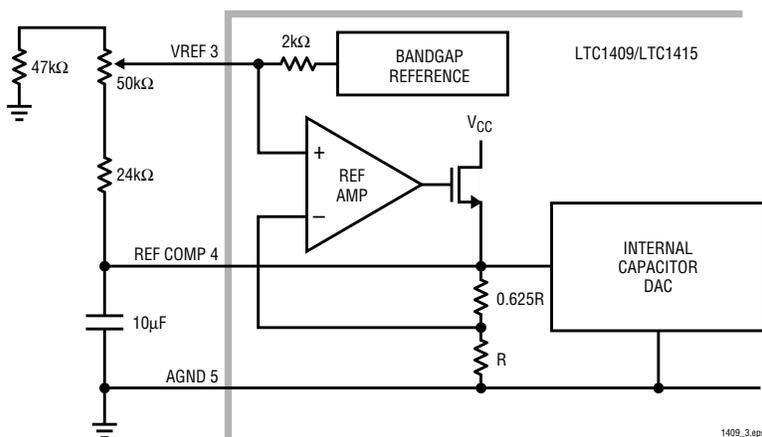
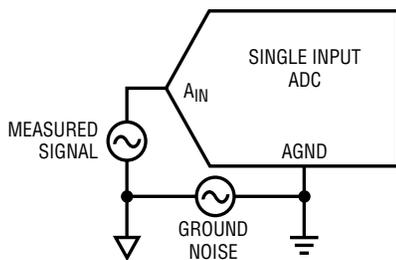
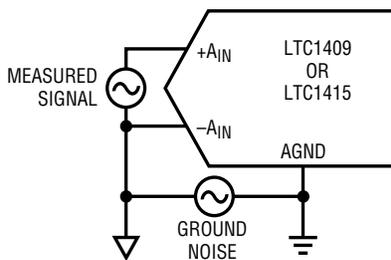


Figure 5. This simple circuitry facilitates full-scale trim and adds nothing to the signal path.



**Figure 6. A single-ended ADC is not able to differentiate the desired signal from the error-inducing ground noise, losing signal integrity.**

(LTC1415) can be significantly reduced during periods between conversions using the two shutdown modes. The NAP/SLP pin is used to select one of the two power reduction shutdown modes. The Nap mode saves 95% of the typical power dissipation. In Nap mode, the LTC1409 and the



**Figure 7. The LTC1409's and LTC1415's excellent broadband CMRR cancels common mode noise, preserving the input signal's integrity.**

LTC1415 reduce the bias current of all internal circuitry, except the reference, to zero. This mode allows the part to return from shutdown as quickly as possible by leaving the reference circuitry operational. The Sleep mode shuts down the bias current to all internal circuitry, including

the reference. Sleep mode saves the greatest amount of power, but requires more time to awaken than the Nap mode.

In the Nap mode, all data output controls are functional: data from the last conversion prior to starting Nap mode is still available and can be read using RD and CS.

## Conclusion

The newest members of LTC's high speed 12-bit family offer effective solutions to many dynamic sampling applications. These include high-speed telephony, compressed video and high frequency data acquisition. The LTC1409 and the LTC1415 offer an unbeatable combination of high speed and low power dissipation. **LT**

*LTC1553, continued from page 8*

Generally speaking, low ESR, high value output capacitors should be chosen to optimize the use of board space. However, if the ESR value is too low for a given capacitor value, loop stability problems can occur. The feedback loop depends on the frequency of the ESR "zero" being well below the loop crossover frequency. (You remember poles and zeros from your bumpy rides on the S-Plane, don't you?) There is 45° of positive phase shift at the frequency where the capacitive reactance equals the ESR of the capacitor. Without this phase shift, the loop would be impossible to stabilize. Low ESR, AVX TPS-series tantalum capacitors are a very good compromise between ESR, capacitance value and physical size.

Input capacitors are included to suppress the input switching noise and to keep the input 5V supply variation to a minimum during the Q1 ON/OFF cycle. Excessive conducted emissions are usually traced back to inadequate input capacitance or poor layout of the power-path traces. The crucial parameter for the input capacitors is ripple current rating. A reasonable rule of thumb says that

the input capacitor ripple current is going to be approximately 50% of the load current. Therefore, in a typical Pentium Pro processor application, the input capacitors should be rated for close to  $7A_{RMS}$ . An excellent choice for the input capacitors are Sanyo OS-CONs or the equivalent. They have extremely high ripple current ratings for their size and have demonstrated excellent reliability in this type of application. Low ESR aluminium electrolytic capacitors are a viable option from both input and output. Although lower in cost than OS-CONs or tantalum capacitors, their long-term reliability is not as good. Using 105°C capacitors and keeping operating temperatures low will help to obtain reasonable capacitor life.

The combination of the Dale NTHS-1206N02 thermistor and the 1.8k resistor are for overtemperature monitoring. The OT flag trips if the ambient temperature at Q1 reaches about 90°C; at 100°C the G1 and G2 drivers stop operating. If the system monitors the OT flag, there should be ample time to take precautions, saving data and system configuration information prior to an overtemperature

shutdown. Alternatively, CPU activity could be reduced, lowering power supply current and allowing the supply to cool down.

The PWRGD pin gives the CPU rail-voltage OK indication. If, for any reason, the output regulation falls out of the ±5% limit (including an overtemperature shutdown), PWRGD will provide a logic low signal to the system monitor.

## Conclusion

The LTC1553 is designed to be used in all N-channel, synchronous buck switching regulators for Pentium Pro and other high performance microprocessors. A high level of integration holds external parts count to a minimum, while providing a flexible solution. High efficiency can be achieved, eliminating the need for heat sinks in applications with currents as high as 14 amps steady state. All required system monitoring functions are supplied on chip. Component count and cost are reduced by eliminating the need for low resistance, high power, current sense resistors. **LT**

# High Efficiency, Low Dropout Lithium-Ion Battery Charger Charges Up to Five Cells at 4 Amps or More

by Fran Hoffart

## Introduction

Rechargeable lithium batteries feature higher energy density per volume, higher energy density per weight and higher voltage per cell than any of the competing battery chemistries. For these reasons, manufacturers of portable equipment are adopting the lithium-ion rechargeable battery as the battery of choice for high performance portable equipment. Lighter weight and increased operating time between charges are important features that customers want and need from portable products.

Laptop computers are one of many areas where rechargeable lithium batteries are rapidly replacing other battery types. Today's laptops feature faster microprocessors, more memory, larger back-lit liquid crystal displays, larger hard disks and more built-in features than ever before. At the same time, laptop manufacturers are striving to reduce the size and weight of

their products. These advances place increased energy demands on the battery.

These increased demands have forced manufacturers to use multiple cells in a combination of series and parallel configurations. Paralleling cells increases the amount of current that can be drawn from the battery and/or increases the operating time between charges, but it also increases the current requirements of the charger.

## Linear Technology Battery Charger Products

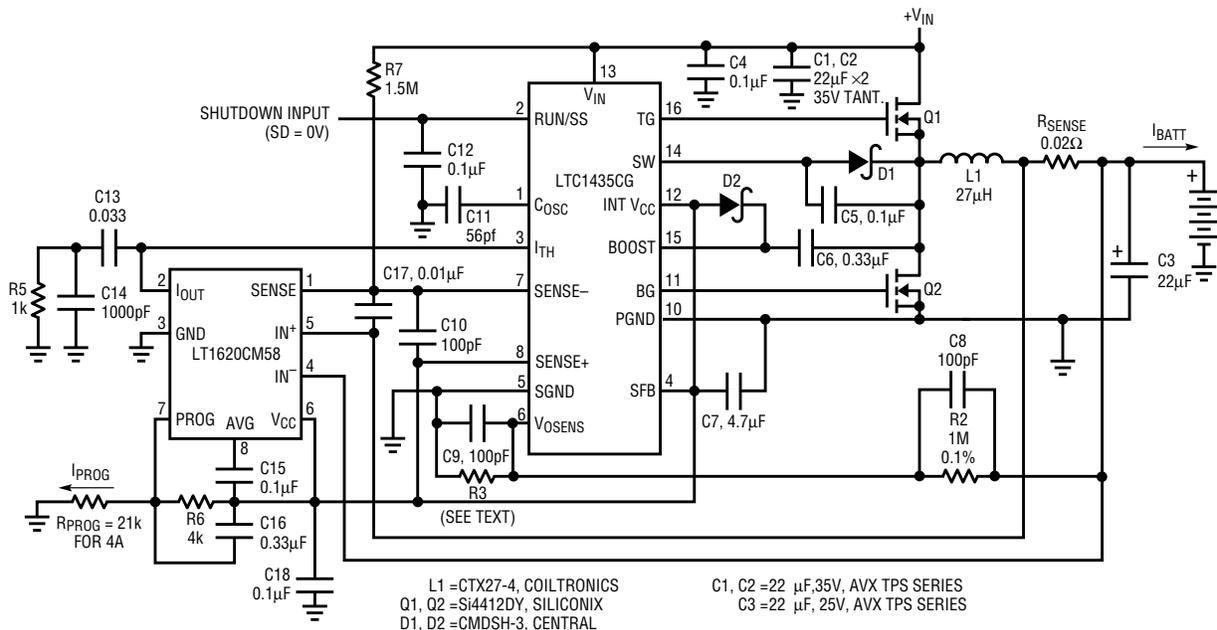
Linear Technology offers several dedicated switch-mode battery charger ICs with charging capabilities up to 3A. For step-down applications, the LT1510, operating at 200kHz, can provide up to 1.5A of charging current in a constant-current and/or constant-voltage mode. For currents

up to 3A, the LT1511 is available. In addition to a constant-current/constant-voltage charge, the LT1511 also features a programmable current limit on the input side of the charger. This allows the input power source (AC adapter) to power a load, such as a laptop computer, and charge a battery simultaneously, without overloading the input power source.

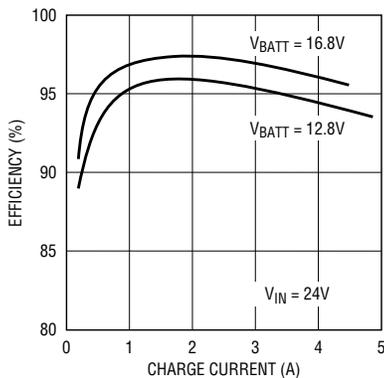
Two 500kHz chargers designed for SEPIC (single-ended primary inductance converter) topology are also available. The SEPIC design allows the input voltage to be less than, equal to or greater than the battery voltage. The LT1512 (1.5A) and LT1513 (3A) can be used in a constant-current/constant-voltage mode.

## Higher Charge Currents

Paralleling cells, regardless of cell chemistry, requires relatively high charge currents to bring the battery



**Figure 1. Complete schematic of high efficiency, 4A constant-voltage/constant-current charger using all surface mount components, with a circuit board area of 1.5 in<sup>2</sup>**



**Figure 2. Charger efficiency for 3- and 4-cell applications**

up to full charge in a short period of time. When charging needs exceed the 3A maximum rating of the LT1511 or LT1513, the circuit shown in Figure 1 can provide much higher current solutions, and very high efficiency. This circuit uses the LTC1435 and LT1620 in a charger that delivers 4A or more with exceptional efficiency and low dropout voltage (Figures 2 and 3).

### The LTC1435 Switching Regulator Controller

The LTC1435 is a step-down current mode switching regulator controller designed to drive two external N-channel power MOSFETs. Operating from input voltages between 3.5V and 36V, this device includes a programmable switching frequency, synchronous

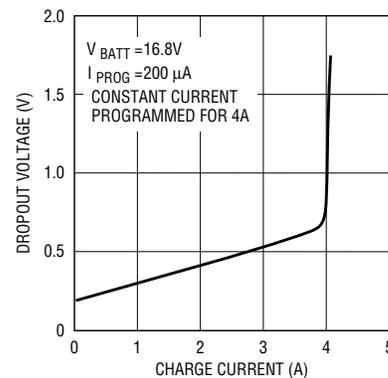
rectification, Burst Mode™ operation and a 99% maximum duty cycle for low dropout voltage. Additional features include a 1% tolerance output voltage (adjustable between 1.2V and 9V), programmable soft start, logic-controlled micropower shutdown and a secondary feedback control pin. Because external MOSFET switches are used, the maximum output load current is determined by the current capabilities of the selected FETs.

### The LTC1435 as a Battery Charger

The low dropout voltage, high current capability and high efficiency of the LTC1435 switching regulator would seem to make it an appropriate choice for high current battery chargers, but it has several limitations. The absolute maximum output voltage of 10 volts allows only two series-connected lithium cells to be charged and the output current is not readily programmable.

### Introducing the LT1620

The LT1620 is an IC designed to be used with a current mode PWM controller (such as the LTC1435 and similar products) to increase the output voltage range and optimize the circuit for battery charging applica-



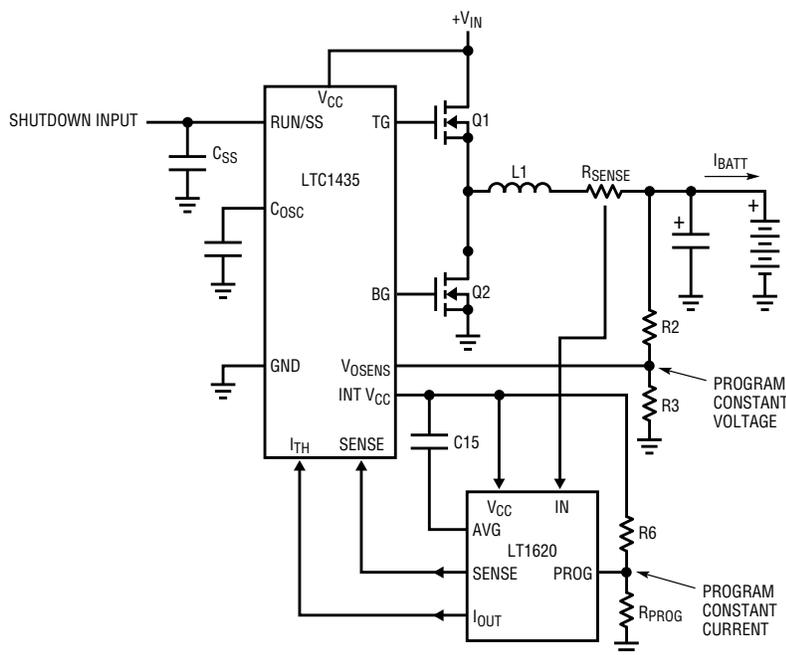
**Figure 3. Charger dropout voltage vs charge current**

tions. Used together, these two products overcome the voltage and current programming limitations previously mentioned, to produce a high current, high performance constant-voltage/constant-current battery charger for lithium-ion and other battery types.

### How They Work Together

To understand how the two parts work together, a brief review of the LTC1435 operation is necessary. See Figure 4. During each cycle of operation, the series MOSFET switch Q1 is turned on by the LTC1435 oscillator (Q2 is off). This causes a current to begin ramping up in inductor L1. When the current in L1 reaches a peak level determined by the voltage at the I<sub>TH</sub> pin, Q1 is turned off and the synchronous MOSFET Q2 is turned on, causing the current in L1 to ramp down to the level at which it started. Thus, a sawtooth of inductor ripple current is generated, with a peak level set by the voltage on the I<sub>TH</sub> pin. This inductor current is sensed via an external, low value sense resistor in series with the inductor and is used to drive the LTC1435 internal current sense amplifier for the current mode feedback signal. This current sense amplifier has a maximum common mode voltage limit of 10V, which limits the maximum output voltage to 10V.

Enter the LT1620. The LT1620 also contains a current sense amplifier, which has a common mode range that extends up to 28V. This amplifier is used to level shift the differential sense voltage, which is riding on the battery voltage, and reference it to the



**Figure 4. Simplified diagram of constant-voltage/constant-current charger**



## Selecting Battery Voltage Programming Resistors

The charging voltage of lithium-ion cells is either 4.1 or 4.2 volts per cell, depending on the battery chemistry. Contact the battery manufacturer for the recommended charge voltage. To program battery charging voltage (float voltage) use the following equation (for best accuracy and stability, use 0.1% resistors).

$$V_{BATT} = V_{REF} \left( 1 + \frac{R2}{R3} \right)$$

$$V_{REF} = 1.19V; \text{ USE APPROXIMATELY } 100k \Omega \text{ FOR } R3$$

$$R2 = R3 \left( \frac{V_{BATT}}{V_{REF}} - 1 \right)$$

## Selecting $R_{SENSE}$

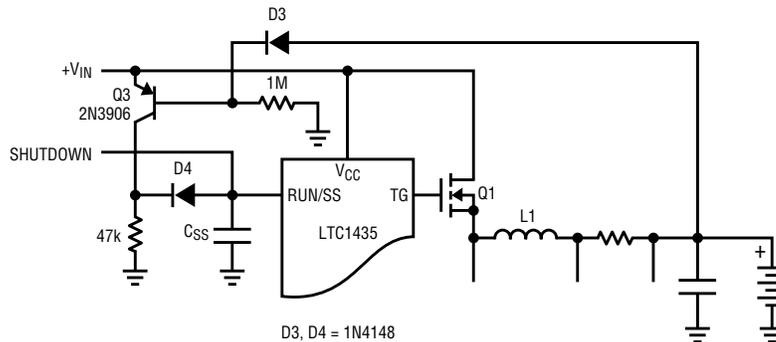
$R_{SENSE}$  is an external, low value resistor that is placed in the inductor current path to develop a signal representative of the inductor or charge current ( $I_{BATT}$ ). This signal is used as feedback to control the switching regulator constant-voltage and constant-current loops. To minimize overall dropout voltage and power dissipation in the sense resistor, a sense voltage of 80mV was chosen to represent maximum charging current. Use the following equation to select current sense resistor  $R_{SENSE}$ . The maximum battery charge current ( $MAX I_{BATT}$ ) must be known.

$$R_{SENSE} = \frac{0.08V}{MAX I_{BATT}}$$

## Selecting $I_{PROG}$

$I_{PROG}$  is a current from the PROG pin to ground that is used to program the maximum charging current.  $I_{PROG}$  can be derived from a resistor to ground, from the output of a DAC or by other methods. This program current is generated using resistors and the 5V  $V_{CC}$  available from the LTC1435.

Refer to the simplified diagram of the constant-current control loop shown in Figure 5. The DC voltage across  $C_{AVG}$  is proportional to the average charge current. This voltage



**Figure 6. Circuitry that shuts down the charger when input power is removed, minimizing reverse battery current drain**

drives one input of a transconductance ( $g_m$ ) amplifier. A program voltage (relative to the 5V  $V_{CC}$  line) proportional to the desired, or programmed charge current is applied to the other input of the transconductance amplifier. This voltage should be selected to be ten times the average voltage dropped across  $R_{SENSE}$  when the charger is in a constant-current mode.

If the voltage across  $C_{AVG}$  increases to a level equal to the voltage at the PROG pin, the transconductance amplifier begins pulling down on the  $I_{TH}$  pin of the LTC1435, thereby limiting the peak inductor current, and thus the average charge current.

The program voltage needed on the program pin can easily be generated by two resistors, as shown in Figure 5. A current ( $I_{PROG}$ ) is generated by these resistors and the 5V  $V_{CC}$  voltage. This  $I_{PROG}$  develops a voltage across  $R6$ , which is used to set the maximum constant charge current level. The circuit is designed for an approximate PROG voltage of 800mV (don't exceed the maximum spec of 1.25V), referenced to the LT1620  $V_{CC}$  pin. Because of the gain-of-10 amplifier, this corresponds to a typical voltage across  $R_{SENSE}$  of 80mV (with a maximum of 125mV).

The recommended range of resistor values for  $R6$  is approximately 2k $\Omega$  to 10k $\Omega$ . With 0.8V across  $R6$ , this will result in program currents ( $I_{PROG}$ ) between 400 $\mu$ A and 80 $\mu$ A.

The LT1620 was designed to reduce the charging current to zero under all conditions when the  $I_{PROG}$  is set to zero. To ensure that the charging

current will always go to zero, an offset was designed into the transconductance amplifier. In the equations for  $R6$  and  $R_{PROGRAM}$ , this offset is represented by using 840mV rather than 800mV.

Example:

$$\text{GIVEN: MAXIMUM } I_{BATT} = 4A \\ I_{PROG} = 200\mu A \text{ (FOR MAXIMUM } I_{BATT})$$

$$R_{SENSE} = \frac{0.08V}{MAX I_{BATT}} = \frac{0.08V}{4A} = 0.02\Omega$$

$$R6 = \frac{0.84V}{I_{PROG}} = \frac{0.84V}{200\mu A} = 4.2k\Omega$$

$$R_{PROG} = \frac{5V - 0.84V}{I_{PROG}} = \frac{5V - 0.84V}{200\mu A} = 20.8k\Omega$$

Once  $R1$  and  $R6$  are known, the following equations can be used to determine  $R_{PROG}$  and  $I_{PROG}$  for lower  $I_{BATT}$  currents:

$$R_{PROG} = \frac{R6 [5 - 10(I_{BATT})(R1)]}{0.04 + 10(I_{BATT})(R1)}$$

$$I_{PROG} = \frac{10(I_{BATT})(R1) + 0.04}{R6}$$

## PC Board Layout

As with any high frequency switching regulator, layout is important. Switching current paths and heat producing thermal paths should be identified and the printed circuit board designed using good layout practices.

Even with efficiency numbers in the mid 90s, under some charging conditions power losses can be as

*continued on page 36*

# LTC1069-X: a New Family of 8th Order Monolithic Filters in SO-8 Packages

by Nello Sevastopoulos and Philip Karantzalis

The LTC1069 switched capacitor filter technology offers economical solutions for a wide range of filter requirements. The filter response, the sampling rate and the power consumption can be easily reprogrammed by means of a single processing layer. The LTC1069 semicustom filter technology can integrate any single 8th order or dual 4th order classical filter approximation (Butterworth, Bessel, Chebyshev or elliptic) or any application specific filter response, in an 8-pin SO package. Three new devices illustrate this technology's versatility.

## LTC1069-1: Low Power Elliptic Filter Works from Single 3.3V to $\pm 5V$ Supplies

The LTC1069-1 has a frequency response that provides a flat passband in combination with steep attenuation in the vicinity of the cutoff frequency. The cutoff frequency of the filter is clock tuned with a clock-to-cutoff-frequency ratio of 100:1. The passband is "flat" up to 95% of the cutoff frequency; the typical ripple is  $\pm 0.1$ dB. Attenuations of 20dB at  $1.2 \times f_{CUTOFF}$  and 52dB at  $1.4 \times f_{CUTOFF}$  are obtained. Beyond these frequencies the transition band keeps rolling off instead of "bouncing back" the way textbook elliptics do. Figure 1 illustrates this "progressive" roll-off. The

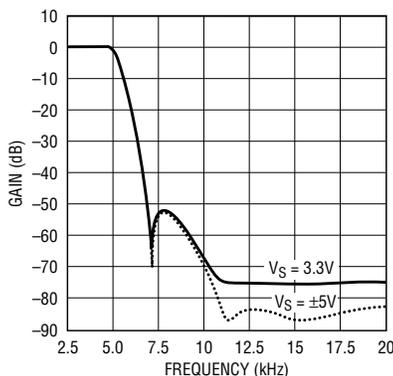


Figure 1. LTC1069-1 elliptic filter frequency response ( $f_{CUTOFF} = 5$ kHz,  $f_{CLK} = 500$ kHz)

attenuation floor reaches 82.5dB at  $2.3 \times f_{CUTOFF}$  with a  $\pm 5V$  supply and 75dB with a single 3.3V supply. The LTC1069-1 is designed for low power, single- or dual-supply, low frequency antialiasing filter applications. Figures 2 and 3 show typical connections for single 5V and  $\pm 5V$  supplies. The analog ground of the device is internally biased to one half the total power supply voltage, thus eliminating the need for additional external components and power waste. The low power consumption and speed obtainable from the part are shown in Table 1.

Despite the low power consumption of the device, extreme care was applied to maintain wide dynamic range. The best dynamic range is obtained with  $\pm 5V$  supplies. Figure 4 shows a  $S/(Noise+THD)$  ratio of better than 70dB for almost a decade of input signal range. The frequency of the input signal was set to 1kHz.

## LTC1069-7 Linear-Phase, Raised-Cosine Filter

The LTC1069-7 lowpass filter uses exactly the same technology as the LTC1069-1, yet it is designed to perform an entirely different task. First, a filter transfer function was synthesized to approximate a raised-cosine amplitude response with an alpha factor of one and linear phase in the passband (Figure 5). A simplified discussion of raised-cosine filters can be found in the boxed section on page

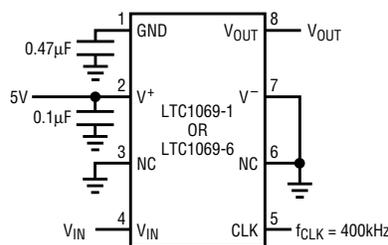


Figure 2. Single 5V supply 4kHz elliptic lowpass filter

Table 1. LTC1069-1 power consumption and speed

$V_S$	$I_{SUPPLY}$ (Typ)	$f_{CUTOFF}$ (Max)
3.3V	1.5mA	5kHz
5V	2.5mA	8kHz
$\pm 5V$	3.2mA	12kHz

28. Digital communication systems in need of pulse shaping and channel band limiting require the properties of raised-cosine filters. Note that the raised-cosine response is not related to the classical filter responses like Butterworth, Bessel or elliptic; its realization with classic RC active techniques requires many precision passive components and tuning adjustments. When compared to a conventional Bessel filter of the same order (for example, the LTC1064-3), the LTC1069-7 provides steeper roll-off at the vicinity of its cutoff frequency (see Figure 5). The impulse response of the LTC1069-7 is also fully symmetrical (see Figure 6) and is designed to shape an incoming pulse for optimum reception.

The LTC1069-7 trades power consumption and, to some degree, sampling rate, for speed. The maximum cutoff frequency is 200kHz, the sampling-rate to cutoff-frequency ratio is 50:1 and the clock-to-cutoff frequency ratio is 25:1. The

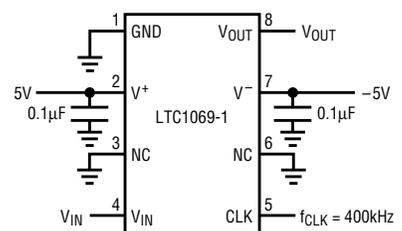


Figure 3.  $\pm 5V$  supply 4kHz elliptic lowpass filter

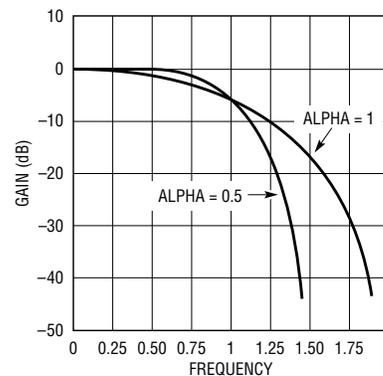
**Raised-Cosine Filters**

In digital communications, information is transmitted and received as sequences of signal units of very short duration. Each signal (referred to as a *symbol*) generates a transient response as it is processed through a communications link. The detection of valid symbols requires precise sampling every T seconds for a signaling rate of 1/T. During sampling, the decaying oscillations of a previous symbol can add errors in the detection process. When an incorrect decision is made about the symbol originally transmitted, intersymbol interference (ISI) is said to occur. In order to minimize ISI with as small a transmission bandwidth as possible, raised-cosine

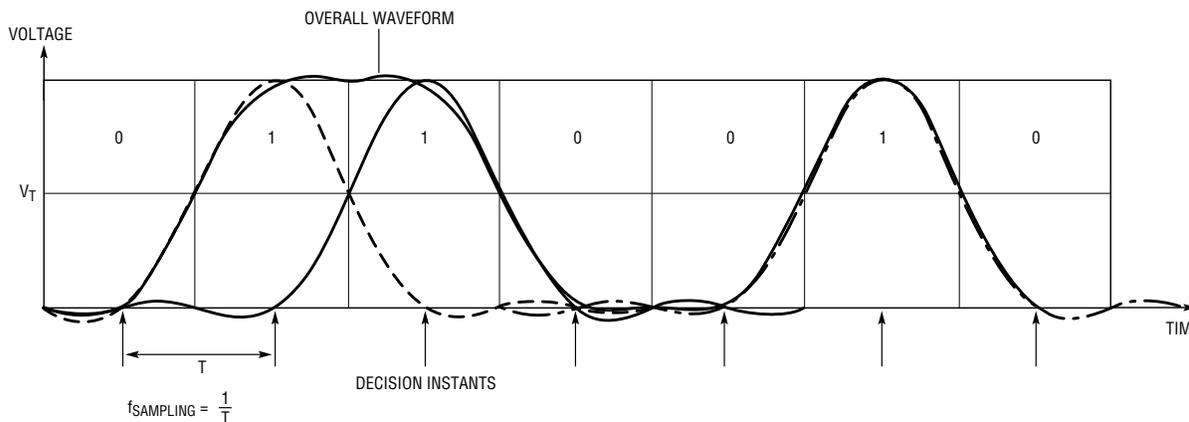
filters are used in data transmission to shape signals. When a pulsed signal is transmitted through a raised-cosine filter, it will be received with minimum ISI, assuming the channel is properly designed. Figure A illustrates how two consecutive pulses can be shaped and properly detected with minimum ISI. Raised-cosine filters are defined by the type of roll-off in the stop band (often referred to as the “alpha” of the filter—Figure B).

One way to create a communications channel with a flat frequency response and low distortion is to match the receiver filter to the transmitter filter; if both filters are designed with a root-raised-cosine response, the overall channel is raised-cosine.

For root-raised-cosine designs using the LTC1069 family of filters, please contact LTC Marketing. 

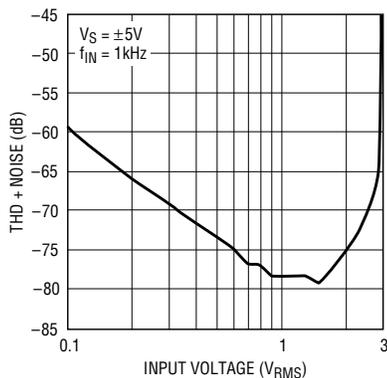


**Figure B. Gain versus frequency for raised-cosine filters**



**Figure A. A sequence of pulses with minimum intersymbol interference at the output of a raised-cosine filter**

LTC1069-7 is pin compatible with the LTC1069-1. Table 2 illustrates the maximum cutoff frequency of the device for different power supplies.



**Figure 4. LTC1069-1 THD + noise versus input amplitude with ±5V supply**

**LTC1069-6: Single-Supply, Very Low Power, Progressive Elliptic Lowpass Filter**

The LTC1069-6 is designed for minimal power consumption and for single 3V and 5V supply operation. The amazingly low supply current of 1mA (3V supply) and 1.2mA (5V supply) includes the current spent to internally bias the AGND pin for optimum voltage swing when operating the part on a single supply. To save power, the clock-to-cutoff frequency ratio is lowered to 50:1 but the sampling rate is still 100:1. With a 50:1 clock-to-cutoff frequency ratio and for clocks equal to or less than 1MHz, cutoff frequencies within the audio band can be obtained.

The amplitude response of the filter is also progressive elliptic, as illustrated in Figure 7, where the clock is set to 600kHz for a 12kHz cutoff frequency. Figure 7 also shows the response of the LTC1069-1 with a clock of 1.2MHz and a 12kHz cutoff frequency. When compared to the LTC1069-1, the LTC1069-6 has a sharper roll-off in the vicinity of its

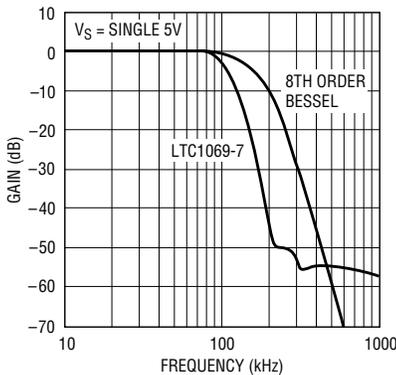
**Table 2. LTC1069-7 maximum cutoff frequencies**

V <sub>S</sub>	I <sub>SUPPLY</sub>	f <sub>CUTOFF</sub>
±5V	18mA	200kHz
5V	12mA	140kHz

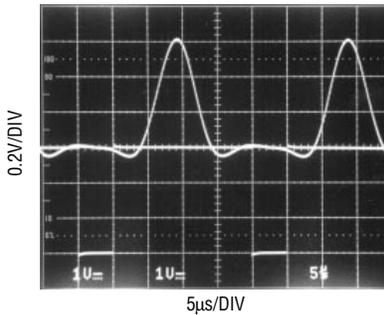
**Table 3. LTC1069-6 maximum cutoff frequencies and resulting power consumption**

$V_s$	$I_{SUPPLY}$ (Typ)	$f_{CUTOFF}$ (Max)	$f_{CLOCK}$ (Max)
3V	1.0mA	14kHz	700kHz
5V	1.2mA	20Hz	1MHz

cutoff frequency; the key feature is 42dB–50dB attenuation for frequencies between  $1.27 \times f_{CUTOFF}$  and  $1.31 \times f_{CUTOFF}$ . Conversely, the LTC1069-1 has better stop band attenuation and a flatter passband and is therefore more selective right at the cutoff frequency.

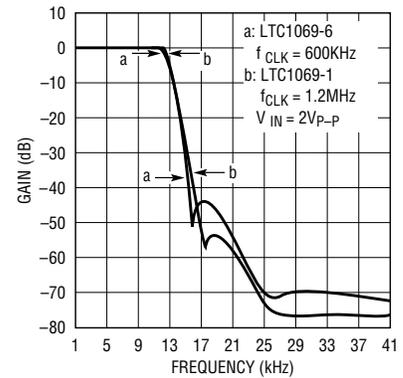


**Figure 5. LTC1069-7 amplitude response compared to 8th order Bessel**

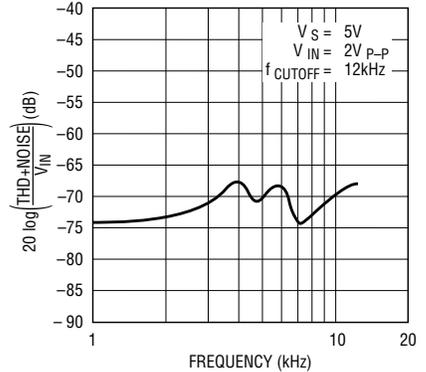


**Figure 6. The pulse response of the LTC1069-7 is fully symmetrical.**

Despite the LTC1069-6's very low power consumption, its noise and distortion performance are quite impressive. The single supply connection of Figure 2 was used to operate the LTC1069-6 with a single 5V supply, 600kHz clock and 12kHz cutoff frequency. A  $2V_{P-P}$  signal was swept from 1kHz to 12kHz. The output of the filter was buffered to drive the cable and the input stage of the signal analyzer. With  $2V_{P-P}$  input, the signal-to-noise ratio measured at 1kHz was 74dB; the -67dB worst-case harmonic distortion occurred for input frequencies of 4kHz, that is, at 1/3 of the filter cutoff frequency. Figure 8 illustrates the above data. Table 3 shows the maximum cutoff frequency the device can reach and the corresponding power consumption. The



**Figure 7. Amplitude response comparison: LTC1069-6 versus LTC1069-1**



**Figure 8. LTC1069-6 signal to (noise + THD) ratio versus frequency**

LTC1069-6 can reach higher cutoff frequencies than the LTC1069-1 for less power. This is mainly due to the lower clock-to-cutoff frequency ratio. 

## The Linear Technology World Wide Web Site is Open

by Kevin R. Hoskins

Linear Technology Corporation's customers can now quickly and conveniently find and retrieve the latest technical information covering the company's products on LTC's new internet web site. Located at [www.linear.com](http://www.linear.com) or [www.linear-tech.com](http://www.linear-tech.com), this site allows anyone with internet access and a web browser to search through all of LTC's technical publications, including data sheets, application notes, *Linear Technology* magazine issues and other LTC publications, to find information on LTC parts and applications circuits. Other areas within the site include help, news and information about Linear

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Other web sites usually require the visitor to download large document files to see if they contain the desired information. This is cumbersome and inconvenient. To save you time and ensure that you receive the correct information the first time, the first page of each data sheet, application note, and *LT* magazine is recreated in a fast, download-friendly format. This allows you to determine whether the document is what you need, before downloading the entire file.

The site is searchable. Among the possible search criteria are part numbers, function, topics and applications. The search is performed on a

user-defined combination of data sheets, application notes, design notes and *Linear Technology* magazine articles. Any data sheet, application note, design note or magazine article can be downloaded or Faxed back. (Files are downloaded in Adobe Acrobat PDF format; you will need a copy of Acrobat Reader to view or print them. The site includes a link from which you can download this program.)

The site also makes it possible to order the LinearView CD-ROM, databooks, application handbooks, and other paper-based publications and make sample requests. Design tools, such as SwitcherCAD, MicroPowerSwitcherCAD and FilterCAD, can be downloaded. 

# Micropower ADC and DAC in SO-8 Give PC 12-Bit Analog Interface

by Kevin R. Hoskins

Needing to add two channels of simple, inexpensive, low powered, compact analog input/output to a PC computer, I chose the LTC1298 ADC and LTC1446 DAC. The LTC1298 and the LTC1446 are the first SO-8 packaged 2-channel devices of their kind. The LTC1298 draws just 340µA. A built-in auto shutdown feature further reduces power dissipation at reduced sampling rates (to 30µA at 1ksps). Operating on a 5V supply, the LTC1446 draws just 1mA (typ). Although the application shown is for PC data acquisition, these two converters provide the smallest, lowest

power solutions for many other analog I/O applications.

The circuit shown in Figure 1 connects to a PC's serial interface using four interface lines: DTR, RTS, CTS and TX. DTR is used to transmit the serial clock signal, RTS is used to transfer data to the DAC and ADC, CTS is used to receive conversion results from the LTC1298 and the signal on TX selects either the LTC1446 or the LTC1298 to receive input data. The LTC1298's and LTC1446's low power dissipation allows the circuit to be powered from the serial port. The TX and RTS lines

charge capacitor C4 through diodes D3 and D4. An LT1021-5 regulates the voltage to 5V. Returning the TX and RTS lines to a logic high after sending data to the DAC or completion of an ADC conversion provides constant power to the LT1021-5.

Using a 486-33 PC, the throughput was 3.3ksps for the LTC1298 and 2.2ksps for the LTC1446. Your mileage may vary.

Listing 1 is C code that prompts the user to either read a conversion result from the ADC's CH0 or write a data word to both DAC channels. The code is available on disk from LTC. ◀

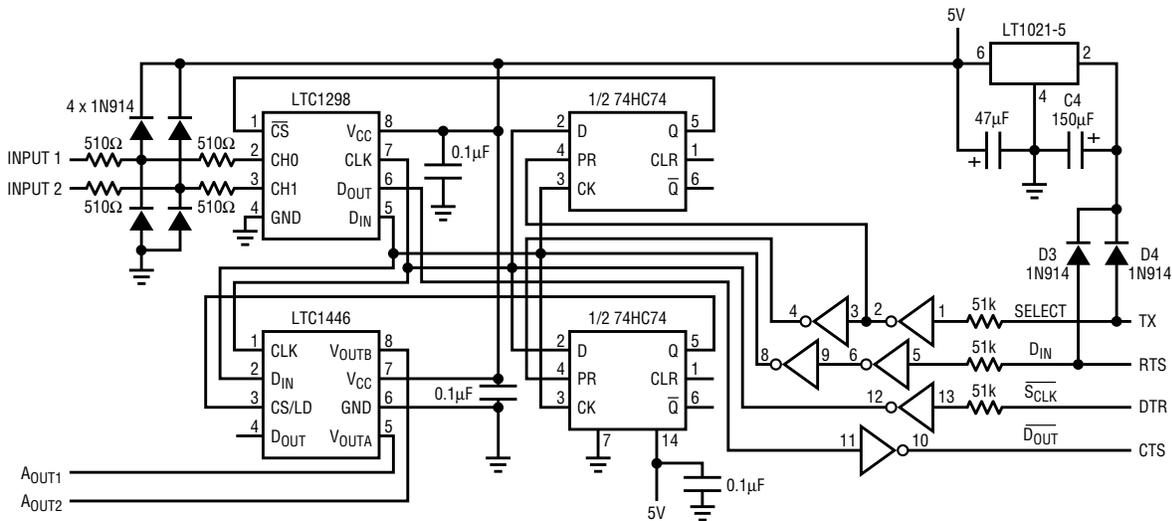


Figure 1. Communicating over the serial port, the LTC1298 and LTC1446 in SO-8 create a simple, low power, 2-channel analog interface for PCs.

Listing 1. Configure analog interface with this C code

```
#define port 0x3FC          /* Control register, RS232 */
#define inprt 0x3FE       /* Status reg. RS232 */
#define LCR 0x3FB        /* Line Control Register */
#define high 1
#define low 0
#define Clock 0x01       /* pin 4, DTR */
#define Din 0x02         /* pin 7, RTS */
#define Dout 0x10        /* pin 8, CTS input */
#include<stdio.h>
#include<dos.h>
```

```
#include<conio.h>
/* Function module sets bit to high or low */
void set_control(int Port, char bitnum, int flag)
{
    char temp;
    temp = inportb(Port);
    if (flag==high)
        temp |= bitnum;          /* set output bit to high */
        else
            temp &= ~bitnum;     /* set output bit to low */
    outportb(Port, temp);
}

/* This function brings CS high or low (consult the schematic) */
void CS_Control(direction)
{
    if (direction)
        {
            set_control(port, Clock, low);          /* set clock high for Din to be read */
            set_control(port, Din, low);           /* set Din low */
            set_control(port, Din, low);           /* set Din high to make CS goes high */
        }
        else {
            outportb(port, 0x01);                  /* set Din & clock low */
            Delay(10);
            outportb(port, 0x03);                  /* Din goes high to make CS go low */
        }
}

/* This function outputs a 24-bit (2x12) digital code to LTC1446L */
void Din_(long code, int clock)
{
    int x;
    for(x = 0; x<clock; ++x)
    {
        code <<= 1;                               /* align the Din bit */
        if (code & 0x1000000)
            {
                set_control(port, Clock, high);    /* set Clock low */
                set_control(port, Din, high);      /* set Din bit high */
            }
        else {
            set_control(port, Clock, high);        /* set Clock low */
            set_control(port, Din, low);           /* set Din low */
        }
        set_control(port, Clock, low);            /* set Clock high for DAC to latch */
    }
}

/* Read bit from ADC to PC */
Dout_()
{
    int temp, x, volt = 0;
```

```

for(x = 0; x<13; ++x)
{
    set_control(port,Clock,high);
    set_control(port,Clock,low);
    temp = inportb(inprt);           /* read status reg. */
    volt <<= 1;                       /* shift left one bit for serial transmission */
    if(temp & Dout)
    volt += 1;                       /* add 1 if input bit is high */
}
return(volt & 0xfff);
}
/* menu for the mode selection */
char menu()
{
printf("Please select one of the following:\na: ADC\nd: DAC\nq: quit\n\n");
return (getchar());
}
void main()
{
long code;
char mode_select;
int temp,volt=0;
/* Chip select for DAC & ADC is controlled by RS232 pin 3 TX line. When LCR's bit 6 is set, the
   DAC is selected and the reverse is true for the ADC. */
outportb(LCR,0x0);           /* initialize DAC */
outportb(LCR,0x64);         /* initialize ADC */
while((mode_select = menu()) != 'q')
{
    switch(mode_select)
    {
        case 'a':
            {
                outportb(LCR,0x0);           /* selecting ADC */
                CS_Control(low);           /* enabling the ADC CS */
                Din_(0x680000, 0x5);       /* channel selection */
                volt = Dout_();
                outportb(LCR,0x64);         /* bring CS high */
                set_control(port,Din,high); /* bring Din signal high */
                printf("\ncode: %d\n",volt);
            }
            break;
        case 'd':
            {
                printf("Enter DAC input code (0 - 4095):\n");
                scanf("%d", &temp);
                code = temp;
                code += (long)temp << 12; /* converting 12-bit to 24-bit word */
                outportb(LCR,0x64);         /* selecting DAC */
                CS_Control(low);           /* CS enable */
            }
    }
}
}

```

*continued on page 37*

# High Efficiency, Low Power, 3-Output DC/DC Converter

by John Seago

The recent proliferation of battery powered products has created a lot of interest in low power, high efficiency DC/DC converter designs. These products are small, lightweight and portable, so space for bulky batteries is limited. Often, operating time between charges is a major selling feature, making the efficient use of battery power very important. Since many products cannot function with a single regulated voltage, multiple-output DC/DC converters are required.

Although developed for somewhat higher power levels, the single output LTC1435 can be used in applications requiring a very efficient, very small, low power, multiple-output DC/DC converter (see Figure 1). This is accomplished through the use of an overwound buck inductor. With additional windings, the inductor can provide additional outputs, requiring only a diode and filter capacitor for

each output. As with the less efficient flyback topology, the additional outputs are not as well regulated as the primary output, but the regulation is suitable for most applications.

The circuit of Figure 1 provides 3.3V at 0.5A, 5V at 0.1A and -5V at 0.05A, and has greater than 93% efficiency for test loads between 1.25W and 2.4W with a 6V input. Load and line regulation of the positive outputs are quite good. Each output voltage was measured with all output currents varied independently between

20% and 100% of their full load range, while the input voltage was varied from 6V to 20V. Table 1 shows the worst-case output voltages measured.

The buck regulator with an overwound inductor is a good solution for those applications that do not have large load current or line voltage variations. The smaller the load and line variations, the smaller the voltage variations on the overwound outputs. As a general rule, output voltage regulation is suitable for most applications if the switch duty cycle is kept between 15% and 50% and minimum load current is kept above 20% of maximum. Since load variation and line variation have an additive effect on output voltage, applications with relatively constant load current requirements can have a larger input voltage range and vice versa. For zero output current requirements, a small preload resistor can be used. 

Table 1. Worst-case output voltages

Output	Minimum	Maximum
3.3V	3.307V	3.315V
5V	5.03V	5.24V
-5V	-4.98V	-5.51V

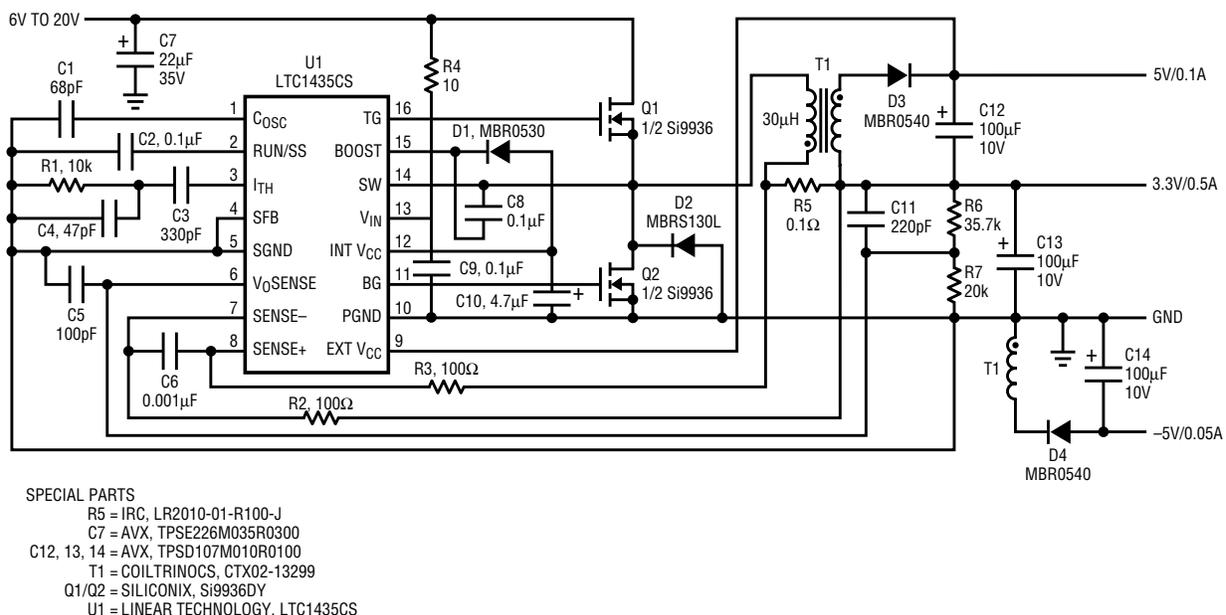


Figure 1. High efficiency, 3-output DC/DC converter

# Synchronizing LTC1430s for Reduced Ripple

by Craig Varga

The recent move to split-plane microprocessors by several CPU makers has led to the inclusion of multiple switching regulators on many motherboard designs. These regulators typically provide 3.3V for system logic and a separate supply for the processor core. Current requirements of 5A–10A or more per supply are not unusual. The LTC1430 synchronous buck regulator is commonly used to provide these tightly regulated supplies. By nature, the input current waveform in the buck topology is discontinuous, resulting in large input ripple current. By synchronizing a pair of supplies out of phase, it is possible to achieve a degree of ripple current cancellation. This results in less stress on the input capacitors (the number of input capacitors could

be reduced) and lower EMI. The ripple is easier to filter since the frequency is effectively doubled and the peak-to-peak current is reduced.

It is extremely simple to synchronize a pair of LTC1430s in an appropriate phase relationship. Simply connect a resistor divider from the low gate drive of a “master” regulator to the sync pin of a “slave” regulator. The resistors should divide the gate-drive voltage down to something slightly less than the  $V_{CC}$  supply of the slave regulator, typically from 12V down to approximately 4.5V. Total divider resistance of 20k to 30k is adequate. Also, the slave regulator must be set up to free run slower than the master regulator. If, for example, the master is configured to run at approximately 300kHz (a 130k resis-

tor from FSET to ground) the slave can be left to run at its natural frequency of 200kHz. The slave frequency will be forced up to that of the master.

The sync function on the LTC1430 works as follows: when the shutdown pin is pulled low, the high-side switch turns off; normal duty factor control determines when the high-side switch will turn back on. As long as the shutdown pin is held low for less than approximately 40 $\mu$ s, the chip will not shut down.

The simplified schematic (Figure 1) shows the synchronization circuitry. For a detailed description of LTC1430-based regulator designs, see the LTC1430 data sheet. The scope photo (Figure 2) shows the voltage at the common connection of the two FETs of each regulator.  $\blacktriangleleft$

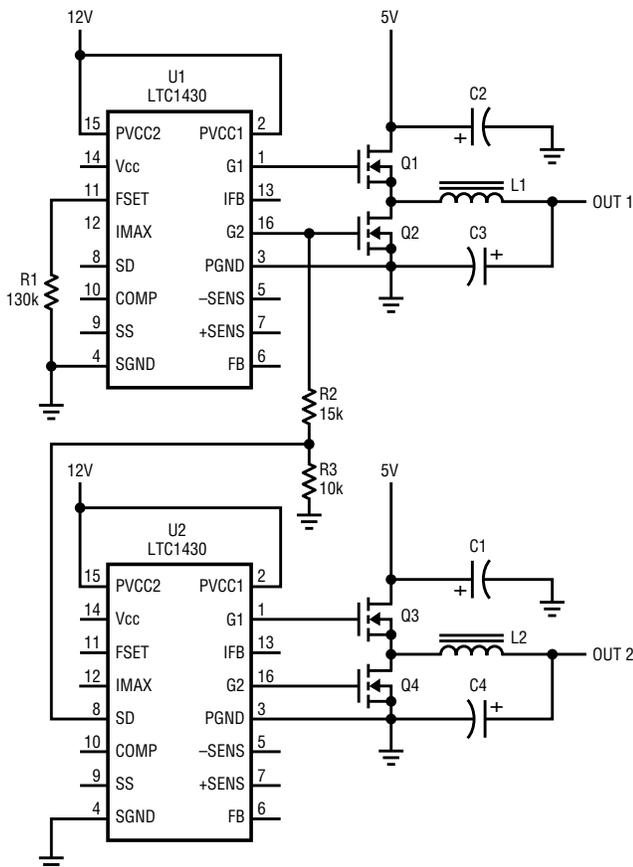


Figure 1. Simplified schematic diagram of synchronization circuitry

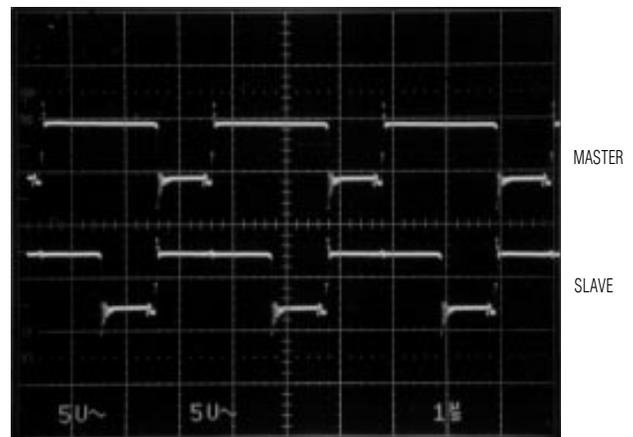


Figure 2. Phase relations looking at the switching nodes of both regulators

Authors can be contacted at (408) 432-1900

# New Voltage References Are Smaller and More Precise

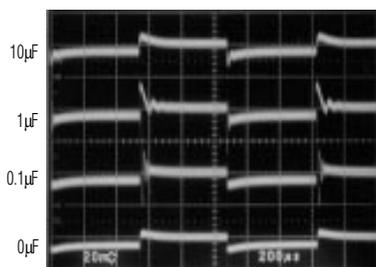
by John Wright

## Introduction

Two new series voltage references bridge the gap between small package size and high precision. Advances in design, process and packaging have made the introduction of these new voltage references possible. The low power LT1460 is designed for minimum space and is available in all popular voltages, including 2.5V, 5V and 10V. By contrast, the LT1236 is designed for use in 12-bit systems and combines 0.05% accuracy, low noise and low drift. These new series references provide supply current and power dissipation advantages over older shunt references that must idle the entire load current to operate. Furthermore, series references are seeing more duty as mini-regulators in data conversion and low power electronics.

## The Small Fry

The LT1460 is a tiny, low power, bandgap series reference with big performance. It uses curvature compensation to obtain low drift, and trimmed precision thin-film resistors to achieve high output accuracy. Its performance does not degrade in either the SO-8 or MSOP packages. Surface mount packages are very space efficient, but the use of a large output capacitor to stabilize the reference defeats the purpose of the small package. The LT1460 is stable with load capacitors, or with no capacitor at all (see Figure 1). This can be helpful when fast settling is a goal,



**Figure 1.** LT1460 transient response for  $I_{OUT} = 10\text{mA}$ , and  $C_L = 0, 0.1\mu\text{F}, 1\mu\text{F}, 10\mu\text{F}$

since load capacitors that change their voltages must recover before the reference value is accurate.

The LT1460 uses so little PC board space that there is a temptation to

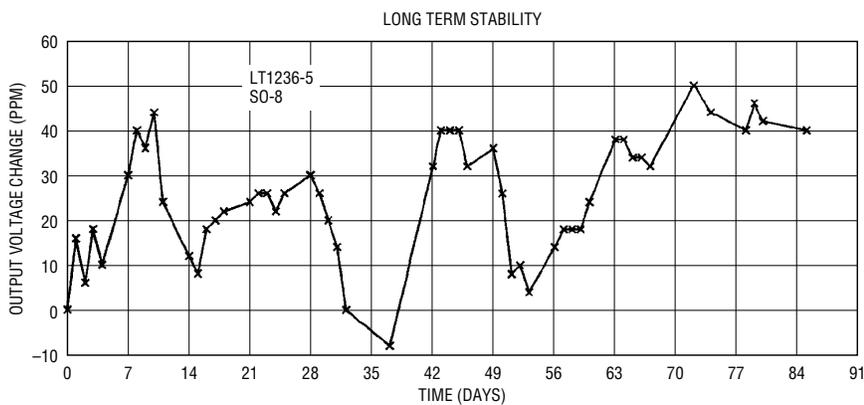
use the device as a “local” regulator. This is exactly what the LT1460 was designed to do: deliver substantial load current while maintaining reference-like features. At  $I_{OUT} = 30\text{mA}$ ,

**Table 1. Key specifications of the LT1460 voltage reference, SO-8 package**

Parameter	Conditions	Value
Output Voltage Tolerance LT1460A LT1460B		0.075% 0.10%
Temperature Coefficient LT1460A LT1460B	$0^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$	10ppm/ $^\circ\text{C}$ 20ppm/ $^\circ\text{C}$
Line Regulation	4.5V to 30V	10ppm/V
Load Regulation Sourcing	$I_{OUT} = 30\text{mA}$	70ppm/mA
Dropout Voltage	$I_{OUT} = 0\text{mA}$	0.7V
Supply Current	$I_{OUT} = 0\text{mA}$	100 $\mu\text{A}$
Reverse Leakage	$I_{OUT} = 0\text{mA}, V_{IN} = -20\text{V}$	20 $\mu\text{A}$
Output Noise Voltage	$0.1\text{Hz} \leq f \leq 10\text{Hz}$	25 $\mu\text{V}_{\text{p-p}}$
Output Voltages		2.5V, 5.0V, 10V

**Table 2. Key specifications of the LT1236-10 voltage reference, SO-8 package**

Parameter	Conditions	Value
Output Voltage Tolerance LT1236A LT1236B LT1236C		0.05% 0.1% 0.15%
Temperature Coefficient LT1236A LT1236B LT1236C	$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$	5ppm/ $^\circ\text{C}$ 10ppm/ $^\circ\text{C}$ 15ppm/ $^\circ\text{C}$
Line Regulation	$11.5\text{V} \leq V_{IN} \leq 40\text{V}$	4ppm/V
Load Regulation Sourcing	$0\text{mA} \leq I_{OUT} \leq 10\text{mA}$	25ppm/mA
Output Noise	$10\text{Hz} \leq f \leq 1\text{kHz}$	6.0 $\mu\text{V}_{\text{RMS}}$
Supply Current	$I_{OUT} = 0\text{mA}$	1.7mA



**Figure 2. LT1236 long-term stability**

the load regulation is 70ppm/mA, yet the LT1460 can withstand a short to ground without being destroyed.

Additionally, if the power supplies are reversed, the reverse battery protection keeps the reference from conducting current and being damaged (see Table 1).

**Higher Performance, Industrial Temperature Range and Surface Mount**

The LT1236 is a precision reference that combines ultralow drift and noise with excellent long-term stability and high output accuracy. To address small package requirements, the new reference is available in the SO-8

package and guarantees critical reference parameters from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  (see Table 2). The LT1236 output will both source and sink 10mA, is almost totally immune to input voltage variations and, like the LT1460, is stable with any load capacitor. Two output voltages are available: 5V and 10V. The 10V version can be used as a shunt regulator (2-terminal Zener) with the same precision characteristics as the 3-terminal connection. Special care has been taken to minimize thermal regulation effects and temperature-induced hysteresis. The LT1236 combines superior accuracy and temperature-coefficient specifications, without using high power, on-chip heaters. The LT1236 references are based on a buried Zener diode structure that eliminates noise and stability problems that plague surface-breakdown devices. **LT**

*LT1620, continued from page 26*

high as 4 watts. These losses are primarily in the two MOSFETs, the inductor and the current sensing resistor. Since these are surface mount components, the major thermal paths are through the pc board copper to the surrounding air. Maximizing copper area around the heat producing components, increasing board area and using double-sided board with feedthrough vias all contribute to heat dissipation. Remember, the pc board is the heat sink.

One exception to the maximum copper area rule is the switch node consisting of Q1's source, Q2's drain and the left side of L1. This node switches between ground and  $V_{IN}$  at a 200kHz rate. To minimize radiation from this node, it should be short and direct. Other copper traces related to input and output capacitors and MOSFET connections should also be as short as practical. See the LTC1435 data sheet for information on good layout practices and additional applications information.

**Loads For Testing**

When testing the charger, several different types of loads can be used. If

the battery to be charged is available, use it for the load. Alternatively, a battery can be simulated by adjusting a power supply to the nominal battery voltage, preloading it with as many amps as the charger is capable of delivering, (using power resistors) and then connecting it to the charger output. A resistor can also be used for a load, but the charger may require additional output capacitance to prevent oscillations. This added capacitance is not needed when a battery is connected to the charger output.

**Noncharger Applications**

The LTC1435 and LT1620 can also be used for an adjustable current limit, high efficiency, low dropout power supply in situations where higher output voltages (greater than the 10V maximum limit of the LTC1435 by itself) are needed.

When used for nonbattery applications, more low ESR capacitance is needed on the output and the compensation component values (R5, C13, and C14) may require changes. Pulse loading the output and checking the transient response is a simple means of checking loop stability.

**Other Versions of the LT1620**

The 16-pin version of the LT1620 includes an additional, gain-of-20 amplifier and a comparator with an open-collector output. This output can be used for charge termination in a Li-Ion battery charger or as a signal to switch from a charge voltage to a float voltage in a lead-acid battery charger system.

Lithium-ion and lead-acid batteries are normally charged with a current limited, constant-voltage source. As the battery charges, the internal battery voltage rises and the charging current begins to taper off. When the charging current drops to 1/20 of the maximum programmed charging current, the comparator pulls low. Also available in a 16-pin DIP is a LT1621. This part contains two independent current control loops for dual-loop control. The second control loop can be used for input current limiting from the power source.

Refer to the LTC1435 and LT1620 data sheets for additional information. **LT**

PC Analog Interface, continued from page 32

```

        Din_(code,24);          /* loading digital data to DAC */
        outportb(LCR,0x0);      /* bring CS high */
        outportb(LCR,0x64);    /* disabling ADC */
        set_control(port,Din,high); /* bring Din signal high */
    }
    break;
}
}
}
    
```



Rail-to-Rail, continued from page 19

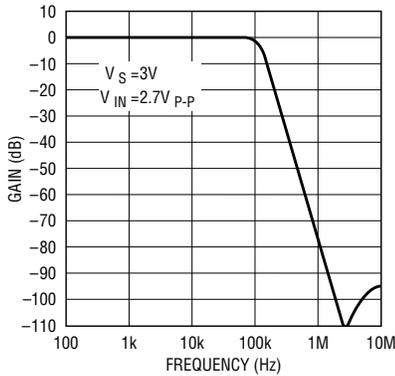


Figure 5. Filter frequency response

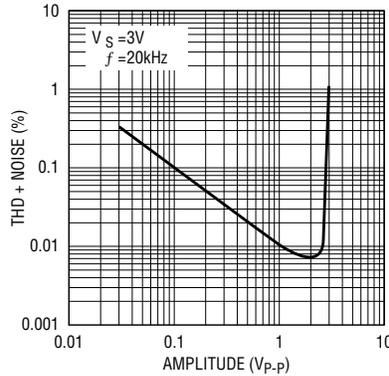


Figure 6. Filter distortion vs amplitude

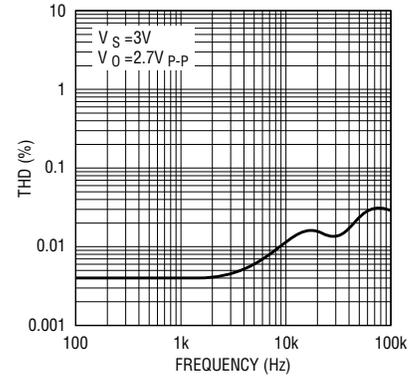


Figure 7. Filter distortion vs frequency

### 100kHz 4th Order Butterworth Filter for 3V Operation

The filter shown in Figure 4 uses the low voltage operation and wide bandwidth of the LT1498. Operating in the inverting mode for lowest distortion, the output swings rail-to-rail. The graphs in Figures 5–7 display the measured lowpass and distortion characteristics with a 3V power supply. As seen from the graphs, the distortion with a 2.7V<sub>P-P</sub> output is under 0.03% for frequencies up to the cutoff frequency of 100kHz. The stop band attenuation of the filter is greater than 90dB at 10MHz.

### Multiplexer

A buffered MUX with good offset characteristics can be constructed using the shutdown feature of the LT1218. In shutdown, the output of the LT1218 assumes a high impedance, so the outputs of two devices can be tied together (wired OR, as they say in the digital world). As shown in Figure 8,

the shutdown pins of each LT1218 are driven by a 74HC04 buffer. The LT1218 is active with the shutdown pin high. The photo in Figure 9 shows the switching characteristics with a 1kHz sine wave applied to one input and the other input tied to ground. As shown, each amplifier is connected for unity gain, but either amplifier or both could be configured for gain.

### Conclusion

The latest members of LTC's family of rail-to-rail amplifiers expand the versatility of rail-to-rail operation to micropower and high speed applications. The devices maintain precision V<sub>OS</sub> specifications over the entire rail-to-rail input range and have open loop gains of one million or more. These characteristics, combined with low voltage operation, makes for truly versatile amplifiers. 

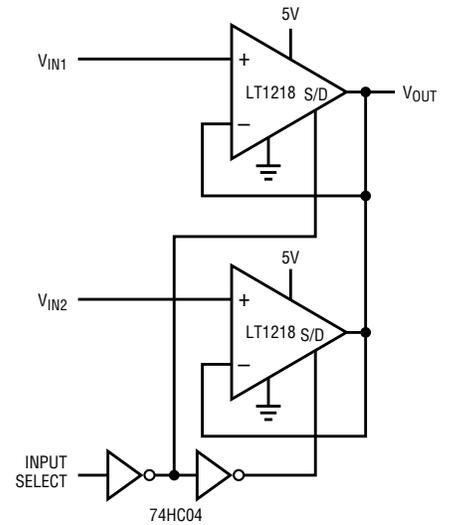


Figure 8. MUX amplifier



Figure 9. MUX amplifier waveforms

# New Device Cameos

## LTC1473 PowerPath Switch

The LTC1473 is a power management IC designed to drive and protect two sets of back-to-back N-channel MOSFET switches in battery-operated equipment such as notebook computers. The LTC1473 has a wide supply range (5V to 30V) to work with most available battery packs and DC adapters. Within this supply range, the supply current is a mere 100 $\mu$ A. When  $V^+$  drops below 3.2V, the LTC1473 shuts down and draws just 5 $\mu$ A of supply current.

An internal boost regulator provides the voltage to fully enhance the logic level N-channel MOSFET switches. N-channel MOSFETs are ideal for battery operated equipment because of their extremely low  $R_{DS(ON)}$  and small package size. Connected back-to-back (actually, source to source), two N-channel MOSFETs in a single package block current in both directions when they are off. A unique start-up mode allows the system to start regardless of which of the two sets of MOSFET switches receives power first.

The LTC1473 uses a current sense loop to limit current flow through the batteries and system supply capacitor during switchover transitions or during a fault condition. When an N-channel MOSFET switch enters the current limit condition, a fault timer will start timing. If this condition exceeds a user-programmable delay time, the MOSFET switch latches off. Deselecting the MOSFET switch resets the latch.

The LTC1473 is available in a 16-pin narrow SSOP package.

## LT2078/LT2079 and LT2178/LT2179 Single Supply, Micropower, Precision Amplifiers in Surface Mount Packages

With their outstanding DC precision and low supply current (only 55 $\mu$ A and 21 $\mu$ A per op amp, respectively), the LT1078/LT1079 and LT1178/LT1179 have become true industry standards. However, these devices have much better offset voltage and

offset voltage drift specifications in the dual inline package (DIP) than in the small surface mount package (SO). This is because the plastic surface mount packages, in cooling, exert stress on the top and sides of the die, causing changes in the offset voltage.

In response to this problem, LTC has created the new LT2078/LT2079 and LT2178/LT2179 single supply, surface mount op amps. These devices use a new, thin (approximately 50 microns), jelly-like coating, applied via a new dispensing system, to reduce stress on the top of the die. The result is that these parts have significantly superior  $V_{OS}$  and  $V_{OS}$  drift specs than their predecessors. The circuit design and process used for the LT2078/LT2079 and LT2178/LT2179 is the same as that for the LT1078/LT1079 and LT1178/LT1179, resulting in identical AC performance.

These new parts are available in 8- and 14-lead SO packages, for operation over the commercial, industrial and extended temperature ranges. **LT**

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**For further information on any of the devices mentioned in this issue of *Linear Technology*, use the reader service card or call the LTC literature service number:**

**1-800-4-LINEAR**

**Ask for the pertinent data sheets and Application Notes.**

## DESIGN TOOLS

## Applications on Disk

**Noise Disk** — This IBM-PC (or compatible) program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise and calculate noise using specs for any op amp. Available at no charge.

**SPICE Macromodel Disk** — This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models and a demonstration copy of PSPICE™ by MicroSim. Available at no charge.

**SwitcherCAD** — SwitcherCAD is a powerful PC software tool that aids in the design and optimization of switching regulators. The program can cut days off the design cycle by selecting topologies, calculating operating points and specifying component values and manufacturer's part numbers. 144 page manual included. \$20.00

SwitcherCAD supports the following parts: LT1070 series: LT1070, LT1071, LT1072, LT1074 and LT1076. LT1082. LT1170 series: LT1170, LT1171, LT1172 and LT1176. It also supports: LT1268, LT1269 and LT1507. LT1270 series: LT1270 and LT1271. LT1371 series: LT1371, LT1372, LT1373, LT1375, LT1376 and LT1377.

**Micropower SwitcherCAD** — MicropowerSCAD is a powerful tool for designing DC/DC converters based on Linear Technology's micropower switching regulator ICs. Given basic design parameters, MicropowerSCAD selects a circuit topology and offers you a selection of appropriate Linear Technology switching regulator ICs. MicropowerSCAD also performs circuit simulations to select the other components which surround the DC/DC converter. In the case of a battery supply, MicropowerSCAD can perform a battery life simulation. 44 page manual included. \$20.00

MicropowerSCAD supports the following LTC micropower DC/DC converters: LT1073, LT1107, LT1108, LT1109, LT1109A, LT1110, LT1111, LT1173, LTC1174, LT1300, LT1301 and LT1303.

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**1990 Linear Applications Handbook, Volume I** — 928 pages full of application ideas covered in depth by 40 Application Notes and 33 Design Notes. This catalog covers a broad range of "real world" linear circuitry. In addition to detailed, systems-oriented circuits, this handbook contains broad tutorial content together with liberal use of schematics and scope photography. A special feature in this edition includes a 22-page section on SPICE macromodels. \$20.00

**1993 Linear Applications Handbook, Volume II** — Continues the stream of "real world" linear circuitry initiated by the 1990 Handbook. Similar in scope to the 1990 edition, the new book covers Application Notes 40 through 54 and Design Notes 33 through 69. Additionally, references and articles from non-LTC publications that we have found useful are also included. \$20.00

**Interface Product Handbook** — This 424 page handbook features LTC's complete line of line driver and receiver products for RS232, RS485, RS423, RS422, V.35 and AppleTalk® applications. Linear's particular expertise in this area involves low power consumption, high numbers of drivers and receivers in one package, mixed RS232 and RS485 devices, 10kV ESD protection of RS232 devices and surface mount packages. Available at no charge

**Power Solutions Brochure** — This 80 page collection of circuits contains real-life solutions for common power supply design problems. There are over 79 circuits, including descriptions, graphs and performance specifications. Topics covered include battery chargers, PCMCIA power management, microprocessor power supplies, portable equipment power supplies, micropower DC/DC, step-up and step-down switching

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