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New LT1300 and LT1301 Micropower DC-to-DC Converters

by Steve Pietkiewicz

Introduction

The new LT1300 and LT1301 micropower DC-to-DC converters provide improvements in both electrical and physical efficiency, two key areas of battery-based power-supply design. Housed in 8-lead DIP or SOIC packages, the devices feature a 1A on-chip switch with a V_{CESAT} of just 170mV. The internal oscillator frequency is set at 155kHz, allowing the use of tiny, 5mm diameter surface mount inductors along with standard D-case size tantalum capacitors. A complete 2-cell to 12V, 5V, or 3.3V converter can fit in less than 0.4 square inches of PC board area.

The devices use Burst Mode™ operation to maintain high efficiency at light load. The quiescent current is only 120µA. It can be further reduced to 10µA by taking the SHUTDOWN pin high, which also disables the

device. The output voltage of the LT1300 can be set at either 5V or 3.3V via the logic controlled SELECT pin, and the LT1301 output can be set at either 5V or 12V using the same pin. The I_{LIM} pin allows the reduction of peak switch current, normally 1A, to approximately 400mA, increasing efficiency and allowing the use of even smaller components in lighter load applications.

Operation

Figure 1 is a block diagram of the LT1300/1301. Refer also to Figure 2 for associated component hook-up. When A1's negative input, related to the SENSE pin voltage by the appropriate resistor-divider ratio, is higher than the 1.25V reference voltage, A1's output is low. A2, A3, and

continued on page 12

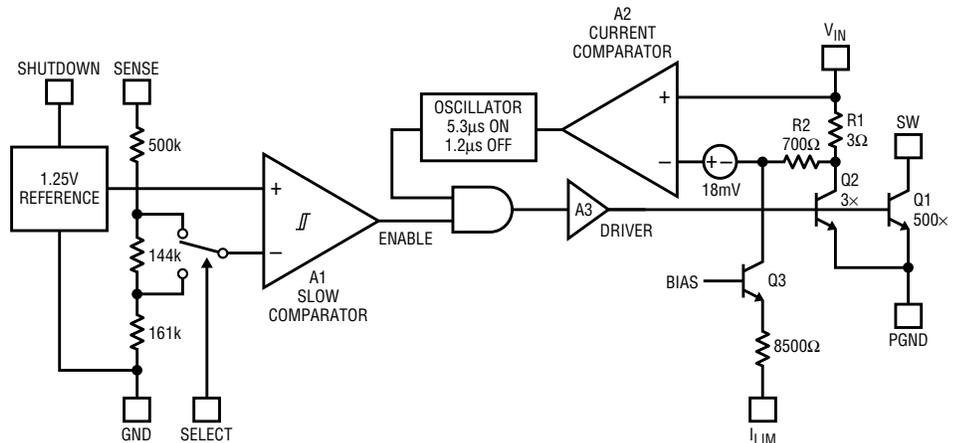


Figure 1. LT1300/LT1301 block diagram

Burst Mode™ is a trademark of Linear Technology Corporation.

Earwigs in the Drip Watering System? Parsnips for Dinner!

by Richard Markell

I've been doing a lot of thinking about earwigs lately. Earwigs are those bugs that look like little lobsters, with the little pincers on their tails (order Dermaptera). They completely blocked a filter in my drip watering system so that I had to clean it out every week. Not good. I spent many a sleepless night trying to reason out how they got into the pipes to be swept down to the point where they were trapped by the filter. Was there a hole underground? Were earwigs spontaneously generated inside the pipes? Were they delivered as protein-enriched water from my small water company? A sort of "big bug" theory of evolution?¹

We all solve engineering problems, both at work and at home. Jim Williams fixes Tektronix 547s; I engineer systems in the garden that water my parsnips. Is it the same thing? I got to thinking about the creative process. I've been tracing through the drip system in my mind, trying to figure out how the earwigs got into a closed system. Is this different from tracing through a buck regulator circuit to

find the source of too much output ripple? How about trying to find out why the last two bits on an A/D converter system toggle? The creative aspect of the thinking process is the same in each endeavor.

This issue is packed with articles on new products from LTC. Steve Pietkiewicz and Dale Eagar provide circuits and architectural insights into the new LT1300 and LT1301 micropower DC-to-DC converters. Steve provides the designer's perspective and Dale provides some novel circuits for the LT1300 series.

George Feliz describes his new series of high-speed operational amplifiers, which combine the high slew rates of current-feedback amplifiers with the benefits of traditional operational amplifiers to create the LT1354 through LT1365 series of amplifiers. In the related area of video products, John Wright presents his 70MHz, four-input video multiplexer, the LT1204. This product provides an incredible 90dB of isolation at 10MHz.

Bob Reay offers a thorough introduction to LTC's first digital-to-analog converter, the LTC1257. This 12-bit serial D/A converter typically achieves 1/4LSB DNL and 2LSBs INL error without trimming. The part complements our line of serial A/Ds quite nicely.

Alexander Strong introduces the JFET-input LT1113 operational amplifier. The LT1113 is the world's lowest-noise dual-JFET op amp; the part was designed to amplify high-impedance capacitive transducers. Tim Skovmand discusses 2-cell power management techniques and provides a complete 2-cell to 3.3V, 5V and 12V power-management system.

Also, there are many Design Ideas: an LCD bias generator, a linear-phase bandpass filter, a high-efficiency battery charger, a +5V to +3.3V converter for desktop computers, and a LT1087 GTL terminator.

¹ See the bottom of page 3 for the answer, "How they got into the pipes."

FAE Cameo: David Dinsmore

LTC now has twenty Field Application Engineers worldwide to assist our customers in the design and selection of circuits available from LTC. All of our FAEs are available by phone and, in certain situations, in person to help you design your circuitry. This space will profile one FAE per issue.

David Dinsmore works out of LTC's Southeast Sales office. He covers the states of Texas, Oklahoma, Alabama, Louisiana, Arkansas, Mississippi and the western half of Tennessee. David's expertise is in the areas of data-acquisition systems and servo-motor control.

Dave relates, "One of my most interesting projects was a 3/4HP motor-control system for a blood-analyzer centrifuge. It had to be precisely

positioned in either direction for loading and unloading the blood samples. The 20-inch-diameter rotor then had to be accelerated to 5000 RPM at a defined rate in 5.0 seconds. In addition, the rotational speed had to be held to 720 RPM \pm 0.1 RPM during the data-acquisition period to define the sample rate in an A/D conversion system. This Analog-to-digital control system comprised F/V and D/A converters, precision amplifiers and filters, high-voltage H-bridge drivers, and a microcontroller with digital filtering."

Dave recently talked to an engineer who had a very interesting application. He was building a hydrophone amplifier to track the movements of schools of fish. He had

gone so far as to have a taxidermist make a plaster mold of a rainbow trout. He and his co-workers spent hours painting the prototype trout to look very realistic. (This may be taking precision to the extreme.) He mounted the electronics (which, of course, use LTC op amps for signal conditioning) inside the plaster fish.

David and his wife, Donna, have been married for seven years. They have a 16-month-old baby girl, Dana, who, like her father, is already taking things apart to see how they work.

He enjoys golf, yard work (really?), and playing with his daughter. You can reach David through the LTC Southeast Sales office listed on the back of this magazine. **LT**

The LTC1257 Provides a Complete, Single-Supply, 12-Bit D/A in an SO-8 Package

by Robert Reay

Introduction

The new 8-pin SO LTC1257 requires no external components and provides one of the smallest, easiest-to-use 12-bit D/A (DAC) systems available. The part includes an output-buffer amplifier, a 2.048V voltage reference, and an easy-to-use, cascadable three-wire serial interface. The single supply voltage can range from 4.75V to 15.75V and an external reference can be used to override the internal reference to extend the output voltage range to 0V–12V. The power supply current is a low 350µA max when operating from a 5V supply, and the differential nonlinearity (DNL) is less than 1/2LSB (see Figure 1), with no missing codes.

Circuit Topology

Digital Section

The block diagram and pin diagram of the LTC1257 are shown in Figure 2. The digital section consists of a 12-bit shift register, control logic, DAC register, and 5V logic regulator. Signal lines include inputs CLK, D_{IN}, and $\overline{\text{LOAD}}$, and output D_{OUT}. The data on the D_{IN} pin is clocked into the shift register and the last bit in the shift register is shifted to D_{OUT} through a buffer on the rising edge of the clock. The MSB is loaded first and the LSB last. The DAC register loads the data from the shift register when $\overline{\text{LOAD}}$ is pulled low, and remains transparent until $\overline{\text{LOAD}}$ is pulled high and the data is latched. The logic regulator limits the internal logic's voltage swing to 5V, reducing clock noise in the analog section when V_{CC} is at 15V. However, the D_{OUT} pin will swing from GND to V_{CC}.

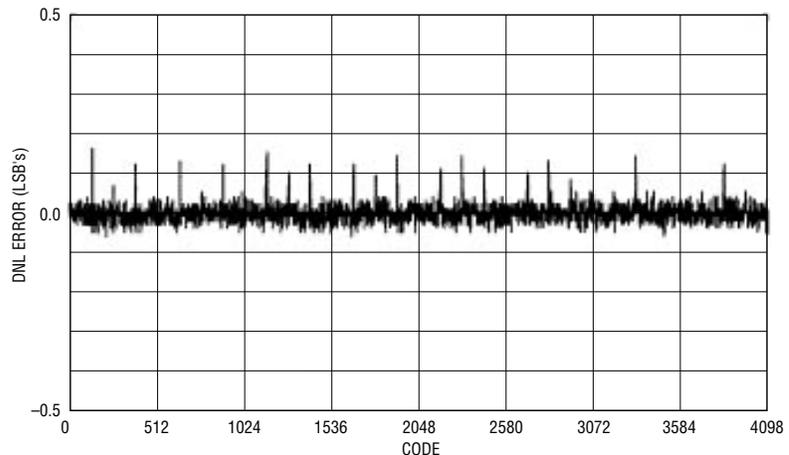


Figure 1. LTC1257 differential nonlinearity (DNL) plot

Multiple LTC1257s can be daisy-chained by connecting the D_{OUT} pin of one chip to the D_{IN} pin of the next, with the CLK and $\overline{\text{LOAD}}$ signals remaining common to all chips. The serial data is clocked to all of the DACs and the $\overline{\text{LOAD}}$ signal is pulled low to update all of them simultaneously. The serial interface can be clocked at any speed up to 1.4MHz.

Analog Section

The 12-bit DAC ladder, the 2.048V reference, and an op amp connected as a voltage follower make up the analog section. The DAC has been optimized for excellent DNL performance in a small area. Figure 3 shows the DAC ladder topology. A string of equal-valued resistors is connected between the reference pin and ground.

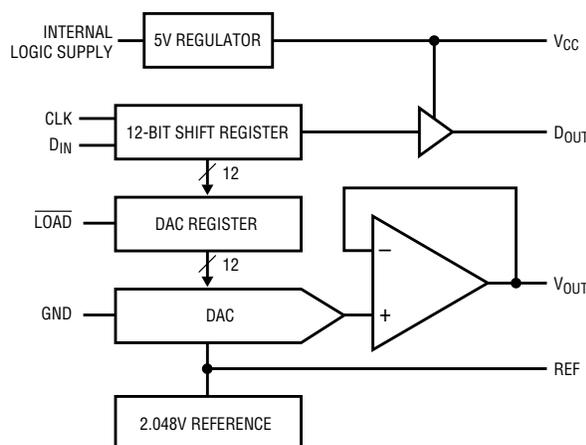


Figure 2a. LTC1257 block diagram

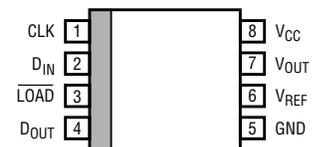


Figure 2b. LTC1257 pin diagram

How they got into the pipes

The earwigs got in through the opening in the anti-siphon valve. I solved the problem by putting a fine mesh (my wife's old stocking) over the valve.

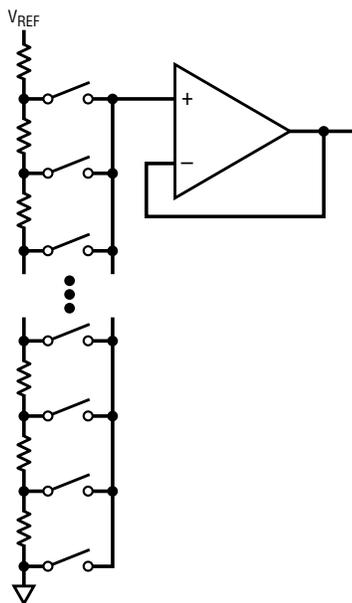


Figure 3. Equivalent DAC topology

A switch connects each resistor tap to the input of the op amp. For any given code, the corresponding switch is turned on, and the resistor ratio determines the fraction of the reference voltage appearing at the output of the buffer op amp. This topology guarantees no missing codes and the integral nonlinearity is determined by the matching of the resistors within the string.

Because a 12-bit DAC would require 4096 resistors and a large layout, we have developed a patented scheme in which only the MSBs are determined by the resistor string and the LSBs are decoded by a modified input stage in the op amp. This design dramatically reduces the number of resistors and the size of the DAC and maintains excellent DNL performance. The typical DNL error is 1/4LSB while the typical INL error is 2LSBs, without any costly trimming.

The internal voltage reference provides a constant 2.048V, making 1LSB equal to 500 μ V. The reference is connected to the DAC resistor ladder

and to the REF pin. The reference is a bootstrapped bandgap circuit with a typical temperature coefficient of 20ppm/ $^{\circ}$ C. The voltage reference output is turned off when the pin is forced above 2.5V, allowing an external, high-precision reference to be connected to the REF pin and DAC resistor ladder. By using the external reference, the full scale voltage of the DAC can be extended up to 12V. The external reference must be greater than 2.5V, less than $V_{CC} - 2.7V$, and must be capable of driving the 10k Ω minimum DAC resistor ladder.

The op amp buffer is connected as a voltage follower and has a common-mode range that extends from ground to within 2.7V of V_{CC} while sourcing 2mA. An internal NMOS transistor with a 200 Ω equivalent impedance pulls the output to ground. The output is protected against short circuits and is able to drive a capacitive load of up to 500pF without oscillation. Offset is 4mV max over temperature and the settling time is 6 μ s maximum.

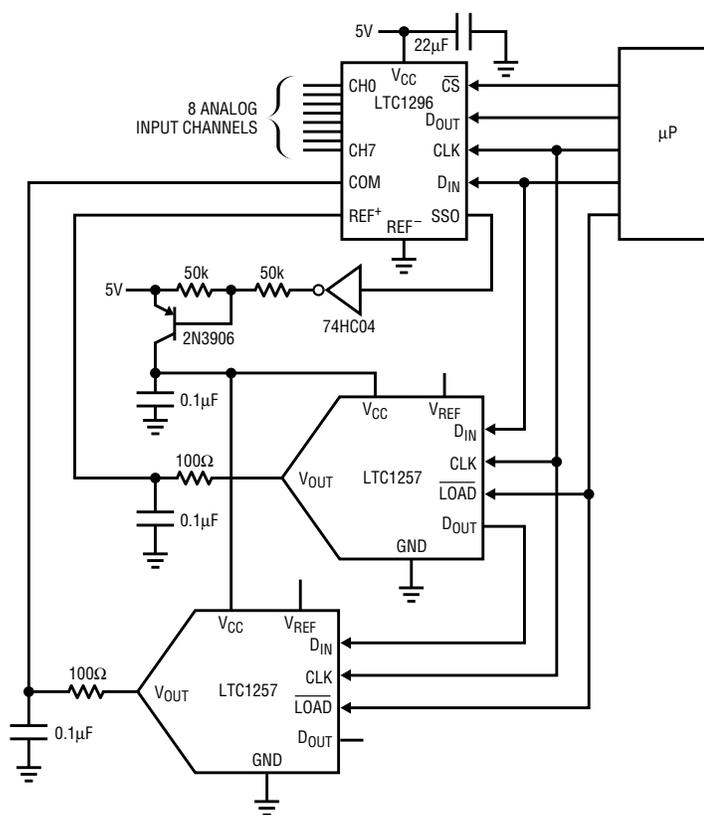


Figure 4. Auto-ranging, 8-channel ADC with shutdown

Applications

The LTC1257 is intended for applications where small size, low external parts count, low supply current, single-supply operation, and excellent DNL performance are needed. Applications include portable instrumentation, digitally controlled calibration, servo controls, process-control equipment, and automatic test equipment.

Two LTC1257s and a LTC1296 A/D can be used to build an auto-ranging, 8-channel ADC system with shutdown, as shown in Figure 4. Two LTC1257s are cascaded together and provide the zero and full-scale reference voltages for the LTC1296 A/D converter. The DAC outputs are filtered to remove the small amount of digital noise from the outputs. V_{CC} for the DACs is supplied via a PNP transistor. The microprocessor writes the two 12-bit full-scale and zero words to the DACs via the D_{IN} and CLK inputs, then pulls LOAD low to update the DAC outputs. With zero and full-scale set, an A/D conversion can be made.

continued on page 15

LT1204: High-Speed Video Multiplexer with Cable Driver has -90dB Crosstalk

by John Wright

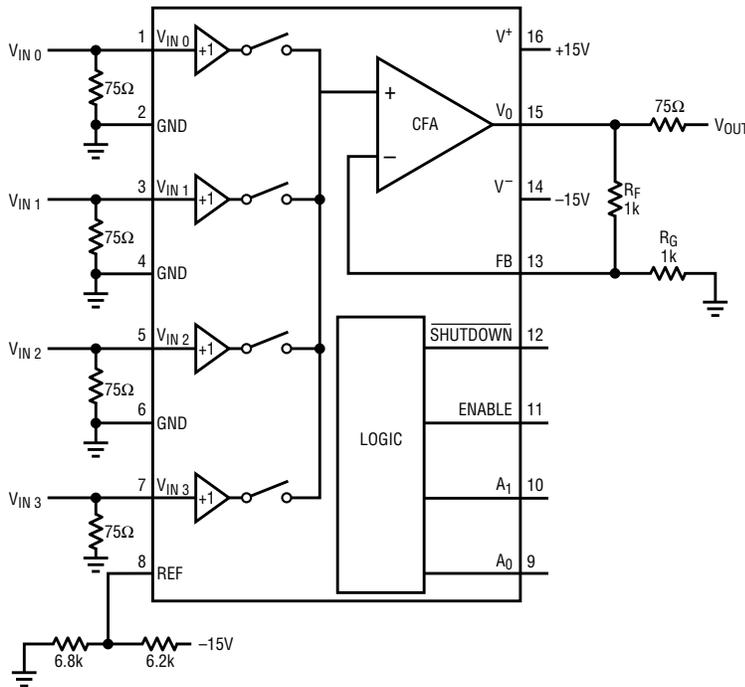


Figure 1. LT1204 block diagram

Introduction

The LT1204 is the first in a series of products developed by Linear Technology to solve difficult video switching and distribution problems in the new multimedia products. This new 4-input multiplexer includes a 75MHz current-feedback amplifier that will directly drive 75 ohm cables. We have developed a novel circuit technique to expand the number of multiplexers for large routing systems without degrading the signal integrity. This technique simplifies cable terminations as the number of inputs increases. Video specifications, such as differential gain and phase, gain flatness, and switching transients are at professional video levels. Unlike many multiplexers, which have 1V-2V input ranges, the LT1204 supports large input and output signal levels, which make it ideal for general-purpose analog signal se-

lection and multiplexing. The LT1204 is available in 16-lead PDIP and 16-lead SOL packages.

Figure 1 shows a block diagram of the LT1204. Its truth table appears as Table 1. The input buffers are actually low-insertion-loss tee switches designed to give the excellent crosstalk performance required for professional video. The switches are internally connected to the noninverting input of the CFA to reduce capacitance and improve the AC characteristics of the signal path; the inverting input is external for easy gain adjustment. The logic interface decodes channel select, shutdown, and enable/disable, the last of which puts the CFA into a true high output impedance state. A reference (Pin 8) is available for optimizing the internal logic circuitry for different input signal ranges.

The Challenge of Video Multiplexers

Before HDTV, CD Interactive, and the proliferation of video products, source selection was made during the blanking period, and the effects of switching transients were not visible. As multimedia, new special effects, and picture processing become popular, it has become necessary to switch video "in picture"; in such cases the nature of the switching transient is critical. Switching techniques that worked in the past now cause problems. Older bipolar ICs that switch lateral PNP transistors in the signal path take several microseconds to settle, blurring the transition between pictures. CMOS multiplexers, which are bidirectional, suffer from poor output-to-input isolation and cause transients to feed to the inputs. CMOS MUXs have been built with break-before-make switches to eliminate the talking between channels, but these suffer from output glitches large enough to interfere with the sync circuitry. By contrast, the LT1204 is fabricated on LTC's complementary-bipolar process to attain good switching characteristics, buffering, crosstalk, and speed. Let's look at these areas one-by-one to see how they stack up.

Table 1. LT1204 truth table

A ₁	A ₀	ENABLE	SHUTDOWN	Channel Selected
0	0	1	1	V _{IN0}
0	1	1	1	V _{IN1}
1	0	1	1	V _{IN2}
1	1	1	1	V _{IN3}
X	X	0	1	High-Z Output
X	X	X	0	OFF

Switching Characteristics

Switching between channels is a make-before-break condition where both inputs are on momentarily. The input with the largest positive voltage determines the output level. If both inputs are equal, there is only 40mV of error at the input of the CFA during the transition. The reference adjust (Pin 8) allows the user to trade positive input voltage range for switching time. For example, on $\pm 15V$ supplies, setting the voltage on pin 8 to $-6.8V$ reduces the switching transient duration to 50ns and the positive input range from $+6V$ to $+2.35V$; the negative input range is independent of the setting on pin 8 and remains at $-6V$. When switching composite video "in picture," this short (50ns) transient is imperceptible, even on high quality monitors. The reference pin has no effect when the LT1204 is operating on $\pm 5V$, and should be grounded in this situation. Figure 2 is a scope photograph of the output switching transient with a 2MHz sine wave connected to V_{IN0} and V_{IN1} .

Input Buffers

The buffers isolate the inputs when the make-before-break switching occurs. The design of these input buffers included special attention to their DC matching and dynamic characteristics. The DC input-offset match between channels is more important to the video engineer than is the actual value of the input offset. A DC mismatch as small as 3mV between channels is just visible on a quality video monitor. The typical V_{OS} mismatch between channels on the LT1204 is about 300 μV .

Crosstalk

The crosstalk (more accurately, all hostile crosstalk) is measured by driving signal into any three of the four inputs and selecting the fourth input with logic control. This fourth input is either shorted to ground or terminated in an impedance. All hostile crosstalk is defined as the ratio in dB of the signal, at the output of the CFA, to the signal on the three driven in-

puts. Disable crosstalk is measured with all four inputs driven and the part disabled. Crosstalk is critical in many applications where video multiplexers are used. In professional video systems, a crosstalk figure of $-72dB$ is a desirable specification.

The key to the outstanding crosstalk performance of the LT1204 is the tee switch shown in Figure 3. When the tee switch is on (Q2 off) Q1 and Q3 are a pair of emitter-followers with excellent AC response for driving the CFA. When the decoder turns off the tee switch (Q2 on), the emitter-base junctions of Q1 and Q3 become reverse biased while the Q2 emitter absorbs current from I_1 . Not only do the reverse-biased emitter-base

junctions provide good isolation, but any signal at V_{IN0} coupling to the Q1 emitter is further attenuated by the shunt impedance of the Q2 emitter. Current source I_2 routes current to any ON switch.

Crosstalk performance is strongly affected by the IC package and the PC board layout, as well as by the circuit design. The die layout uses grounds between the inputs to isolate adjacent channels, and the output and feedback pins are on opposite sides of the die from the inputs. Laying out a PC board that provides 90dB of isolation from all crosstalk at 10MHz is not a trivial task. That crosstalk level corresponds to a 30 μV output below a 1V input at 10MHz. We have fabricated a

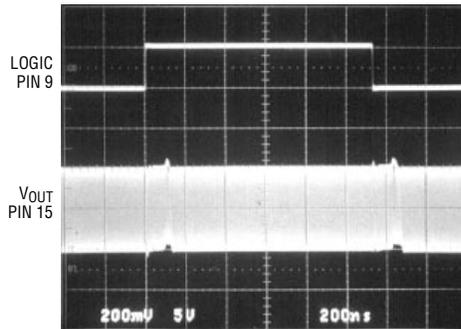


Figure 2. V_{IN0} and V_{IN1} connected to a 2MHz sinewave, pin 8 voltage = $-6.8V$

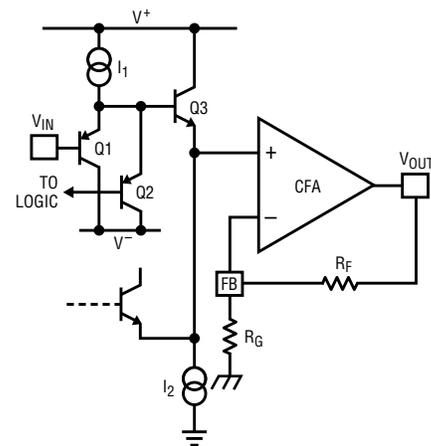


Figure 3. Tee switch

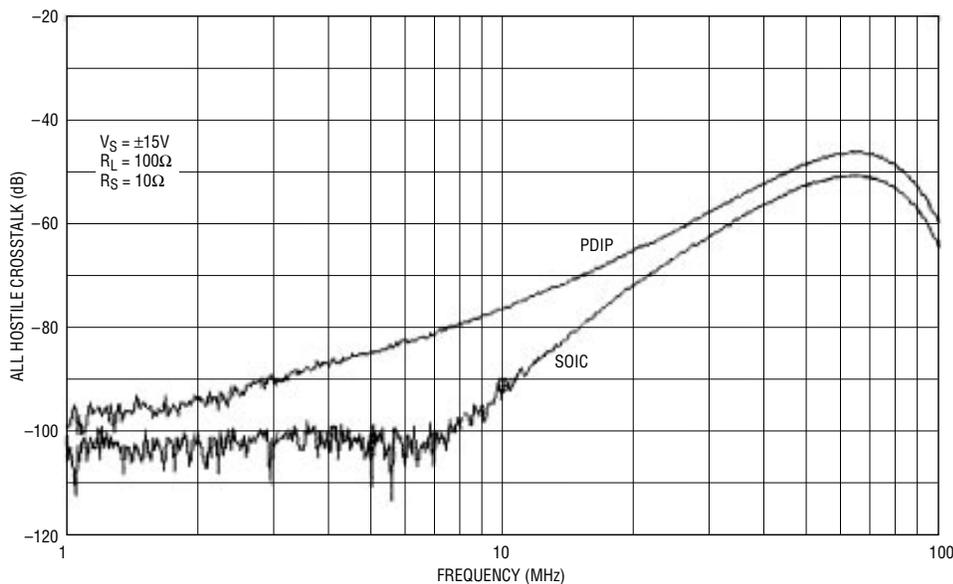


Figure 4. All hostile crosstalk of LT1204 in PDIP and SOIC

demonstration board to show the component and ground placement required to attain these crosstalk numbers. Figure 4 is a graph of all hostile crosstalk for both the PDIP and SO packages. It has been found empirically from these PC boards that capacitive coupling across the package of greater than 3fF (yes, that is 0.003 picofarads) will diminish the rejection; we recommend that you use this proven layout in your designs.

Multiplexer Expansion

LT1204s can be paralleled by shorting their outputs together to expand the number of MUX inputs. This new multiplexer uses a novel circuit (patent pending) to ensure that the unselected amplifiers do not load or alter the cable termination and that there is no shoot-through current when the outputs of two or more amplifiers are shorted together. (Shoot-through current is a spike of power-supply current caused by both amplifiers being on at the same time.) When the LT1204 is disabled (pin 1 low), the output stage is turned off and an active buffer senses the output voltage and drives the feedback pin of the CFA (Figure 5). This bootstraps the feedback resistors and raises the true output impedance of the circuit. For the condition where $R_F = R_G = 1k\Omega$, the output impedance is typically raised to $25k\Omega$ during disable. If the part is shut down, however, the bootstrapping is inoperative, and the feedback resistors will load the output ($R_{OUT} = 2k\Omega$). If the CFA is operated at a gain of +1, the feedback resistor will not load the output even in shutdown mode, because there is no resistive path to ground; however, there will be a 6dB loss through the cable.

Figure 6 is a frequency-response plot showing the effect of using the disable feature versus using the shutdown feature. In this example, four LT1204s were connected together at their outputs to form a 16-to-1 MUX. The plot shows the effect of the bootstrapping circuit, which eliminates the improper cable termination due to the feedback resistors loading the cable.

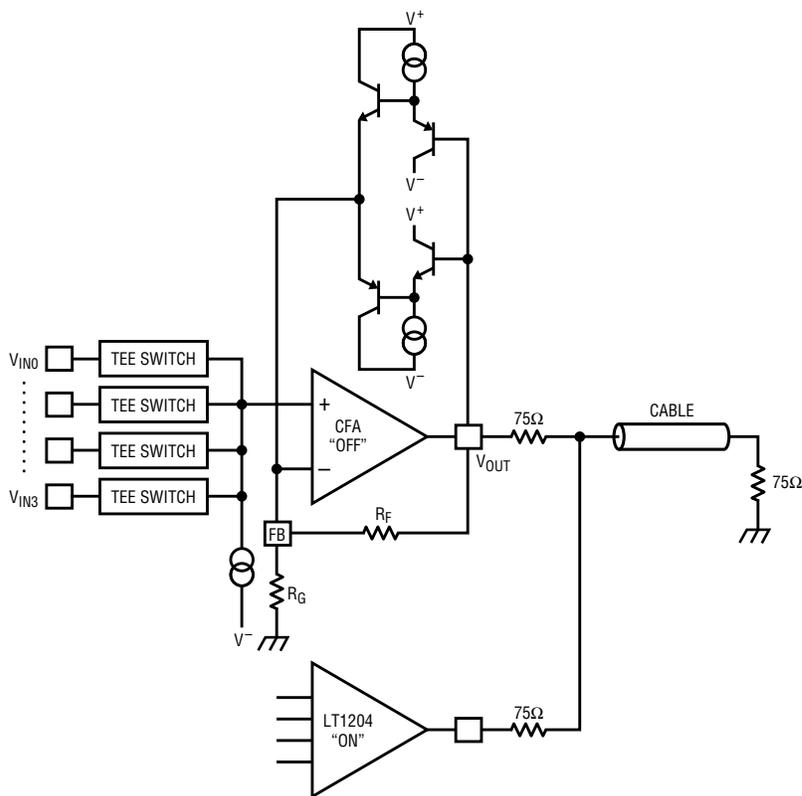


Figure 5. Active buffer drives FB node during disable

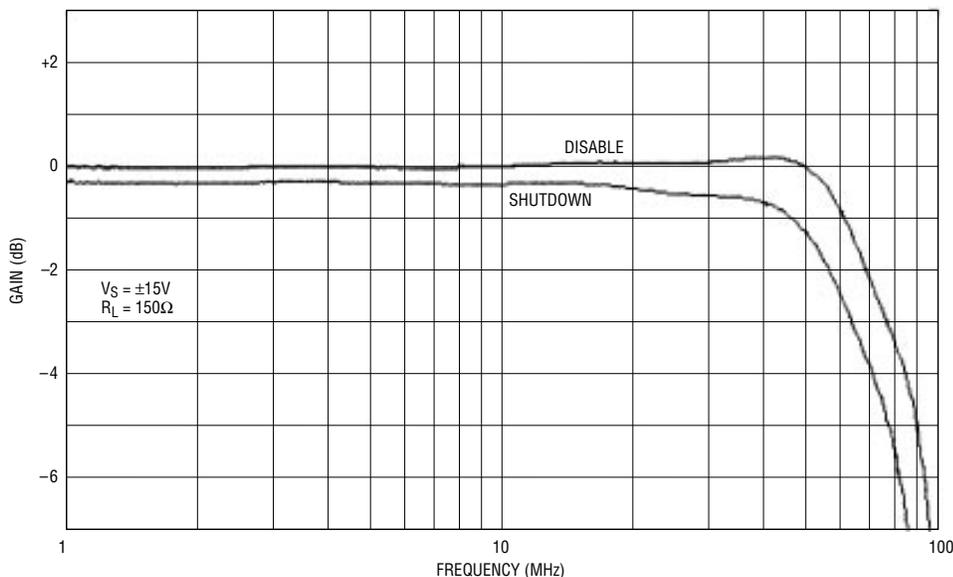


Figure 6. 16-to-1 multiplexer response using disable feature versus shutdown feature

Continued on page 16

The World's Lowest-Noise Dual-JFET Op Amp, the LT1113, Debuts

by Alexander Strong

Introduction

The LT1113 joins the LTC family of low-noise op amps as the lowest-noise dual-JFET op amp available. This op amp combines the low current noise (less than $10\text{fA}/(\text{Hz})^{1/2}$) of a FET op amp with a maximum voltage noise of $6.0\text{nV}/(\text{Hz})^{1/2}$. In addition, the LT1113 is stable for a gain of +1 and will handle 1000pF load capacitances. All of this is available in an 8-pin small-outline surface mount package with the standard pinout. Most op amps require a relaxation of specifications in the surface mount package due to assembly shifts. For the LT1113CS8, spec relaxation is not necessary. The LT1113CS8 specs are identical to the LT1113CN8. Table 1 highlights some of the guaranteed specifications for the low-cost grade.

Table 1. LTC1113CS8 guaranteed specifications: 100% tested, $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$

Voltage Noise @ 1kHz	$6.0\text{nV}/\sqrt{\text{Hz}}$ Max
V_{OS}	1.8mV Max
A_{VOL} ($R_L = 10\text{k}\Omega$)	1000V/mV Min
GBWP @ 100kHz	4.5MHz Min
Slew Rate	$2.5\text{V}/\mu\text{s}$ Min
I_{SUPPLY} per amp	6.5mA Max

Hydrophones Require High Input Impedance

The combination of low voltage noise and low current noise makes the LT1113 suitable in applications where low level signals need to be amplified from high impedance capacitive transducers. Photo diodes, hydrophones, and accelerometer transducers exhibit high impedances, which make the op amp current noise dominate the total output noise:

$$V_n = A_V \sqrt{V_n^2(\text{OP AMP}) + 4kT \cdot 2R_{\text{TRANS}} + 2q I_B \cdot 2(R_{\text{TRANS}})^2}$$

Current noise is derived from the DC value of the FET input bias current, or

$$I_n(\text{fA}/(\text{Hz})^{1/2}) = (2q I_B)^{1/2}$$

where $q = 1.6\text{E}-19$

For a 300pA I_B , a $9.8\text{fA}/(\text{Hz})^{1/2}$ current noise is multiplied by the transducer impedance, which adds to the total output voltage noise of the amplifier. The best low-noise bipolar op amps cannot match the performance of the LT1113 where high-impedance transducers are used. Figure 1 shows a comparison between the LT1113 and the LT1124 bipolar op amp. The LT1124 has 40% less voltage noise at 1kHz than the LT1113 and is a better choice for transducer impedances less than $1\text{k}\Omega$, but for transducer impedances over $100\text{k}\Omega$, the LT1113 is clearly the champ. The dashed lines on Figure 1 show the total noise with a parallel 1000pF capacitance (since most hydrophone and accelerometer transducers are capacitive by nature). The graph shows that when the LT1113 is used, the total noise is dominated by the transducer impedance and not the amplifier, as in the case of the LT1124.

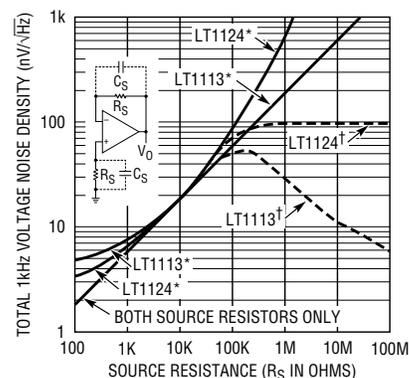


Figure 1. Comparison of LT1113 and LT1124 total output 1kHz voltage noise versus source resistance

* PLUS BOTH SOURCE RESISTORS
 † SOURCE RESISTORS || 1000pF SOURCE CAPACITANCE

$$V_n = \sqrt{V_n^2(\text{OP AMP}) + 4kT \cdot 2R_{\text{SOURCE}} + 2q I_B \cdot 2(R_{\text{SOURCE}})^2}$$

The two basic gain configurations are shown in Figure 2. The noninverting gain configuration is used for voltage-mode transducers such as hydrophones, whereas the inverting gain configuration is used for charge transducers such as accelerometers. In each example, a source-balancing impedance is added to improve the overall performance of the amplifier. R_B is selected to cancel the voltage offset due to the input bias current flowing

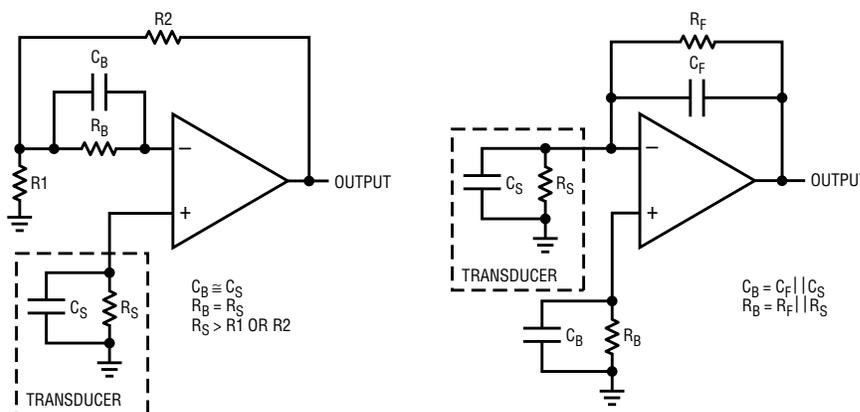


Figure 2. Noninverting and inverting gain configurations

into the source impedance. This is especially important as the operating temperature increases, since FET input bias currents are usually uncancelled, and double for every 10 degrees C. A parallel capacitor C_B cancels the pole that is caused by the amplifier input capacitance and R_B .

Applications

Figure 3 shows a low-noise hydrophone amplifier with a DC servo. Here one half of the LT1113 is configured in the noninverting mode to amplify a voltage signal from the hydrophone, and the other half of the LT1113 nulls errors due to voltage and current offsets of the amplifier and to impedance mismatches. The value of C_1 depends

on the capacitance of the hydrophone, which can range from 200pF to 8000pF. The time constant of the servo should be larger than the time constant of the hydrophone capacitance and the 100M Ω source resistance. This will prevent the servo from canceling the low-frequency signals from the hydrophone.

Another popular charge-output transducer is the accelerometer. Since precision accelerometers are charge output devices, the inverting mode is used to convert the transducer charge to an output voltage. Figure 4 is an example of an accelerometer with a DC servo. The charge from the transducer is converted to a voltage by C_1 , which should equal the transducer capaci-

tance plus the input capacitance of the op amp. The noise gain will be $1 + C_1/C_T$. The low frequency bandwidth will depend on the value of R_1 (or $R_1 \times (1+R_2/R_3)$ for a Tee network). As with the hydrophone example, the time constant of the servo should be larger than the time constant of the amplifier.

Conclusion

The LT1113 is not just another op amp. As the lowest-noise dual-JFET op amp in the market place, the LT1113 should be the first choice where high-impedance transducers are used. The 8-pin surface mount package will allow the LT1113 to satisfy the most demanding board space requirements. **LT**

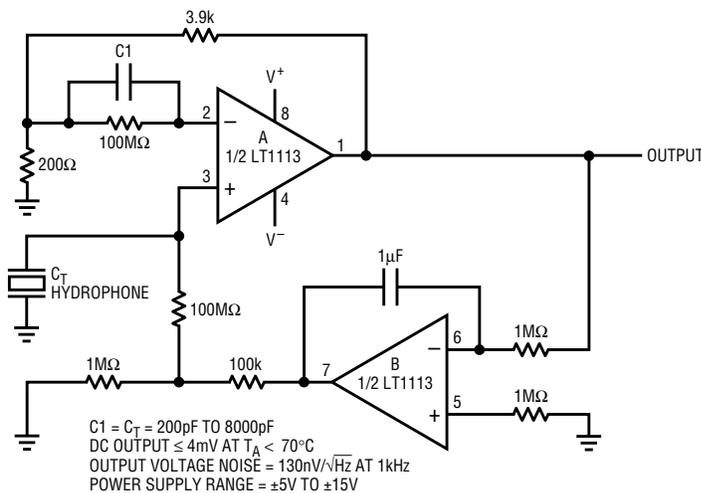


Figure 3. Low-noise hydrophone amplifier with DC servo

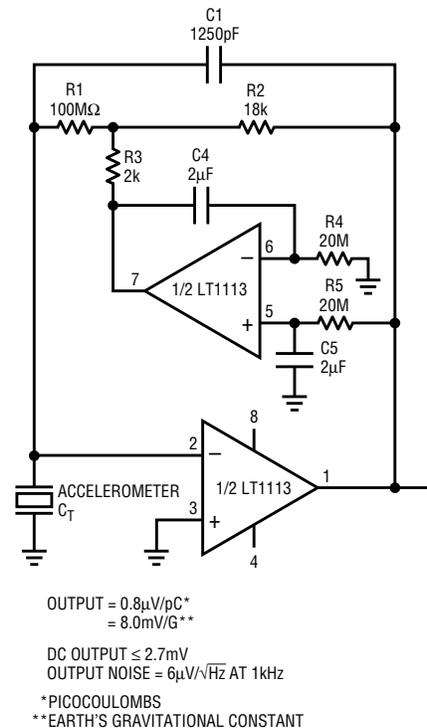


Figure 4. Accelerometer circuit with DC servo

A New Family of High-Speed, Low-Power Operational Amplifiers

by George Feliz

Introduction

A new family of high-speed operational amplifiers from LTC utilizes a novel circuit topology that blends the high slew rate of current-feedback amplifiers with the benefits of true voltage-feedback amplifiers. Compared to other devices with similar bandwidths, these amplifiers offer lower supply current, higher slew rate, better DC specifications, faster settling times, and lower input noise. The family is built on LTC's complementary bipolar process and encompasses bandwidths from 12MHz to 70MHz. The fastest parts are the LT1363, LT1364, and LT1365, which have 70MHz gain bandwidth and 1000V/μs slew rate, and consume only 6mA of supply current per amplifier. The lowest power devices are the LT1354, LT1355, and LT1356, which draw only 1mA of supply current and provide 12MHz of bandwidth and 400V/μs slew rate. In between are the LT1357, LT1358, and LT1359, which have 25MHz gain bandwidth and 600V/μs slew rate and consume 2mA, and the LT1360, LT1361, and LT1362, which have 50MHz bandwidth and 800V/μs slew rate, and consume 4mA.

Table 1 summarizes the important specifications of each device. All

Table 1. Important specifications; LT1354, LT1357, LT1360, and LT1363 op amp families

Parameter	Conditions	LT1354/5/6	LT1357/8/9	LT1360/1/2	LT1363/4/5	Units
V _{OS} (max)	V _S = ±5V, ±15V	1	0.6	1	1.5	mV
I _B (max)	V _S = ±5V, ±15V	0.3	0.5	1	2	μA
I _{OS} (max)	V _S = ±5V, ±15V	70	120	250	350	nA
A _{VOL} (min)	V _S = ±5V, 500Ω	10	10	3	3	V/mV
	V _S = ±15V, 1kΩ	20	20	4.5	4.5	V/mV
GBW	V _S = ±15V	12	25	50	70	MHz
SR	V _S = ±15V	400	600	800	1000	V/μs
t _{SETTLE}	10V step, 0.1%	240	170	60	50	ns
CMRR (min)	V _S = ±15V	86	86	86	86	dB
	V _S = ±5V	80	80	79	78	dB
PSRR (min)	V _S = ±2.5V to ±15V	92	92	97	90	dB
Noise voltage	10kHz	10	8	10	10	nV/√Hz
Noise current	10kHz	0.6	0.8	1	1.2	pA/√Hz
Output swing	V _S = ±15V, 500Ω	12.5	12.5	13	13	V
	V _S = ±5V, 150Ω	3	3	3.2	3.4	V
I _{SUPPLY}	V _S = ±15V	1	2	4	6	mA

devices operate over a wide supply voltage range of ±2.5V to ±18V and are available in dual, single, and quad versions. The single and dual versions are available in 8-pin DIPs and surface mount packages. The quad versions are available in 14-pin DIPs and narrow, S16 surface mount packages.

Background

The new topology changes the relationship between slew rate and supply current found in traditional voltage-feedback amplifiers. In order to understand the circuit, let's review a traditional high-speed, voltage-feedback design, as shown in Figure 1. The input pair Q1 and Q2 is resistively degenerated and feeds PNP cascodes Q3 and Q4. Differential-to-single-ended conversion is performed by the mirror Q5-Q7. The collectors of Q4 and Q5 form the high-impedance gain node with capacitance C_T, establishing the dominant pole. A unity-gain buffer follows the gain node. The slew rate is determined by the current available to charge C_T, which, in this case, is I_O. Since the slew rate is I_O/C_T, it is directly proportional to supply current. In order to obtain high slew rates, the circuit's quiescent currents must be large. For instance, a 1mA current is required to obtain 250V/μs with 4pF of capacitance. The bandwidth of the amplifier

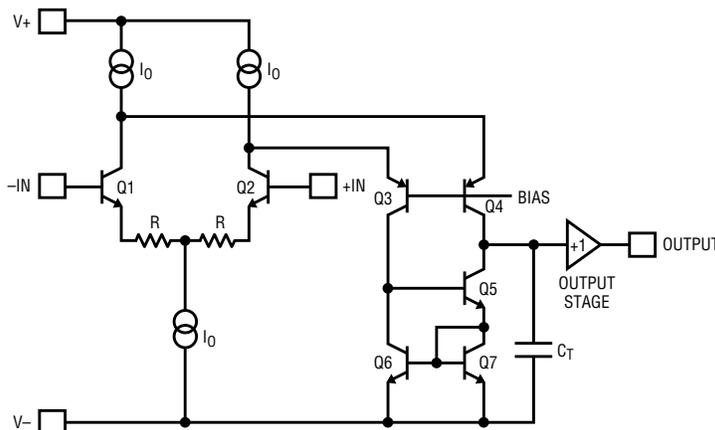


Figure 1. Traditional high-speed amplifier—simplified schematic

is determined by R and C_T and is given by $1/(2\pi RC_T)$. The useable bandwidth is typically limited by other poles in the frequency response, so R is selected to obtain adequate stability. For $R = 1k\Omega$ and $C_T = 4pF$, the bandwidth is 40MHz. Once the slew rate and bandwidth are chosen, the DC performance is set by the degeneration of the input pair. With $I_O = 1mA$ and $R = 1k\Omega$, a resistor mismatch of only 0.2% gives 1mV of input offset voltage. The open-loop gain is also reduced by the input degeneration, as it is inversely proportional to R . For high-slew-rate designs, the input bias current is high because it is also directly proportional to I_O . In our example, if the transistor beta is 100, the input bias current would be $5\mu A$ and the offset current would be about 500nA. Input noise is also degraded due to the resistor noise and reduced gain.

The New Topology

Figure 2 is a simplified schematic of the new circuit. The circuit looks similar to a current-feedback amplifier, but both inputs are high impedance as in a traditional voltage-feedback amplifier. A complementary cascade of emitter followers Q1-Q4 buffers the noninverting input and drives one side of a resistor. The other side of the resistor is driven

by Q5-Q8, which form a buffer for the inverting input. The input voltage appears across the resistor, generating a current that is mirrored by Q9-Q14 into the high impedance node. Q15-Q18 form an output stage. In a current-feedback amplifier, there would be an external resistor connected between the output and the emitters of Q3 and Q4, which would be the inverting input.

The bandwidth, as before, is $1/(2\pi RC_T)$, but the current available to slew C_T is the differential input voltage divided by $2R$, so the slew rate is independent of the operating currents of the input stage (which can then be reduced). For a 4V input step, a 2k Ω resistor, and a 4pF capacitor, the slew rate is ideally 500V/ μs . The high slew rate and balanced input stage significantly reduce settling time. As with current-feedback amplifiers, the RC time constant sets both the small and large signal responses. Figure 3 shows the large signal response of the family of amplifiers.

The new topology provides significantly better DC performance. The offset does not rely on tight resistor matching as it does in the conventional circuit, but rather on transistor matching and errors in the current mirrors. A mismatch of 4% between the input devices gives 1mV of input

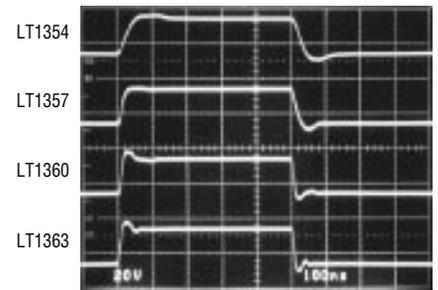


Figure 3. Large signal step response: LT1354, LT1357, LT1360, LT1363

offset voltage; this degree of matching is more readily achieved than the 0.2% resistor matching required for the conventional circuit. A $1\mu A$ mirror error will show up as 2mV of V_{OS} for $R = 2k\Omega$. It is practical to reduce the value of R in this circuit, increasing the open-loop gain, decreasing offset contributions from the current mirrors, and reducing noise. Input bias currents are reduced in two ways: the input devices can run at lower currents because the slew rate is independent of their operating current, and the NPN and PNP base currents tend to cancel. For example, if the input devices run at $200\mu A$, the input bias current will be less than $1\mu A$, even if the betas of the NPN and PNP mismatch by a factor of two. The balanced inputs of the new topology also provide excellent rejection of power-supply and common-mode variations.

The circuit has one other noteworthy feature—it is able to drive capacitive loads and remain stable. The R_C - C_C network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving a capacitive load, the network is incompletely bootstrapped and adds to the compensation network. The added capacitance provided by C_C slows down the amplifier and the zero created by R_C adds phase margin,

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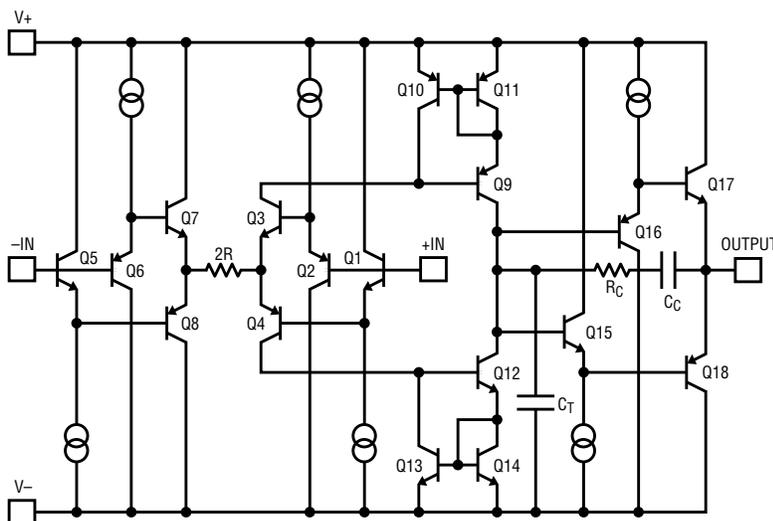


Figure 2. New high-speed amplifier—simplified schematic

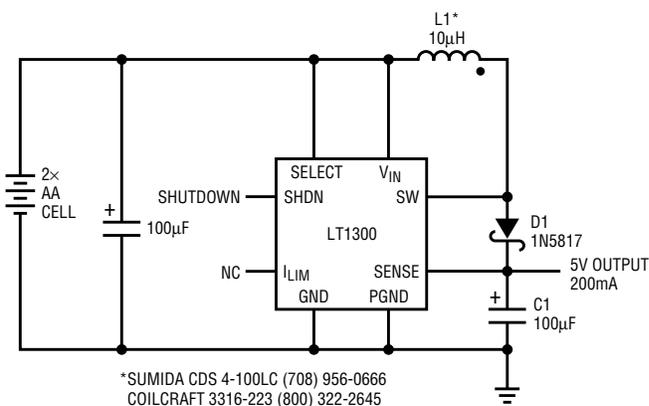


Figure 2. 2-cell to 5 volt DC/DC converter delivers >200mA with a 2.0 volt input

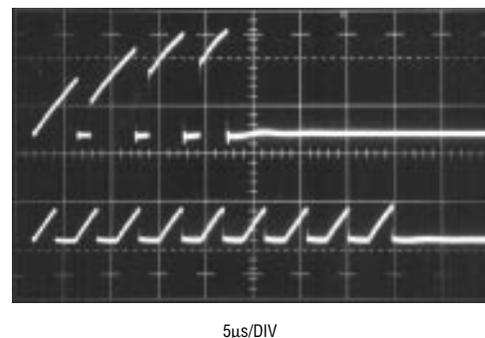


Figure 3. Switch pin current with I_{LIM} floating or grounded

LT1300, continued from page 1

the oscillator are turned off, drawing no current. Only the reference and A1 consume current, typically 120µA. When the voltage at the SENSE pin decreases enough to overcome A1's 6mV hysteresis, A1's output goes high, enabling the oscillator, A2, and A3. Quiescent current increases to 2mA as the device prepares for high-current switching. Q1 then turns on in a controlled saturation for (nominally) 5.3µs or until current comparator A2 trips, whichever comes first. After a fixed off-time of (nominally) 1.2µs, Q1 turns on again. Q1's switching causes current to alternately build up in L1 and dump into output capacitor C1 via D1, increasing the output voltage. When the output is high enough to cause A1's output to go low, switching action ceases. C1 is left to supply current to the load until V_{OUT} decreases enough to force A1's output

high, and the entire cycle repeats. If switch current reaches 1A, causing A2 to trip, switch on-time is reduced and off-time increases slightly. This allows continuous mode operation during bursts. A2 monitors the voltage across 3Ω resistor R1. Q2's collector current is set by the emitter-area ratio to 0.6% of Q1's collector current. When R1's voltage drop exceeds 18mV, A2's output goes high, truncating the on-time portion of the oscillator cycle and increasing off-time to about 2µs, as shown in Figure 3, trace A. Eighteen millivolts across R1 corresponds to a switch current of 1A. This peak current can be reduced by tying the I_{LIM} pin to ground, causing 15µA to flow through R2 into Q3's collector. Q3's current causes a 10.4mV drop in R2, so that only 7.6mV is required across R1 to turn off the switch. This corresponds to a 400mA switch current, as shown in

Figure 3, trace B. The reduced peak switch current reduces I²R losses in Q1, L1, C1, and D1. You can increase efficiency by doing this, provided the output-current reduction is acceptable. Lower peak currents also extend alkaline battery life, due to the alkaline cells' high internal impedance.

Five Volts from Two Cells

Figure 2's circuit provides 5V from a 2-cell input. Shutdown is effected by taking the SHUTDOWN pin high. V_{IN} current drops to 10µA in this condition. This simple boost topology does not provide output isolation, and in shutdown the load is still connected to the battery via L1 and D1. Figure 4 shows the efficiency of the circuit with a range of input voltages, including a fresh battery (3V) and an "almost-dead" battery (2V). At load currents below a few milliamperes, the 120µA quiescent cur-

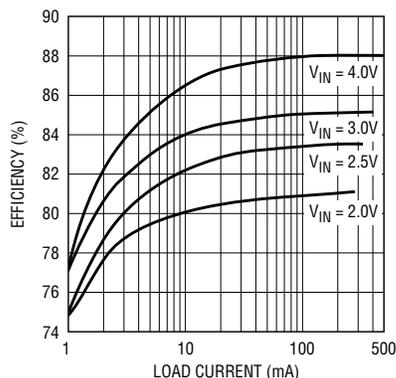


Figure 4. Efficiency of Figure 2's circuit

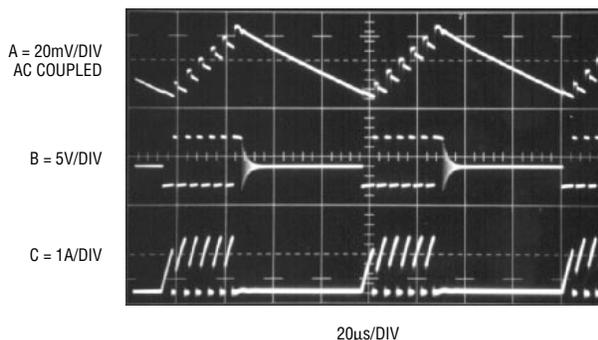


Figure 5. Burst Mode™ operation in action

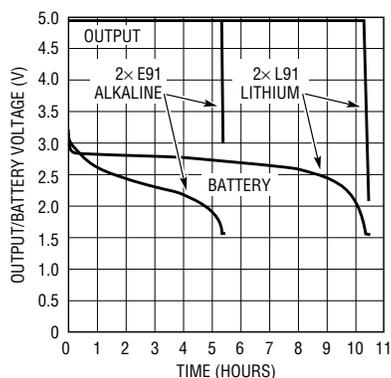


Figure 6. Two Eveready L91 lithium AA cells provide approximately twice the life of E91 alkaline cells at a 100mA load current

rent of the device becomes significant, causing the fall-off in efficiency detailed in the figure. At load currents in the 20mA to 200mA range, efficiency flattens out in the 80% to 88% range, depending on the input. Figure 5 details circuit operation. V_{OUT} is shown in trace A. The burst-repetition pattern is clearly shown as V_{OUT} decays, then steps back up due to switching action. Trace B shows the voltage at the switch node. The damped, high-frequency waveform at the end of each burst is due to the inductor “ringing off,” forming an LC tank with the switch and diode capacitance. It is not harmful and contains far less energy than the high-speed edge which occurs when the switch turns off. Switch current is shown in trace C. The current comparator inside the LT1300 controls peak switch current, turning off the

switch when the current reaches approximately 1A.

Although efficiency curves present useful information, a more important measure of battery-powered DC/DC converter performance is operating life. Figures 6 and 7 detail battery life tests with Figure 2’s circuit at load currents of 100mA and 200mA, respectively. Operating-life curves are shown using both Eveready E91 alkaline cells and new L91 “Hi-Energy” lithium cells. These lithium cells, new to the market, are specifically designed for high-drain applications. The performance advantage of lithium is about 2:1 at 100mA load current (Figure 6), increasing to 2.5:1 at 200mA load (Figure 7). Alkaline cells perform poorly at high drain rates because their internal impedance ranges from 200mΩ to 500mΩ, causing a large voltage drop within the

cell. The alkaline cells feel quite warm at 200mA load current, the result of I^2R losses inside the cells.

The reduced-power circuit shown in Figure 8 can generate five volts at currents up to 50mA. Here the I_{LIM} pin is grounded, reducing peak switch current to 400mA. Lower profile components can be used in this circuit. The capacitors are C-case size solid tantalum and inductor L1 is the tallest component at 3.2mm. The reduced peak current also extends battery life, since the I^2R loss due to internal battery impedance is reduced. Figure 9 details efficiency versus load current for several input voltages and Figure 10 shows battery life at a 50mA load. Note that the L91 lithium battery lasts only about 40% longer than the alkaline. The higher cost of the lithium cells makes the alkaline cells more

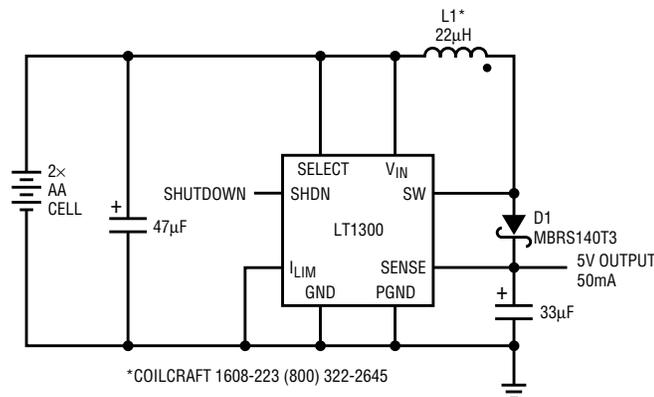


Figure 8. Lower-power applications can use smaller components. L1 is tallest component at 3.1mm

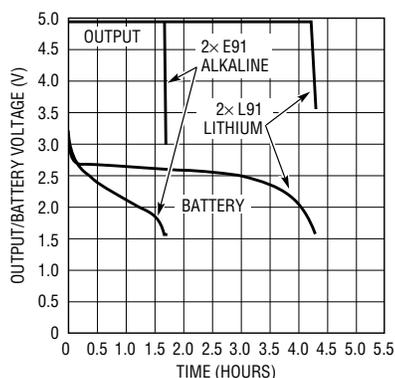


Figure 7. Doubling load current to 200mA causes E91 Alkaline battery life to drop by 2/3; L91 lithium battery shows 2.5:1 difference in operating life

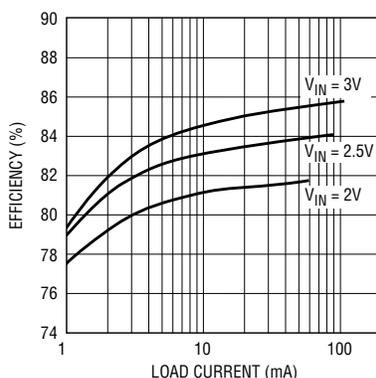


Figure 9. Efficiency of Figure 8’s circuit

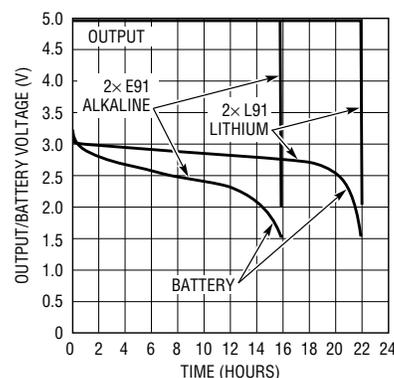


Figure 10. 50mA load and reduced switch current are kind to E91 AA alkaline battery; the advantages of L91 lithium are not as evident

cost-effective in this application. A pair of Eveready AAA alkaline cells (type E92) lasts 96.6 hours with 5mA load, very close to the rated capacity of the battery.

A 4-Cell Application

A 4-cell pack is a convenient, popular battery size. Alkaline cells are sold in 4-packs at retail stores and four cells usually provide sufficient energy to keep battery replacement frequency reasonable. Generating 5V from four cells, however, is a bit tricky. A fresh 4-cell pack has a terminal voltage of 6.4V, but at the end of its life, the pack's terminal voltage is around 3.2V; hence, the DC/DC converter must step the voltage either up or down, depending on the state of the batter-

ies. A flyback topology with a costly, custom-designed transformer could be employed, but Figure 11's circuit gets around these problems by using a flying-capacitor scheme along with a second inductor. The circuit also isolates the input from the output, allowing the output to go to zero volts during shutdown. The circuit can be divided conceptually into boost and buck sections. L1 and the LT1300 switch comprise the boost or step-up section, and L2, D1, and C3 comprise the buck or step-down section. C2 is charged to V_{IN} and acts as a level shift between the two sections. The switch node toggles between ground and $V_{IN} + V_{OUT}$, and the L2-C2-diode node toggles between $-V_{IN}$ and $V_{OUT} + V_D$. Figure 12 shows efficiency versus load current for the circuit. All four

energy-storage elements must handle power, which accounts for the lower efficiency of this circuit compared to the simpler boost circuit in Figure 2. Efficiency is directly related to the ESR and DCR of the capacitors and inductors used. Better capacitors cost more money. Better inductors do not necessarily cost more, but they do take up more space. Worst-case RMS current through C2 occurs at minimum input voltage and measures 0.4A at full load with a 3V input. C2's specified maximum RMS current must be greater than this worst-case current. The Sanyo capacitors noted specify a maximum ESR of 45mΩ with a maximum ripple current rating of 2.1A. The Gowanda inductors specify a maximum DCR of 58mΩ.

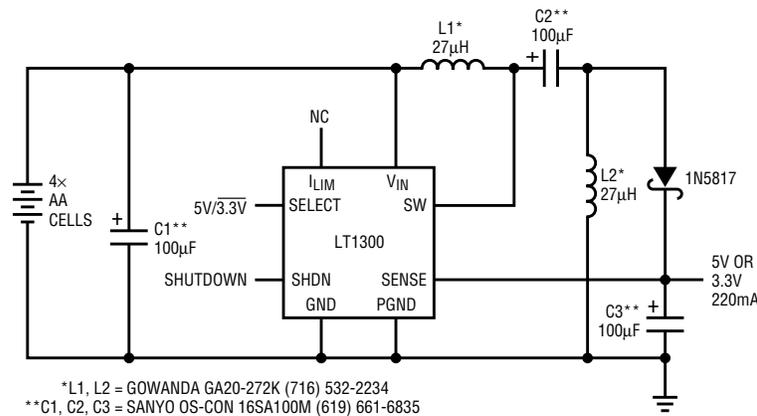


Figure 11. 4-Cell to 3.3V or 5V converter output goes to zero when in shutdown. Inductors may have, but do not require coupling; a transformer or two separate units can be used

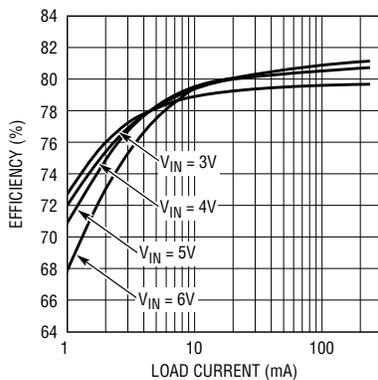


Figure 12. Efficiency of up-down converter in Figure 11

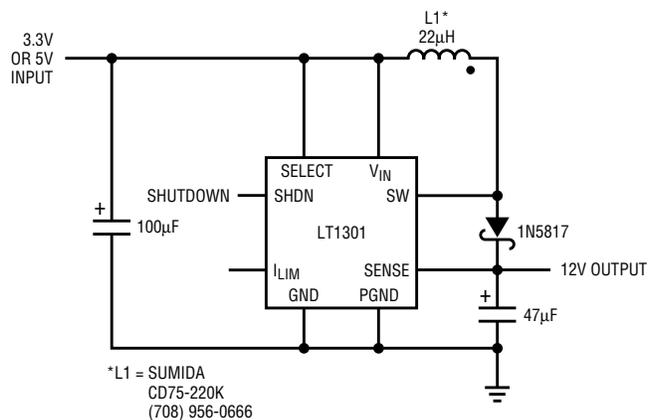


Figure 13. LT1301 Delivers 12V from 3.3V or 5V input

LT1301 Outputs Five or Twelve Volts

The LT1301 is identical to the LT1300 in every way except output voltage. The LT1301 can be set to a 5V or 12V output via its SELECT pin. Figure 13 shows a simple 3.3V or 5V to 12V step-up converter. It can generate 120mA at 12V from either 3.3V or 5V inputs, enabling the circuit to provide V_{PP} on a PCMCIA card socket. Figure 14 shows the circuit's efficiency. Switch voltage drop is a smaller percentage of input voltage at 5V than at 3.3V, resulting in the higher efficiency at 5V input.

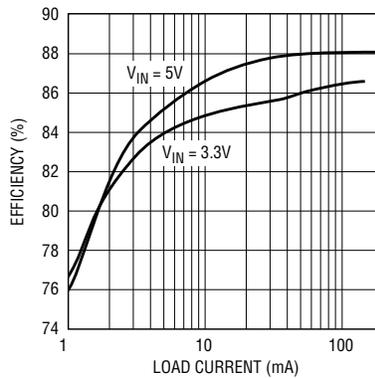


Figure 14. Efficiency of Figure 13's circuit

Conclusion

The new LT1300 and LT1301 are full-function, micropower step-up DC/DC converters optimized for battery-powered operation. The converters have been optimized for a complete surface mount solution with high efficiency, low quiescent current, and a low parts count.

LTC1257, continued from page 4

When the LTC1296 receives a shutdown command, the SSO pin of the ADC goes high, the PNP turns off, and the system shuts off.

Figure 5 shows how an LT1021-10 can be used to override the LTC1257's internal reference. The supply voltage for both the reference and the DAC is set to 15V, and the full-scale voltage for the DAC becomes 10V.

The circuit in Figure 6 is a 12-bit, single 5V-supply temperature-control system with shutdown. An external temperature is monitored by a J-type

thermocouple. The LT1025A provides the cold junction compensation for the thermocouple and the LTC1050 chopper op amp provides signal gain. The 47k Ω , 1 μ F capacitor filters the chopping noise before the signal is sent to the A/D converter. The LTC1297 A/D converter uses the reference of the LTC1257 after it has been filtered to set full scale. After the A/D measurement is taken, \overline{CS} is pulled high and everything except the LTC1257 is powered down, reducing the system supply current to about 350 μ A. A word can

then be written to the LTC1257 and its output can be used to as a temperature-control signal for the system being monitored.

Conclusion

The LTC1257 is one of the smallest, easiest-to-use 12-bit DACs available today. With its cascadable 3-wire serial interface, built-in reference and voltage buffer, single supply operation, low supply current, and small package size, the chip is a natural choice to reduce system complexity and cost.

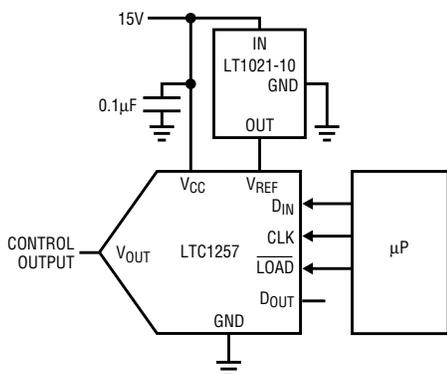


Figure 5. DAC with external reference

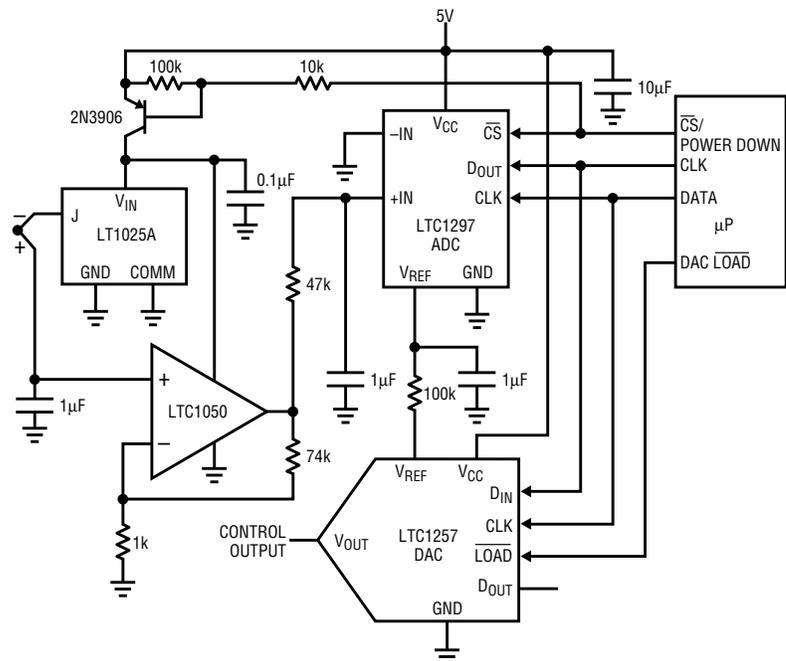


Figure 6. 12-bit single 5V control system with shutdown

LT1204, continued from page 7

Switchable Gain Amplifier

An example of the flexibility of the LT1204 can be seen in a switchable gain amplifier (Figure 7), which can use either the shutdown or disable feature. This circuit maintains a relatively constant output voltage of 1VPP \pm 330mV over a 128-to-1 change in input level. When LT1204 #1 is selected, an input attenuator alters the

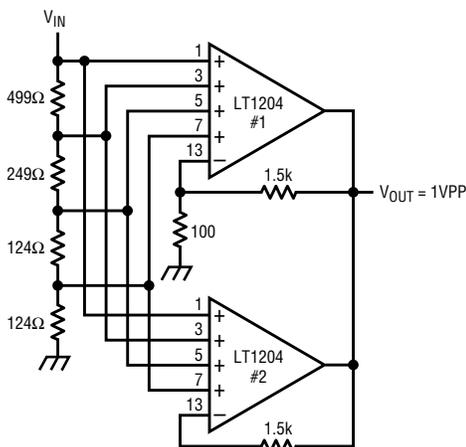


Figure 7. Switchable Gain amplifier
 $A_V = 1, 2, 4, 8$

input signal by 1, 0.5, 0.25, or 0.125 to form an amplifier with a gain of 16, 8, 4, or 2. LT1204 #2 is connected to the same attenuator, and when it is enabled (LT1204 #1 disabled), it has a gain of +1 instead of +16. The second LT1204 is used to extend the gain range to 1, 0.5, 0.25, and 0.125.

Performance

Table 2 summarizes the major performance specifications of the LT1204.

Table 2. LT1204 Performance

Parameter	Conditions	Typical Value
Bandwidth	$A_V = +2, R_L = 150\Omega$	70MHz
0.1dB gain flatness	$A_V = +2, R_L = 150\Omega$, no peaking	>30MHz
Slew rate	$A_V = +10$	1000V/ μ s
Differential gain	$A_V = +2, R_L = 150\Omega$, NTSC	0.04%
Differential phase	$A_V = +2, R_L = 150\Omega$, NTSC	0.06°
Channel select time	$A_V = +10, V_{IN} = 0.5V$	120ns
Enable time	$A_V = +10, V_{IN} = 0.5V$	100ns
Disable time	$A_V = +10, V_{IN} = 0.5V$	50ns
Input voltage range	Pin 8 = 0V, $V_S \geq \pm 10V$	$\pm 6V$
Input offset voltage		5mV
Output swing	$R_L = 400\Omega$	13.5V
Supply current		19mA
Supply current in shutdown	Pin 12 = 0V	1.5mA
Output limit current		55mA

Conclusions

The LT1204 combines a fast-switching multiplexer with a high-speed current-feedback amplifier for gain adjustment and cable driving. Switching transients have been greatly reduced in amplitude and duration, all hostile and disable crosstalk have been reduced below -90dB at 10MHz, and the unique disable feature eases system expansion. The high performance of this multiplexer makes it ideal for the newest multimedia products. \blacktriangleleft

LT1363, continued from page 11

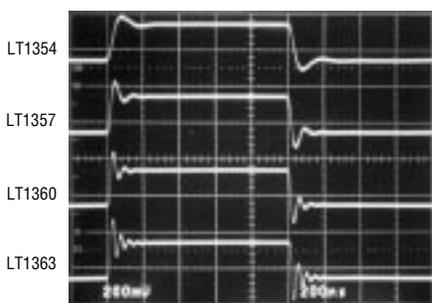


Figure 4. Small signal step response, $C_{Load} = 200pF$:
 LT1354, LT1357, LT1360, LT1363

ensuring stability. Figure 4 shows the family of amplifiers driving a 200pF load and Figure 5 shows the large signal response with a 10,000pF load. Note that the slew rate when driving a large capacitive load is limited by the short-circuit current limit of the amplifier.

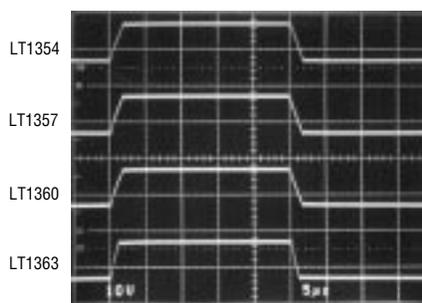


Figure 5. Large signal step response, $C_{Load} = 10,000pF$:
 LT1354, LT1357, LT1360, LT1363

Conclusion

The new topology offers significant improvement in circuit performance. It achieves higher slew rates with lower supply currents and improves DC specifications and noise with higher input-stage transconductance, lower

operating currents, and balanced input stages. The family of parts is also stable with capacitive loads and can be used in any voltage feedback application. \blacktriangleleft

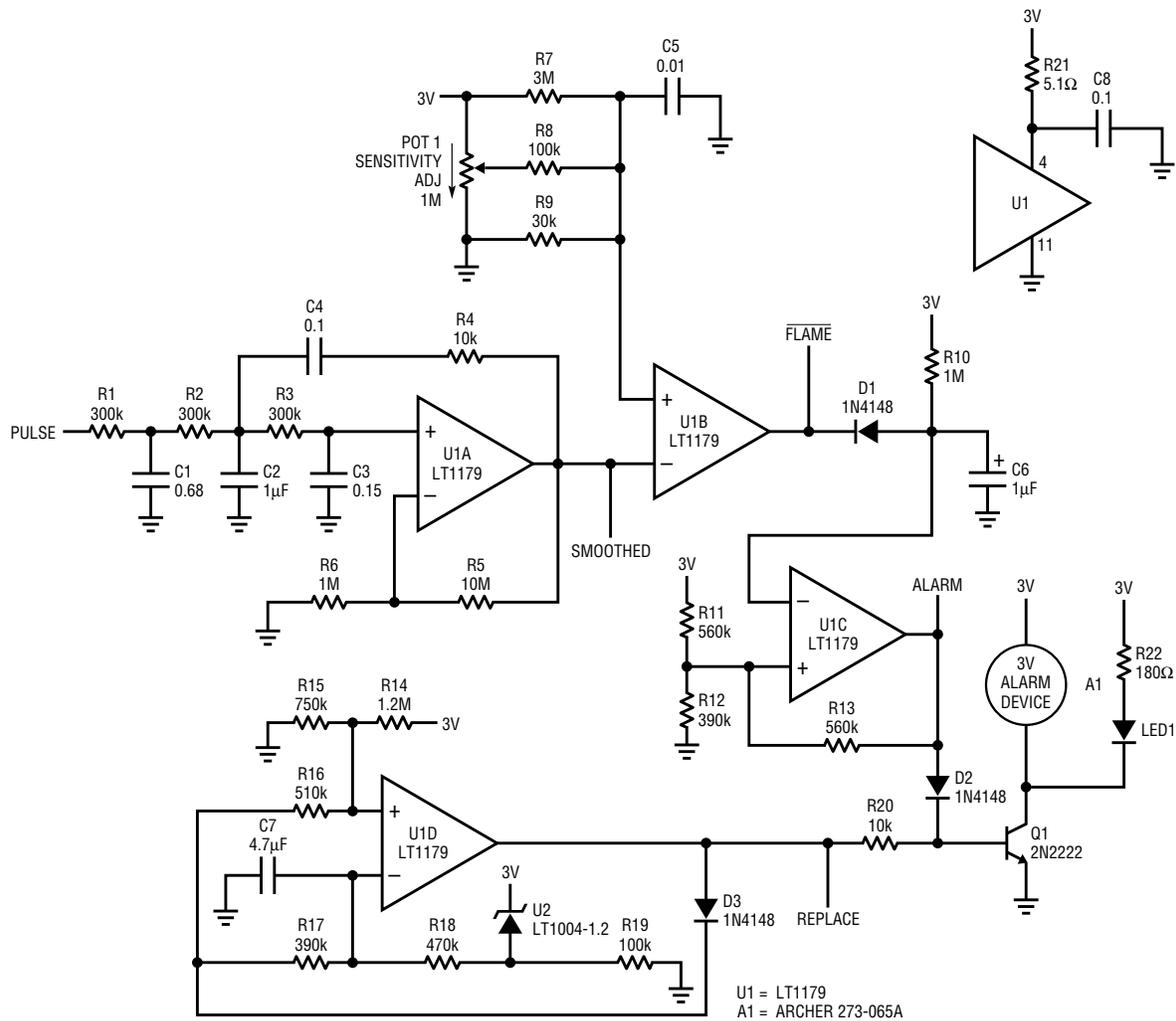


Figure 3. Discriminator circuitry

feedback loop comprised of D3, R2, and Q1 kicks in and charges C4 through D4. When the voltage at C4 exceeds 3.3V, the LT1300 goes into its wait mode. In wait mode the LT1300 consumes only 100μA of current. The LT1300 stays in wait mode until the voltage on C4 falls below 3.3V, at which time the LT1300 turns on to burst recharge both C1 and C4. Burst Mode™ operation ensures 30Hz oscillation in this system. This rate is determined by the value of C4, the internal sense resistance to ground in the LT1300 (approximately 1 MΩ), and the amount of overcharge C4 gets when charging.) D5 is a Schottky catch diode to keep reverse current out of U1.

When illuminated with a photon of sufficient energy, the photoelectric tube's cathode liberates an electron.

The tube V1 has 325V across its terminals to get sufficient energy into a liberated photo electron to ionize the gas that fills the tube. Once the gas in the tube ionizes, there are more electrons available; they cause a chain reaction in the tube that causes the tube to avalanche. When the tube avalanches, most of the charge on C1 is transferred to C2 and the voltage across C1 drops to a fraction of its original 325V. When C2 has charged to 3.6V, all the excess charge residing in C1 gets dumped through D2 into the battery. The voltage across C2 is the output signal called PULSE. PULSE asserts the shutdown pin of the LT1300, allowing the plasma in the photoelectric tube to quench. Figure 2 shows an interface circuit that enables the PULSE signal to interrupt a microprocessor.

For you analog purists, Figure 3 shows a discriminator circuit with low battery detect for a complete 3V flame alarm. The discriminator is needed because the photo detector occasionally detects a cosmic ray or some rare room-light photon. The discriminator consists of four sections.

Filter Section (U1a, R1-R6, C1-C4)

In this section, the PULSE signal is filtered with a third-order Gaussian lowpass filter. Each PULSE is converted into a Gaussian-shaped pulse about 300ms wide. These Gaussian-shaped pulses are superimposed and can be seen on the SMOOTHED test point. The net effect of this filtering is to accumulate PULSES that are close together (<300ms) into a single DC

voltage. When the input PULSE happens frequently, the SMOOTHED test point goes positive, indicating many recently detected photons.

Threshold-Setting Section (U1b, POT1, R1-R9, C5)

POT1 sets the threshold of the alarm; U1b compares the threshold with the SMOOTHED signal from the previous section and pulls its output low when it detects more voltage on SMOOTHED than on the threshold. This output is the test point labelled FLAME.

Pulse-Stretcher Section: (D1, R10-R13, C6, U1c)

When FLAME goes low, C6 discharges through D1 and is slowly recharged through R10. U1c is a comparator with hysteresis that outputs a high signal (test point ALARM) when FLAME goes low. Because of the time constant of R10 and C6, ALARM stays high for about one second after FLAME goes high. The ALARM output also drives the base of Q1 through D2 to sound the sounding device A1.

Low-Battery-Detect Circuit (R14-R19, C7, D3, U1d)

This sub-circuit is a divider/comparator/oscillator that is activated when the battery voltage drops to 2V. The output is a positive-going 1/4-second signal called REPLACE. REPLACE initially occurs every three seconds at a battery voltage of 2V, but the frequency of repetition increases as the battery voltage drops. At a battery voltage of 1.5V, the REPLACE signal frequency is approximately 2Hz. REPLACE also sounds the sounding device A1 through R20 and Q1. R21 and C8 form a trash compactor to decouple U1.

The complete circuit, including the detector (Figure 1) and the discriminator (Figure 3) consume a mere 300µA of supply current from 3V. The circuit lends itself very well to both battery operation and two-wire remote operation. Battery life is more than two years when powered by two C-size alkaline cells. In full sun, the

detector can easily “see” a cigarette lighter 30 feet away and still discriminate it from the sun.

Infinite-Input-Impedance Voltage Buffer

In the flame detector circuit (Figure 1), it is difficult to measure the voltage across C1 because almost any load invalidates the meter reading. This next application for the LT1300 is a voltage buffer that overcomes this measurement problem. This is a four-terminal, unity-gain buffer, as shown functionally in Figure 4. The input impedance is essentially infinite, the input bias current is negligible,

and the input offset voltage is less than 0.05 volts. The output voltage tracks the input voltage from 0V to 520V. For safety (and to isolate the input capacitance) a 100MΩ resistor is placed in series with the input, but with the ±570pA of input bias current (over temperature) for the LT1097, this translates into only ±57mV of additional offset. The input impedance of this buffer measures four trillion ohms when measured with a 100-to-400 volt input. The detailed circuit is shown in Figure 5.

Theory of Operation

U1 monitors the voltage difference between the circuit’s noninverting input and output and attempts to make it zero. If the voltage on the noninverting input is less than the voltage on the noninverting output, U1’s output goes positive, turning Q1 on slightly. Q1 acts as a current source, discharging C3. When the

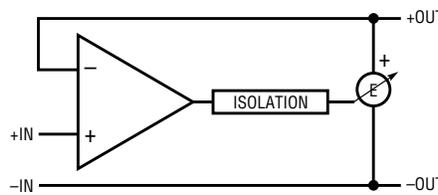
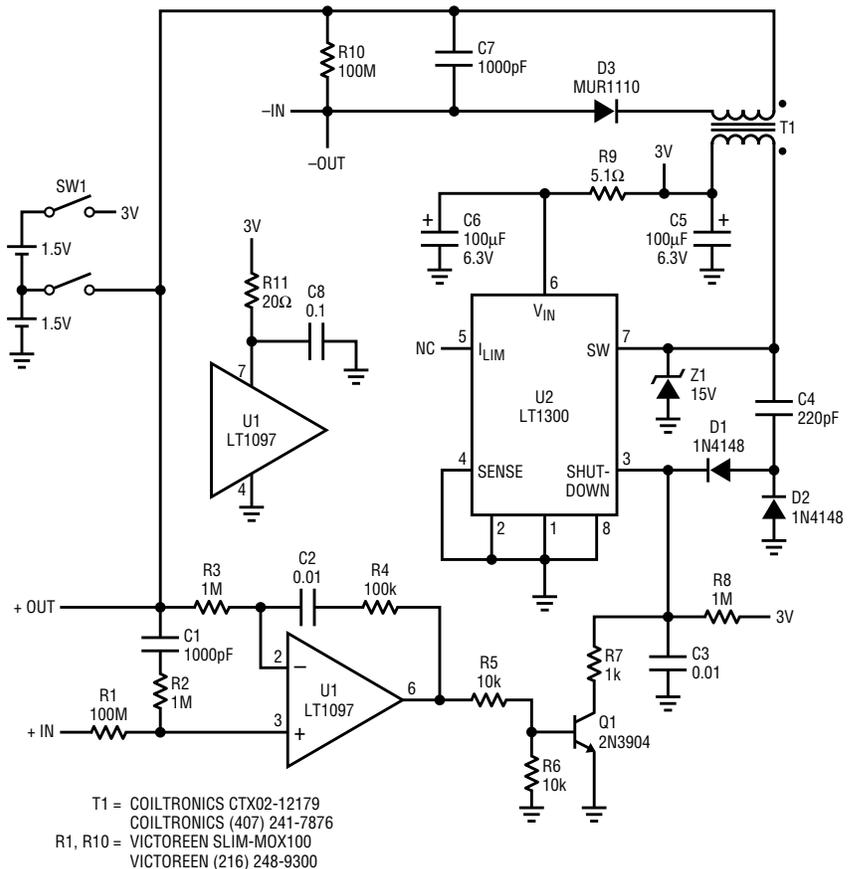


Figure 4. Voltage buffer block diagram



- T1 = COILTRONICS CTX02-12179
- COILTRONICS (407) 241-7876
- R1, R10 = VICTOREEN SLIM-MOX100
- VICTOREEN (216) 248-9300

Figure 5. Voltage buffer schematic

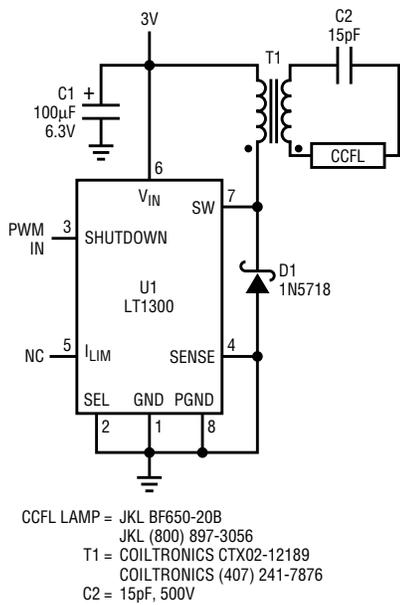


Figure 6. CCFL driver

voltage on C3 falls below approximately 0.6V, U2 is enabled. When it is enabled, U2 turns its switch on (U2 pin 7 pulls low, to near 0V). This causes approximately 3V to be imposed across the primary winding of T1. The magnetizing inductance of the primary winding of T1, across which a voltage is applied, requires a steadily increasing current. At the same time, C4 is charging through D2. When the current flowing through the switch of the LT1300 reaches 1 amp, the LT1300 switches off. The magnetizing inductance of the primary winding of T1, seeing that the LT1300 is attempting to discontinue current flow, takes over by swinging positive in voltage until it finds something that will take the 1 amp of magnetizing current. While the primary winding is finding somewhere to put the magnetizing current, the secondary winding takes it upon itself to do the same, but due to its turns ratio with the primary winding, it moves 100 times faster and 100 times as far as the primary winding. T1's secondary dumps a significant portion of the magnetizing energy into C7 via D3, thus forming a flyback inverter.

Z1 dissipates the energy stored in T1's inductance. During the flyback time, C4 charges C3 through D1. The voltage across C3 exceeds 0.6V, shutting down U2. U2 stays shut down until Q1 discharges C3 to restart the sequence.

When the +output voltage is more positive than the +input voltage, the output of U1 goes low, Q1 stays off, R8 keeps C3 charged to more than 0.6V, and U2 stays shut down. The parallel combination of R10 and the load resistance (e.g., 10MΩ in a handheld voltmeter) discharges C7 and the +output and the +input voltages are again equal. The current output of this circuit is limited to a safe value (1mA at 50V, 0.1mA at 500V), even when the +input is attached to +500V. We do not recommend increasing the value of C7, because at higher voltages it may become a shock hazard. Battery life 40 hours for a pair of AA alkaline batteries driving 10MΩ at 500V.

Cold-Cathode Florescent Lamp Driver

CCFLs seem to be the latest craze; they offer high brightness, long life, small size, and produce white light. Figure 6 shows a CCFL driver circuit.

Theory of Operation

This is a forward/flyback inverter optimized for minimum parts count. When enabled, U1 charges the primary winding of T1 to 1 amp, and lets go. T1 then flies back, exciting many hundreds of volts across its secondary winding, which, in turn, ionizes the CCFL. Because the initial current through the CCFL is only in one direction, C2 takes on a DC potential. As the circuit runs, the voltage across C2 stabilizes at about 100VDC. Additionally, C2 removes the DC component from the tube current, extending tube life. The nonlinear V/I characteristic of the CCFL, in conjunction with C2, forces the converter to run in both forward and flyback modes simultaneously. The light intensity can be pulse-width modulated

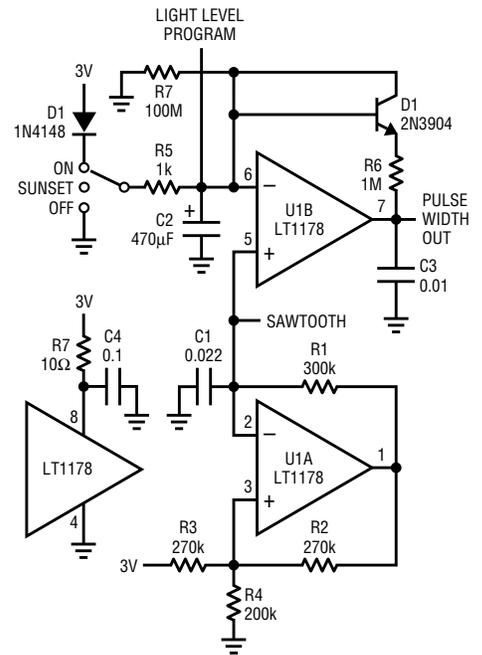


Figure 7. Electronic light stick controller

by modulating the shutdown pin. When the shutdown pin is pulled high, the LT1300 goes into its shutdown mode, where it draws only 10µA of input current.

Electronic Light Stick

Camping in November with my kids has its own unique problems, even if we aren't camping in six feet of snow. Although we had the usual light sources, something was missing, namely a light that simulates the natural sunset at bedtime to wind the kids down for the night. The circuit in Figures 6 and 7 (see explanation below) details a high efficiency fluorescent lantern with a built in sunset feature.

The function of the circuit is as follows:

- To turn on: switch SW1 into the ON position.
- To turn off fast: switch SW1 into the OFF position.
- To simulate sunset: 1. turn light ON. 2. switch SW1 into the SUNSET position.

This application uses the circuitry of both Figure 6 and Figure 7. The pulse-width output of Figure 7 drives the pulse-width input of Figure 6.

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Using a Fast Analog Multiplexer to Switch Video Signals for NTSC “Picture-in-Picture” Displays

by Frank Cox

Introduction

The majority of production¹ video switching consists of selecting one video source out of many for signal routing or scene editing. For these purposes, the video signal is switched during the vertical interval in order to reduce visual switching transients. The image is blanked during this time, so if the horizontal and vertical synchronization and subcarrier lock are maintained, there will be no visible artifacts. Although vertical-interval switching is adequate for most routing functions, there are times when it is desirable to switch two synchronous video signals during the active (visible) portion of the line to obtain picture-in-picture, key, or overlay effects. Picture-in-picture or active video switching requires signal-to-signal transitions that are both clean and fast. A clean transition should have a minimum of pre-shoot, over-shoot, ringing, or other aberrations commonly lumped under the term “glitching.”

Using the LT1204

A quality, high-speed multiplexer amplifier can be used with good

results for active video switching. The important specifications for this application are small, controlled switching glitch, good switching speed, low distortion, good dynamic range, wide bandwidth, low path loss, low channel-to-channel crosstalk, and good channel-to-channel offset matching. The LT1204 specifications match these requirements quite well, especially in the areas of bandwidth, distortion, and channel-to-channel crosstalk (which is an outstanding 90dB at 10MHz). The LT1204 was evaluated for use in active video switching with the test setup shown in Figure 1. Figure 2 shows the video waveform of a switch between a 50% white level and a 0% white level about 30% into the active interval and back again at about 60% of the active interval. The switch artifact is brief and well controlled. Figure 3 is an expanded view of the same waveform. When viewed on a monitor, the switch artifact is just visible as a very fine line. The lower trace is a switch between two black level (0V) video signals showing a very slight channel-to-channel offset, which is not visible on

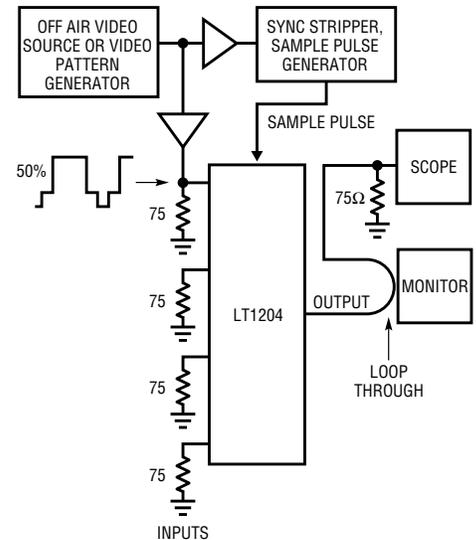


Figure 1. “Picture-in-picture” test setup

the monitor. Switching between two DC levels is a worst-case test, as almost any active video will have enough variation to totally obscure this small switch artifact.

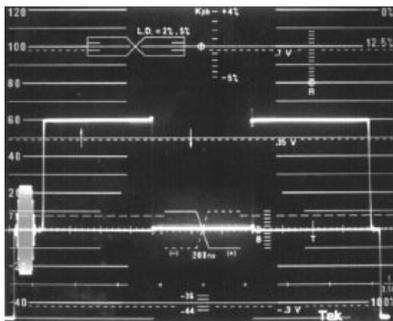


Figure 2. Video waveform switched from 50% white level to 0% white level and back

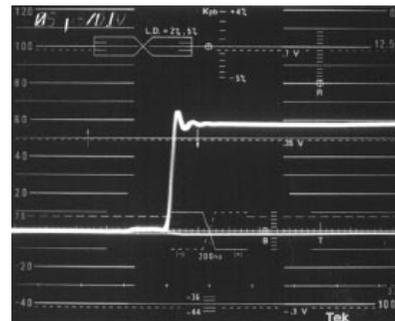


Figure 3. Expanded view of rising edge of LT1204 switching from 0% to 50% (50ns horizontal division)

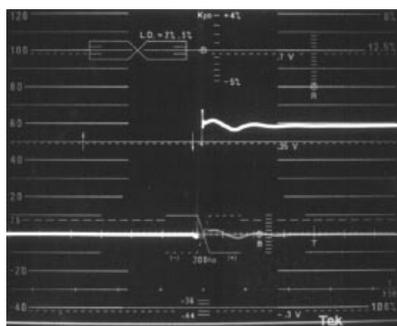


Figure 4. Expanded view of "brand-x" switch 0%-50% transition

Video-Switching Caveats

In a video processing system that has a large bandwidth compared to the bandwidth of the video signal, a fast transition from one video level to another (with a low-amplitude glitch) will cause minimal visual disturbance. This situation is analogous to the proper use of an analog oscilloscope. In order to make accurate measurement of pulse waveforms, the instrument must have much more bandwidth than the signal in question (usually five times the highest frequency). Not only should the glitch be small, it should be otherwise well controlled. A switching glitch that has a long settling "tail" can be more

troublesome (that is, more visible) than one that has more amplitude but decays quickly. The LT1204 has a switching glitch that is not only low in amplitude but well controlled and quickly damped. Refer to Figure 4, which shows a video multiplexer that has a long, slow-settling tail. This sort of distortion is highly visible on a video monitor.

Composite video systems, such as NTSC, are inherently band-limited and thus edge-rate limited. In a sharply band-limited system, the introduction of signals that contain significant energy higher in frequency than the filter cutoff will cause distortion of transient waveforms (see Figure 5). Filters used to control the bandwidth of these video systems should be group-delay equalized to minimize this pulse distortion. Additionally, in a band-limited system, the edge rates of switching glitches or level-to-level transitions should be controlled to prevent ringing and other pulse aberrations that could be visible. In practice, this is usually accomplished with pulse-shaping networks (Bessel filters are one example). Pulse-shaping networks and delay-equalized filters add cost and complexity to video systems and are usually found

continued on page 29

Some Definitions—

"Picture in picture" refers to the production effect in which one video image is inserted within the boundaries of another. The process may be as simple as splitting the screen down the middle or it may involve switching the two images along a complicated geometric boundary. In order to make the composite picture stable and viewable, both video signals must be in horizontal and vertical sync. For composite color signals, the signals must also be in subcarrier lock.

"Keying" is the process of switching among of two or more video signals, triggering on some characteristic of one of the signals. For instance, a chroma keyer will switch on the presence of a particular color. Chroma keyers are used to insert a portion of one scene into another. In a commonly used effect, the TV weather person (the "talent") appears to be standing in front of a computer generated weather map. Actually, the talent is standing in front of a specially colored background; the weather map is a separate video signal, which has been carefully prepared to contain none of that particular color. When the chroma keyer senses the keying color, it switches to the weather map background. Where there is no keying color, the keyer switches to the talent's image.

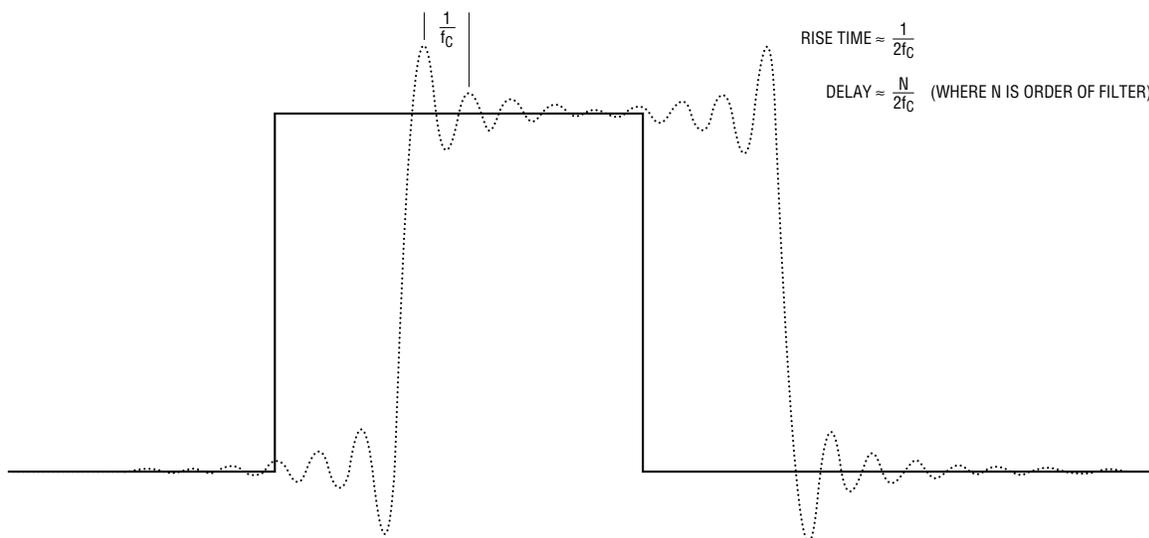


Figure 5. Pulse response of an ideal sharp-cutoff filter at frequency f_c

High-Efficiency (>90%) NiCad Battery-Charger Circuit Programmable for 1.3A Fast Charge or 100mA Trickle Charge

by Brian Huffman

Battery-charger circuits are of universal interest to laptop, notebook, and palmtop computer manufacturers. High efficiency is desirable in these applications to minimize the power dissipated in the surface mount components. The circuit shown in Figure 1 is designed to charge four NiCad cells at a 1.3A fast charge or a 100mA trickle charge, with efficiency exceeding 90%. This circuit can be modified easily to handle up to eight NiCad cells.

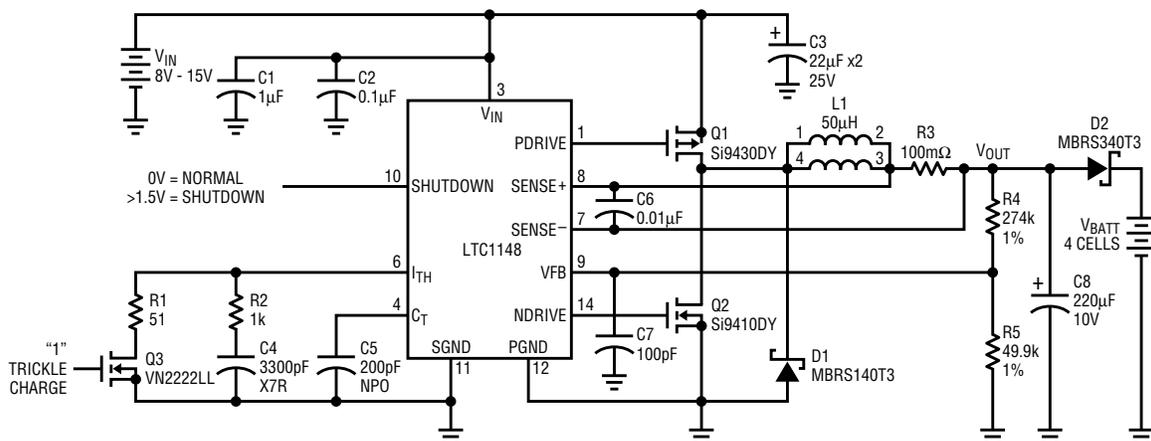
The circuit uses an LTC1148 in a step-down configuration to control the charge rate. The LTC1148 is a synchronous switching-regulator controller that drives external, complementary power MOSFETs using a constant off-time current mode architecture. When the LTC1148's P-drive output pulls the gate of Q1

low, the P-channel MOSFET turns on and connects one side of the inductor to the input voltage. During this period, current flows from the input through Q1, through the inductor, and into the battery. When the LTC1148 P-drive pin goes high, Q1 is turned off, and the voltage on the drain of Q1 drops until the clamp diode is forward biased. The diode conducts for a very short period of time, until the LTC1148 internal circuitry senses that the P-channel is fully off, preventing the simultaneous conduction of Q1 and Q2. Then the N-drive output goes high, turning on Q2, which shorts out D1. Now the inductor current flows through the N-channel MOSFET instead of through the diode, increasing efficiency. This type of switching architecture is known as synchronous rectification.

During the fast-charge interval, the resistor divider network (R4 and R5) forces the LTC1148's feedback pin (VFB) below 1.25V, causing the LTC1148 to operate at the maximum output current. R3, a 100mΩ resistor, senses the current and sets it at approximately 1.3A, according to equation 1. When the batteries are disconnected, the error amplifier forces the feedback pin to 1.25V, limiting the output voltage to 8.1V. Diode D2 prevents the batteries from discharging through the divider network when the charger is shut down. In shutdown mode, the circuit draws less than 20μA from the input supply.

The dual-rate charging is controlled by Q3, which can be toggled between fast charge and trickle charge. The trickle-charge rate is set by resistor R1. Figure 2 is a graph showing the

continued on page 24



- C1 = (TA)
- C3 = AVX (TA) TPSD226K025R0200 ESR = 0.200 IRMS = 0.775A
- C8 = AVX (TA) TPSE227M010R0100 ESR = 0.100 IRMS = 1.149A
- Q1 = SILICONIX PMOS BVDSS = 20V RDS_ON = 0.125 C_RSS = 400pF Q_G = 25nC θ_JA = 50°C/W
- Q2 = SILICONIX NMOS BVDSS = 30V RDS_ON = 0.050 C_RSS = 160pF Q_G = 50nC θ_JA = 50°C/W
- D1, D2 = MOTOROLA SCHOTTKY VBR = 40V
- R3 = KRL SP-1/2-A1-OR100J Pd = 0.75V
- L1 = COILTRONICS CTX50-4 DCR = 0.175 IDC = 1.350A KOOL Mμ CORE

$$V_{OUT} = 1.25V \cdot (1 + R4/R5) = 8.1V$$

$$\text{FAST CHARGE} = 130mV/R3 = 1.3A \text{ (EQ. 1)}$$

$$\text{TRICKLE CHARGE} = 100mA \text{ (SEE FIGURE 2)}$$

ALL OTHER CAPACITORS ARE CERAMIC

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Figure 1. Schematic diagram: 4 cell, 1.3 amp battery charger implemented in surface mount technology

An LT1087-Based 1.2V GTL Terminator

by Mitchell Lee

A recent development in high-speed digital design has resulted in a new family of logic chips called Gunning Transition Logic (GTL). Because of the speeds involved, careful attention must be paid to the transmission-line characteristics of the interconnections between these chips; active termination is required.

The termination voltage is 1.20V, and currents of several amperes are common in a complete system. One method of generating 1.2V is to use a linear regulator operating from 3.3V or 5V. Unfortunately, this method suffers from two major drawbacks. First, the minimum adjust voltage,

without the aid of a negative supply, is 1.25V for most adjustable linear regulators. Second, most low-voltage linear regulators do not feature low dropout characteristics, rendering them unusable on a 3.3V input. The LT1087 solves both of these problems with an output that can be adjusted to less than the reference voltage and a low-dropout architecture.

Figure 1 shows the complete circuit. The LT1087 features feedback sense, which, in its original application, was used for remote Kelvin sensing. In the GTL terminator circuit, the sense pins are used to adjust the internal 1.25V reference downward.

The result is a 1.20V, 5A regulator, with 2% output tolerance over all conditions of line, load, and temperature. To minimize power dissipation, a 3.3V input source is recommended.

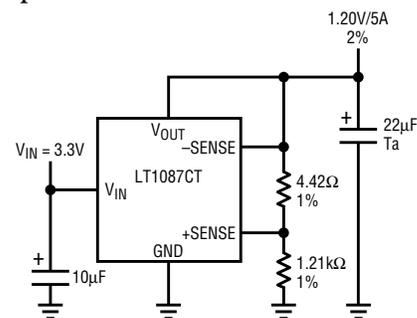


Figure 1. Schematic diagram: 1.2 volt GTL termination voltage generator

NiCad, continued from page 23

value of R1 for a given trickle-charge output current. The trickle-charge current can also be varied by using an op amp to force the threshold pin voltage within its 0V–2V range. Figure 3 shows the output current as a function of threshold pin voltage.

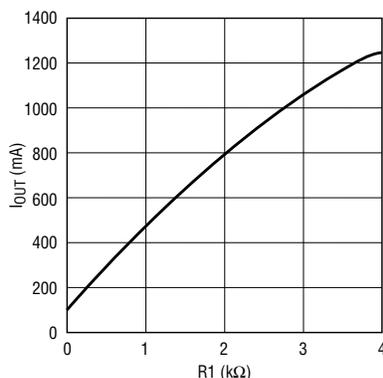


Figure 2. LTC1148 output current versus trickle charge set resistance (R1)

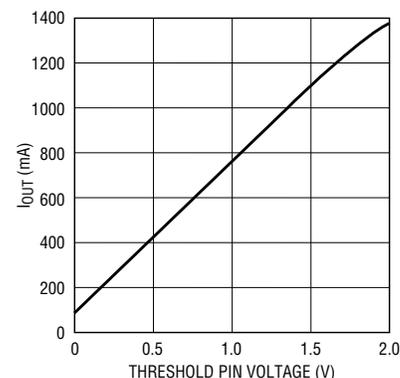


Figure 3. LTC1148 output current versus forced threshold pin voltage

LT1300, continued from page 20

Theory of Operation

U1a, R1–R4, and C1 form a sawtooth oscillator for pulse-width modulating the light (implementing light levels less than 100%). U1b acts as a comparator, comparing the sawtooth output of the oscillator with the programmed light level (as seen on the + terminal of C2). C2 is the holding cap that programs the light level; when it is charged to 2.5V, the light is on 100% of the time. As the voltage on C2 drops below 2.5V, the overall light level decreases, because the light is being pulse-width modulated. When the voltage on C2

is at or below 1 volt, the light is off. D1 and R5 charge and hold C2 when SW1 is in the ON position. R5 and SW1 discharge and hold C2 when SW1 is in the OFF position. The combination of D2, R6, and U1b discharge C2 when SW1 is in the SUNSET position. The discharging of C2 when in the SUNSET mode is doubly exponential, causing the tail end of the simulated sunset to go very slowly (a good idea, because kids have a logarithmic response to light). The first exponential aspect of the SUNSET decay is implemented by R6 and C2,

which form an exponential RC time constant. The second exponential aspect of the SUNSET decay is implemented because R6 is driven by U1b pin 7, whose duty factor is changing, causing the off time to decrease exponentially as the light level fades. The output of U1b is a pulse-width-modulated level gating the light driver on and off. The lamp is illuminated when U1b's output is low. C3 is a trash compactor and R7 and C4 form a trash compactor to decouple U1 from the high-frequency ripple generated by the switcher.

LTC1163: 2-Cell Power Management

by Tim Skovmand

The LTC1163 1.8V to 6V high-side MOSFET driver allows inexpensive N-channel switches to be used to efficiently manage power in 2-cell systems such as palmtop computers, portable medical equipment, cellular telephones and personal organizers.

Any supply voltage above 3V, such as: 3.3V, 5V or 12V, can be generated by step-up converters powered from a 2-cell supply. Step-up regulators are typically configured as shown in Figure 1. An inductor is connected

directly to the 2-cell battery pack and switched by a large (1A) switch. The inductor current is then passed through a low-drop Schottky rectifier to charge the output capacitor to a voltage higher than the input voltage. Unfortunately, when the regulator is shut down, the inductor and diode remain connected and the load may leak significant current in standby.

One possible solution to this problem is to add a low $R_{DS(ON)}$ MOSFET switch between the battery pack and

the input of the regulator to completely disconnect it and the load from the battery pack. MOSFET switches, however, cannot operate directly from 2-cell battery supplies because the gate voltage is limited to 3V with fresh cells and 1.8V when the cells are fully discharged.

The LTC1163 solves this problem by generating gate drive voltages which fully enhance high-side N-channel switches when powered from a 2-cell battery pack as shown in Figure 2. The standby current with all three drivers switched off is typically 0.01 μ A. The quiescent current rises to 85 μ A per channel with the input turned on and the charge pump producing 10V (above ground) from a 3V supply. The surface mount MOSFET switches shown are guaranteed to be less than 0.1 Ω with $V_{GS} = 5V$ and less than 0.12 Ω with $V_{GS} = 4V$ and therefore have extremely low voltage drops. \blacktriangle

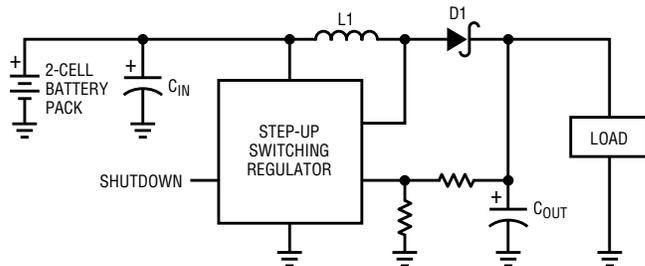


Figure 1. Typical step-up converter topology

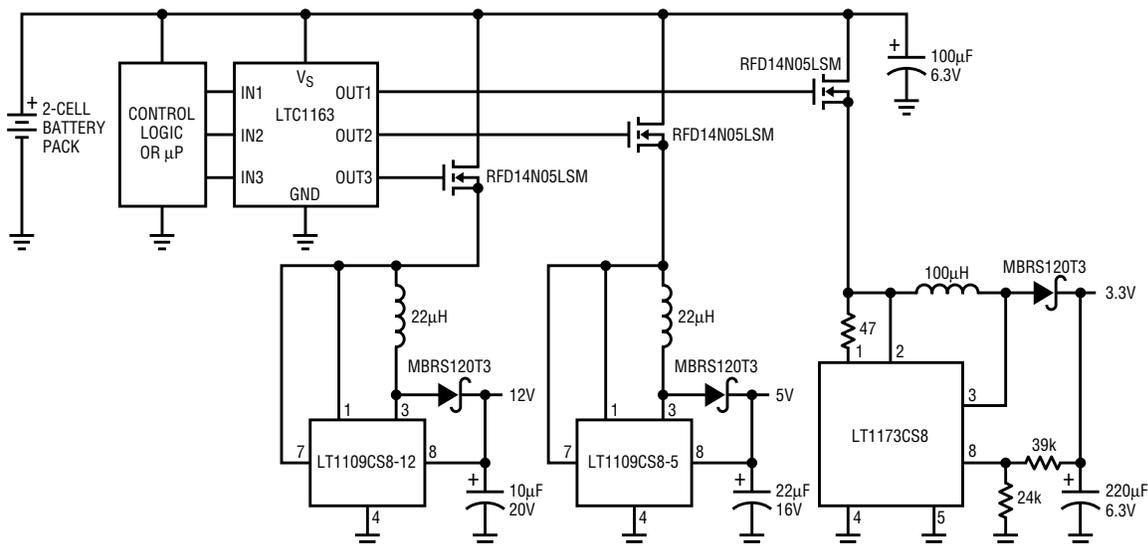


Figure 2 Complete 2-cell to 3.3V, 5V, and 12V power management system

A High-Efficiency, 5V to 3.3V/5A Converter

by Randy G. Flatness

The next generation of notebook and desktop computers is incorporating more 3.3V ICs alongside 5V devices. As the number of devices increases, the current requirements also increase. Typically, a high-current 5V supply is already available. Thus, the problem is reduced to deriving 3.3V from 5V efficiently in a small amount of board space.

High efficiency is mandatory in these applications, since converting 5V to 3.3V at 5A using a linear regulator would require dissipating over 8W. This wastes power and board space for heat sinking.

The LTC1148 synchronous switching-regulator controller accomplishes the 5V to 3.3V conversion with high efficiencies over a wide load-current range. The circuit shown in Figure 1 provides 3.3V at efficiencies greater than 90% from 5mA to 5A (over three decades of load current). The

efficiency of the circuit in Figure 1 is plotted in Figure 2.

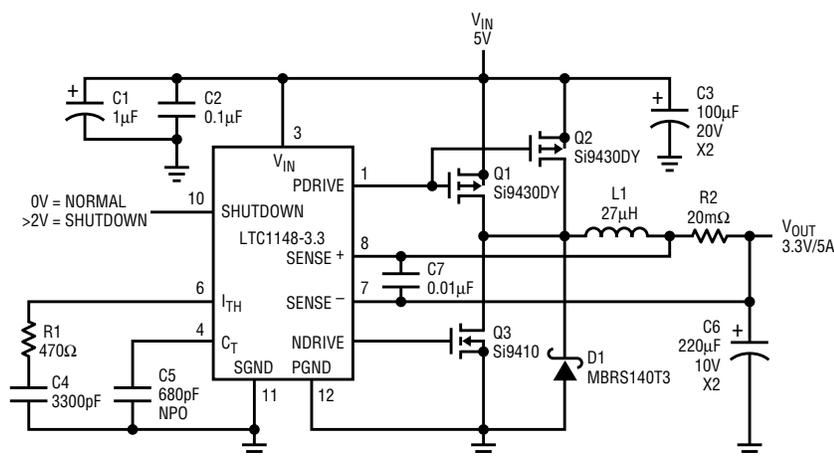
At an output current of 5A the efficiency is 90%; this means only 1.8W are lost. This lost power is distributed among R_{SENSE} , L1, and the power MOSFETs; thus heat sinking is not required.

The LTC1148 series of controllers use constant off-time current-mode architecture to provide clean start-up, accurate current limit, and excellent line and load regulation. To maximize the operating efficiency at low output currents, Burst Mode™ operation is used to reduce switching losses. Synchronous switching, combined with Burst Mode™ operation, yields very efficient energy conversion over a wide range of load currents.

The top P-channel MOSFETs in Figure 1 will be on 2/3 of the time with an input of 5V. Hence, these devices should be carefully examined

to obtain the best performance. Two MOSFETs are needed to handle the peak currents safely and enhance high-current efficiency. The LTC1148 can drive both MOSFETs adequately without a problem. A single N-channel MOSFET is used as the bottom synchronous switch, which shunts the Schottky diode. Finally, adaptive anti-shoot-through circuitry automatically prevents cross conduction between the complementary MOSFETs, which can kill efficiency.

The circuit in Figure 1 has a no-load current of only 160µA. In shutdown mode, with pin 10 held high (above 2V), the quiescent current reduces to less than 20µA with all MOSFETs held off DC. Although the circuit in Figure 1 is specified at a +5V input voltage, the circuit will function from 4V to 15V without requiring any component substitutions. ◀



- C1 = TANTALUM
- C3 = SANYO (OS-CON) 20SA100M ESR = 0.037Ω I_{RMS} = 2.25A
- C6 = AVX (TA) TPSE227K01R0080 ESR = 0.080Ω I_{RMS} = 1.285A
- Q1, Q2 = SILICONIX PMOS BV_{DSS} = 20V DCR_{ON} = 0.100Ω Q_g = 50nC
- Q3 = SILICONIX NMOS BV_{DSS} = 30V DCR_{ON} = 0.050Ω Q_g = 30nC
- D1 = MOTOROLA SCHOTTKY VBR = 30V
- R2 = KRL NP-2A-C1-0R020J Pd = 3W
- L1 = KOOL Mµ CORE, 16 GAUGE

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Figure 1. LTC1148-3.3 high-efficiency 5V to 3.3V/5A step-down converter

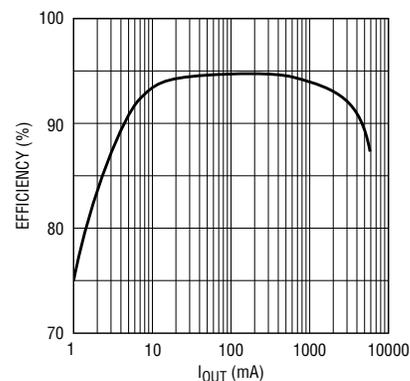


Figure 2. Efficiency for 5V to 3.3V synchronous switcher

A Dual-Output LCD-Bias Voltage Generator

by Jon A. Dutra

With the many different kinds of LCD displays available, systems manufacturers often want the option of deciding the polarity of the LCD-bias voltage at the time of manufacturing.

The circuit in Figure 1 uses the LT1107 micropower DC-to-DC converter with a single inductor. The LT1107 features an I_{LIM} pin that enables direct control of maximum inductor current. This allows the use of a smaller inductor without the risk of saturation. The LT1111 could also be used, with a resulting reduction in output power.

Circuit Operation

The circuit is basically an AC-coupled boost topology. The feedback signal is derived separately from the outputs, so loading of the outputs does not affect loop compensation. Since there is no direct feedback from the outputs, load regulation performance is reduced. With 28 volts out, from 10% to 100% load (4mA to 40mA), the output voltage sags by

about 0.65 volts. From 1mA to 40mA load, the output voltage sags by about 1.4 volts. This is acceptable for most displays.

Output noise is reduced by using the auxiliary gain block (AGB) in the feedback path. This added gain effectively reduces the hysteresis of the comparator and tends to randomize output noise. With low-ESR caps for C2 and C4, output noise is below 30mV over the output load range. Output power increases with $V_{BATTERY}$, from about 1.4 watts out with 5 volts in to about 2 watts out with 8 volts or more. Efficiency is 80% over a broad output-power range.

If only a positive or negative output voltage is required, the two diodes and two capacitors associated with the unused output can be eliminated. The 100k Ω load is required on each output to load a parasitic voltage doubler created by the capacitance of diodes D2 and D4. Without this minimum load, the output voltage can go up to almost 50% above the nominal value.

Component Selection

The voltage at the switch pin SW1 swings from zero volts to V_{OUT} plus two diode drops. This voltage is AC coupled to the positive output through C1 and D1 and to the negative output through C3 and D3. The full output current flows through C1 and C3. Most tantalum capacitors are not rated for current flow, and their use can result in field failures. Use a rated tantalum or a rated electrolytic for longer system life. At lower output currents or higher frequencies, using monolithic ceramics is also feasible.

One could replace the 1N5819 Schottky diodes with 1N4148 types for lower cost, with a reduction in efficiency and load-regulation characteristics.

Shutdown

The circuit can be shut down in several ways. The easiest is to pull the set pin above 1.25 volts; however, this consumes 300 μ A in shutdown conditions. A lower power method is to turn off V_{IN} to the LT1107 by means of a high-side switch or by simply disabling a logic supply. This drops quiescent current from the $V_{BATTERY}$ input below 10 μ A. In both cases V_{OUT} drops to zero volts. In the that event $+V_{OUT}$ does not need to drop to zero, C1 and D1 can be eliminated.

Output Voltage Adjustment

The output voltage can be adjusted from any voltage above $V_{BATTERY}$ up to 46 volts with proper passive components. Output voltage can be controlled by the user with DAC, PWM, or potentiometer control. By summing currents into the feedback node, the output voltage can be adjusted downward. 

This design idea originally appeared in EDN magazine.

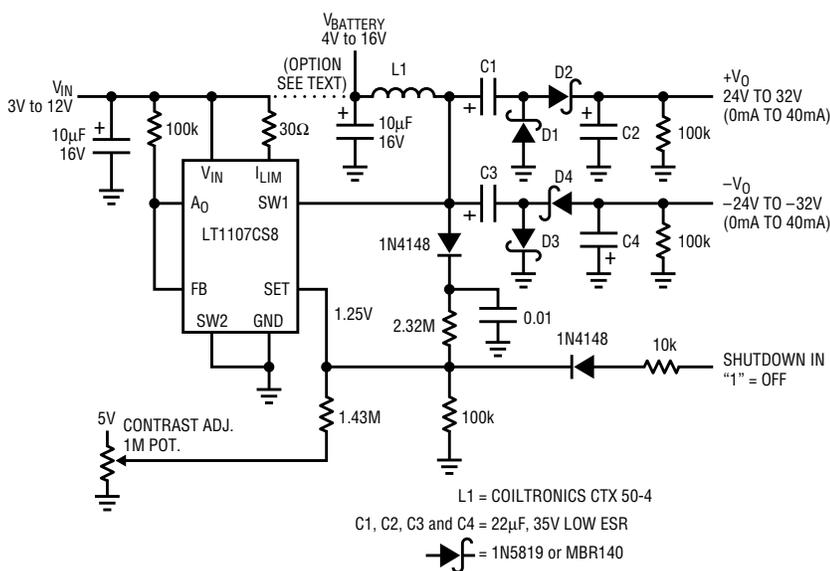


Figure 1. Schematic diagram LT1107 dual-output LCD-bias generator

A Linear-Phase Bandpass Filter for Digital Communications

by Philip Karantzalis

Bandpass filters with linear pass-band phase are useful for a variety of data communications tasks, the most noteworthy of which may be in modulation-demodulation (modem) circuitry. Modems generate signals that must be processed without phase distortion to allow error-free transmission and reception of information (or the closest approach to that ideal we can achieve).

Figure 1 shows a linear-phase bandpass filter using the LTC1264 high-frequency, universal switched-

capacitor filter building block. This filter is an eighth-order narrow bandpass filter, centered at 50kHz for a 1MHz clock input, with flat group delay in its passband. The f_{CLK} -to- f_{CENTER} frequency ratio is 20:1. Figure 2 shows the filter's narrow-band gain response and Figure 3 shows the passband group delay.

An interesting feature of linear-phase bandpass filters is that their response to a step input produces a short transient sine wave burst with a symmetrical envelope. Figure 4

shows a comparison of the transient responses to a step input for the linear phase bandpass filter of Figure 1 and a bandpass filter with a similar passband and nonlinear phase response. The response of a bandpass filter to a step input is a simple qualitative test for determining the linearity of its phase response, although in data transmission systems the measurements are usually made with eye-diagrams and constellation displays.

The maximum clock frequency for the filter is 2MHz with ± 7.5 volt supplies. This allows bandpass filters with center frequencies up to 100kHz to be realized without significant phase distortion in the passband.

Capacitor C, across R4 in sections C and D, minimizes gain and phase variations when the filter is used with clock frequencies greater than 1.4MHz. For ± 5 volt supplies, the maximum clock frequency is 1.6MHz. Use the Table 1 as a guide for the selection of capacitor C. \blacktriangleleft

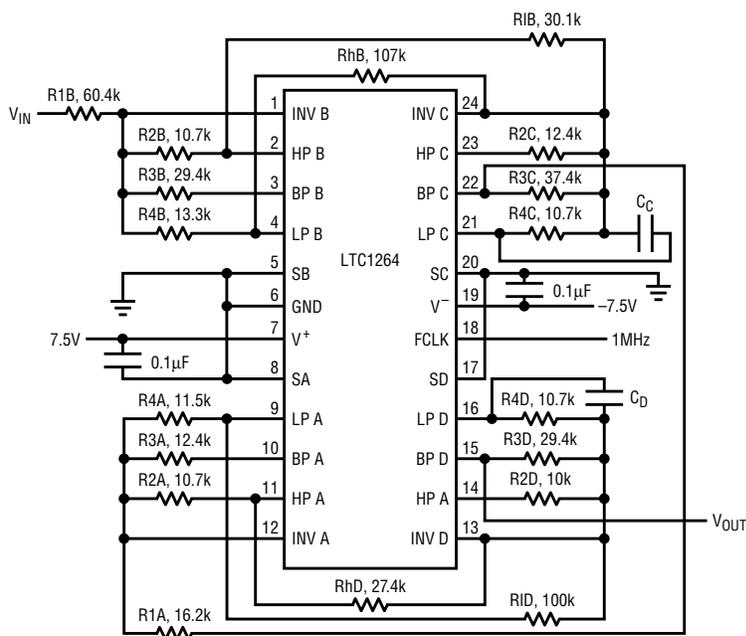


Figure 1. LTC1264 linear-phase, 8th order bandpass filter

Table 1. Capacitor selection guide

V_S	f_{CLK}	$C_C = C_D$
$\pm 7.5V$	1.8MHz	3pF
$\pm 7.5V$	2.0MHz	5pF
$\pm 5V$	1.6MHz	5pF
$\pm 5V$	1.4MHz	3pF

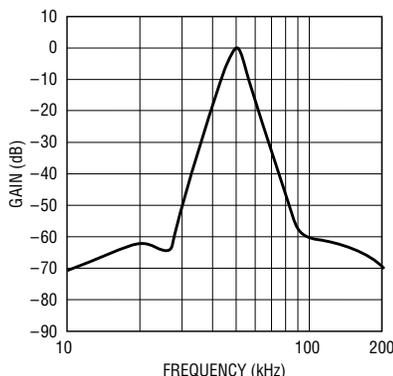


Figure 2. Filter gain versus frequency

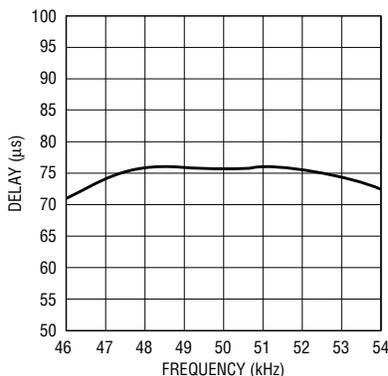


Figure 3. Filter group delay versus frequency

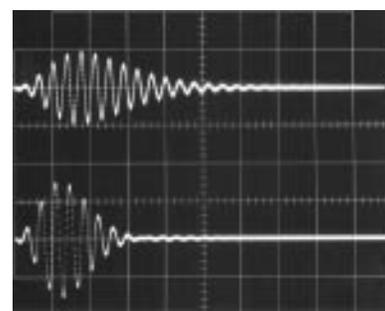


Figure 4. Step response—
Top: nonlinear-phase filter
Bottom: linear-phase filter



Book Review: Power Electronics— Circuits, Devices and Applications

by Muhammad H. Rashid, Englewood Cliffs, New Jersey,
Prentice Hall Publishing. Second Edition, 1993.

This is the first book review to appear in the pages of *Linear Technology*. As is our custom, we shall present the reader with tools that help him to do his job. We hope that by reviewing and recommending a few really useful books each year, we will help you, our customers, become even better design engineers.

While such subjects as power and DC/DC converters are certainly worthy of life-long study, one has to start somewhere. I am a novice in this area, but I chose to review this book in order to bring an unbiased viewpoint to the subject.

The book is quite a good fundamental text on power electronics. Power electronics is the study and application of solid-state electronics for the control and conversion of electric power. Rashid walks the reader through many of the basic to not-so-basic concepts inherent in the design of all types of power circuits, from large "electric company" type circuitry to DC/DC converters. For example, Rashid carefully covers the important parameters of power transistors

in his chapter on these devices. I noted, in particular, his discussions on the storage-time constant and the saturating charge in bipolar transistors. His treatment of the gate-drive requirements for MOSFETs will help the non-expert designer gain the expertise required for complex switcher designs.

The text also includes chapters on DC/DC converters, Advanced Modulation Techniques, and Resonant Converters. There is a chapter on Protection of Devices and Circuits that should be required reading for all designers, whether of power supplies or A-to-D converters.

Simulation of circuits, a topic often given the "black magic" treatment until graduate school or one's first job, receives some ink in Rashid's text. Rashid examines device models in PSpice for diodes, thyristors, power transistors, and other active devices as well as for circuits ranging from buck regulators to pulse-width-modulated inverters. These simulations are included to verify design examples and to

introduce the reader to SPICE. This is an excellent way to introduce not only the concept of modeling but the idea that each SPICE model represents a device or circuit composed of devices in the real world. Designers must build circuits from these real-world devices, so the model must match the device; though such models are simplifications and may omit some real-world complexities.

I would advise the reader to bread-board any circuits gleaned from this text. Although it is quite a good introduction to power circuitry, no text can bring home the problems encountered when real circuits are switching amperes in the vicinity of nodes that must sense millivolts.

Rashid's book is a good, concise text that includes all the right topics at a technical level that will be useful for many power-supply designers. The book also is a good introduction to power electronics for would-be power supply experts. It deserves a look. **LT**

—RM

"Picture-in-Picture" continued from page 22

only on expensive equipment. Where cost is a determining factor in system design, the exceptionally low amplitude and brief duration of the LT1204's switching artifact make it an excellent choice for active video switching.

Conclusion

Active video switching can be accomplished inexpensively and with excellent results when care is taken with both the selection and application of the high-speed multiplexer. Both fast switching and small, well-controlled switching glitches are

important. When the LT1204 is used for active video switching between two flat-field video signals (a very critical test) the switching artifacts are nearly invisible. When the LT1204 is used to switch between two live video signals, the switching artifacts are invisible. **LT**

¹ Video production, in the most general sense, means any purposeful manipulation of the video signal, whether in a television studio or on a desktop PC.

New Device Cameos

LT1161: Quad, Protected, High-Side MOSFET Driver

High-side switching in hostile environments, such as industrial control, avionics, and automotive applications, requires a ruggedized N-channel MOSFET driver. The LT1161 provides a full 100% operating voltage margin in 24V systems and can survive supply voltages from -15V to +60V (+75V on the gate) without damage.

Each of the four LT1161 switch channels has a completely self-contained charge pump to fully enhance an N-channel MOSFET switch with no external components. Also included in each switch channel is a drain-sense comparator which is used to sense switch current.

The LT1161 independently protects and restarts each MOSFET. Latch-off current limit can also be implemented with the LT1161.

The LT1161 carries an industrial temperature grade and is available in either 20-lead plastic DIP or 20-lead SO surface mount packages.

The LTC1165 Triple, Inverting 1.8V to 6V MOSFET Driver

The LTC1165 triple, inverting 1.8V to 6V gate driver makes it possible to switch either supply- or ground-referenced loads through low $R_{DS(ON)}$, N-channel switches from as little as 1.8V (two discharged cells). The inverting inputs make it possible to directly replace P-channel MOSFET switches while maintaining system-drive polarity. The LTC1165 contains three on-chip charge pumps, so that less expensive, lower $R_{DS(ON)}$ N-channel MOSFETs can be used to replace high-side P-channel switches.

The three charge pumps have been designed to be very efficient and require no external components. The standby current with the three inputs switched off is typically 0.01 μ A. The quiescent current rises to 95 μ A per channel with the input turned on and the charge pump producing 11V

from a 3.3V supply. The LTC1165 is available in both 8-pin DIP and 8-pin SOIC packaging.

LTC1143: Dual, 3.3V/5V High-Efficiency Step-Down Regulator

The LTC1143 is a dual-output switching-regulator controller in a narrow, 16-lead SOIC package that minimizes board area. The LTC1143 utilizes two independent current-mode regulator blocks to provide simultaneous 3.3V and 5V outputs with individual shutdown controls.

The LTC1143 extends battery life by providing high efficiencies at load currents ranging from milliamps to amps. Both LTC1147-based regulator blocks use current-mode architecture with Burst Mode™ operation.

The LTC1143 is ideal for low-cost applications requiring 3.3V and 5V simultaneously, with high conversion efficiencies and the smallest component count and board space.

LTC1142: Dual, 3.3V/5V Ultra-High-Efficiency Synchronous Step-Down Regulator

The LTC1142 is a dual-output, synchronous switching-regulator controller in a compact, 28-lead SSOP. Two independent regulator blocks simultaneously provide 3.3V and 5V outputs with individual shutdown controls.

Both LTC1148-based regulator blocks use current-mode architecture with Burst Mode™ operation to provide extremely high operating efficiency, typically greater than 90%, over the entire load range. The LTC1142 extends battery life by providing high efficiencies at load currents ranging from milliamps to amps.

LT1203/LT1205: 170MHz Dual and Quad Video Multiplexers

The LT1203 is a wideband, two-input video multiplexer designed for sub-pixel switching and broadcast-quality routing. The LT1205 is a four-input, two-output multiplexer

designed for multi-input expansion. These multiplexers act as SPDT video switches with 10ns transition times at toggle rates up to 30MHz. The -3dB bandwidth is 170MHz; gain flatness is -0.1dB to greater than 60MHz. Many parts can be tied together at their outputs by using a shutdown feature that reduces the power dissipation and raises the output impedance to 5M Ω . Output capacitance in shutdown mode is only 1pF and the LT1203 peaks less than 2dB with a 50pF load. Channel crosstalk and shutdown isolation are greater than 80dB at 10MHz. An on-chip logic buffer interfaces to fast TTL or CMOS edges to reduce switching transients to 50mV with a 20ns duration. The LT1203 and LT1205 outputs are protected against shorts to ground.

The LT1203 is available in 8-lead PDIP and SO packages and the LT1205 is available in the 16-lead SO package.

LTC1327, LTC1337, LTC1349, and LTC1350 Ultra-Low-Power RS232 Transceivers

Four new RS562/RS232 transceivers for notebook and palmtop computers feature the industry's lowest power consumption. Each transceiver is a three-driver/five-receiver device that offers a complete PC serial port solution for 3V or 5V systems and draws only 300 μ A quiescent supply current.

On-chip charge pumps allow operation from standard logic supplies. The charge pumps require only four space-saving 0.1 μ F capacitors and can supply up to 12mA of extra current for external circuitry. The transceivers operate up to 120k baud with a 1000pF/3k Ω loads. The parts are pin compatible with the LT1137.

All transceivers feature LTC's proprietary output structure, which withstands repeated ESD strikes of up to \pm 10kV using the human body model.

The LTC1327 is an RS562 transceiver designed for 3V systems. In the SHUTDOWN mode, the supply cur-

rent drops to less than 1 μ A. The LTC1337 is the RS232 version of the LTC1327—it operates from a 5V supply.

The LTC1349 is a 5V-supply RS232 transceiver that features two low-power receivers that remain active while in the SHUTDOWN mode. The two receivers together draw only 30 μ A of supply current. The LTC1350 is the RS562, 3V-supply version of the LTC1349.

All four circuits are available in 28-pin DIP, SSOP, and SOIC packages.

Four New Products Combine Low-Power RS562 and RS485 Transceivers On One Chip

Four new RS562/RS485 transceivers each contain two interface ports that can operate in either RS485 mode, RS562 mode, or in a combination of the two. A loopback mode performs a diagnostic self test; a shutdown mode reduces the supply current to 15 μ A. The typical unloaded supply current is only 600 μ A in normal operation.

The RS562 transceivers operate to 120k baud and are fully compliant with RS562 overvoltage specifications. The RS485 transceivers operate to 10M baud and are fully compliant with all RS485 specifications. All driver outputs feature short-circuit protection and thermal shutdown. An enable pin allows the RS485 driver outputs to be forced into three-state operation, which is maintained when the outputs are forced beyond the supply rails or the power is off. Both receiver inputs and driver outputs feature \pm 10kV ESD protection.

A +5V supply for V_{DD} and V_{CC} and a -5V supply for V_{EE} are required for RS562 operation. However, if RS232 voltage levels are required, V_{DD} can be raised to +(6.5 to 10V) and V_{EE} lowered to -(6.5 to 10V).

The LTC1321 can be configured as two RS562 transceivers, as one RS562 transceiver and one RS485 transceiver, or as two RS485 transceivers. The LTC1322 can be configured as four RS562 transceivers, as two RS562 transceivers and one RS485 trans-

ceiver, or as two RS485 transceivers. The LTC1334 and LTC1335 are pin compatible with the LTC1321 and LTC1322 respectively, except that V_{CC} is internally connected to V_{DD} and the unused pin becomes a receiver-output enable.

All four circuits are available in 24-pin DIP and SOIC packages.

LT1413 Dual, Single-Supply Precision Op Amp

The LT1413 is an improved, low-cost version of Linear Technology's industry-standard LT1013 dual, single-supply op amp. The LT1413 is optimized for single 5V applications: the input goes below ground and the output swings to ground while sinking current (no output pull-down resistors are needed). Phase-reversal protection circuitry keeps the proper phase at the output, even when the input is significantly below ground.

The specifications achieved at supply voltages of $V_+ = +5V$, $V_- = 0V$ with the low-cost plastic DIP and SO-8 grades are 280 μ V maximum offset voltage (380 μ V maximum in the SO-8), 0.8nA maximum offset current, 1.4 million voltage gain, 0.5 μ V/ $^{\circ}$ C drift, 950kHz gain-bandwidth product, 0.55 μ V peak-to-peak noise from 0.1Hz to 10Hz, and 140dB channel separation. The output delivers in excess of 10mA load current (sourcing or sinking), even though the supply current per amplifier is only 330 μ A quiescent. A full set of specifications is also provided on the LT1413 at \pm 15V supplies. \blacktriangleleft

For further information on the above or any other devices mentioned in this issue of Linear Technology, use the reader service card or call the LTC literature-service number: 1-800-4-LINEAR. Ask for the pertinent data sheets and application notes.

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology makes no representation that the circuits described herein will not infringe on existing patent rights.

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LTC in the News . . .

Fiscal 1993 Again a Record

On July 20, 1993, Linear Technology Corporation announced that net sales for its fiscal year ended June 27, 1993 were a record \$150,867,000, an increase of 26% over fiscal 1992. The company also reported record net income for the year of \$36,435,000 or \$0.99 per share.

Net sales for the fourth quarter of 1993 were a record \$42,813,000, a 31% increase over the fourth quarter of the previous year. Net income for the quarter was \$10,838,000 or \$0.29 per share, an increase of 49% over the fourth quarter of the previous year. A cash dividend of \$0.05 per share will be paid on August 18, 1993 to LTC shareholders of record on August 2, 1993.

According to Robert H. Swanson, President and CEO, "1993 was another excellent year for us. Bookings, revenues, profits, and cash generated from the business all grew handsomely. We introduced a record number of new products, brought up a second fabrication line, and commenced construction on our first offshore plant in Singapore. This balance of financial performance, product support and introduction, and sales penetration continues to be our major strategic focus."

More Rankings and Ratings

Recognition of Linear Technology's performance continues. *California Business* ranked LTC as 43rd in its Top 500 companies in California, and also ranked LTC among its Top 50 in Technology.

The *Los Angeles Times* included Linear Technology in its Top 100 Companies in California. Locally, LTC was included in the *San Francisco Chronicle's* and the *San Francisco Examiner's* Top 100 Bay Area Companies, and in the *San Jose Mercury News* Silicon Valley Top 150. \blacktriangleleft

DESIGN TOOLS

Applications on Disk

NOISE DISK

This IBM-PC (or compatible) program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise, and calculate noise using specs for any op amp. Available at no charge.

SPICE MACROMODEL DISK

This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models, and a demonstration copy of PSPICE™ by MicroSim. Available at no charge.

Technical Books

1990 Linear Databook — This 1440 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices. \$10.00

1992 Linear Databook Supplement — This 1248 page supplement to the *1990 Linear Databook* is a collection of all products introduced since then. The catalog contains full data sheets for over 140 devices. The *1992 Linear Databook Supplement* is a companion to the *1990 Linear Databook*, which should not be discarded. \$10.00

Linear Applications Handbook — 928 pages full of application ideas covered in depth by 40 Application Notes and 33 Design Notes. This catalog covers a broad range of "real world" linear circuitry. In addition to detailed, systems-oriented circuits, this handbook contains broad tutorial content together with liberal use of schematics and scope photography. A special feature in this edition includes a 22 page section on SPICE macromodels. \$20.00

1993 Linear Applications Handbook Volume II — Continues the stream of "real world" linear circuitry initiated by the *1990 Handbook*. Similar in scope to the 1990 edition, the new book covers Application Notes 41 through 54 and Design Notes 33 through 69. Additionally, references and articles from non-LTC publications that we have found useful are also included. \$20.00

Interface Product Handbook — This 200 page handbook features LTC's complete line of line driver and receiver products for RS232, RS485, RS423, RS422 and AppleTalk® applications. Linear's particular expertise in this area involves low power consumption, high numbers of drivers and receivers in one package, 10kV ESD protection of RS232 devices and surface mount packages. Available at no charge.

Monolithic Filter Handbook — This 232 page book comes with a disk which runs on PCs. Together, the book and disk assist in the selection, design and implementation of the right switched capacitor filter circuit. The disk contains standard filter responses as well as a custom mode. The handbook contains over 20 data sheets, Design Notes and Application Notes. \$40.00

SwitcherCAD Handbook — This 144 page manual, including disk, guides the user through SwitcherCAD—a powerful PC software tool which aids in the design and optimization of switching regulators. The program can cut days off the design cycle by selecting topologies, calculating operating points and specifying component values and manufacturer's part numbers. \$20.00

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