

Industrial/Automotive Step-Down Regulator Accepts 3.6V to 36V and Includes Power-On Reset and Watchdog Timer in 3mm × 3mm QFN

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Introduction

As the number of microprocessors in automotive and industrial applications continues to expand, so does the need for rugged step-down regulators that can operate over a wide input voltage range and withstand high voltage transients and output shorts. Microprocessor-based applications also require supervisory functions, such as power-on reset (POR) and watchdog timing, to ensure high system reliability. The regulator must have high efficiency at light loads to increase battery life. The LT3689 delivers all of these features in tiny 16-pin 3mm × 3mm QFN and 16-pin MSOP packages.

Features of the LT3689 Step-Down Regulator

The LT3689 employs a constant frequency, current mode architecture to provide 800mA of continuous output current. The part operates from a wide 3.6V to 36V input range and can protect itself from input transients up to 60V. It is internally compensated, which helps to lower the external component count. The switching frequency can be set anywhere between 350kHz and 2.2MHz by tying a resistor from

the R_T pin to ground, allowing the designer to optimize component size and efficiency. The switching frequency can also be synchronized to an external clock for noise sensitive applications. An external resistor divider programs the output voltage to any value above the part's 0.8V reference. Also, the boost diode is integrated into the IC to minimize solution size and cost. Figure 1 shows a typical application of LT3689.

Soft-Start and Output Short Circuit Protection

The LT3689 includes a soft-start feature that limits the maximum inrush current during start-up and recovery from fault conditions. The soft-start circuit ramps up the peak switch current limit in approximately 150 μ s, reducing the peak input current.

The DA pin is used to monitor the current in the catch diode. If the catch diode current at the end of switch cycle is higher than the DA current limit then the part delays the switch turn-on until the catch diode current drops below the DA current limit. This protects the LT3689 in the face of inductor current runaway situations,

especially during output overload or short at high switching frequencies with high input voltages and small inductor values. Other protection features such as frequency foldback, cycle-by-cycle current limit, and thermal shutdown together ensure that the part is not damaged by excessive switch currents during startup, overload or short circuit.

Pin Selectable Modes of Operation: Low Ripple Burst Mode Operation and Pulse-Skipping Mode

Two modes of operation can be selected through the SYNC pin. Applying a logic low to the SYNC pin enables the low ripple Burst Mode[®] operation, which maintains high efficiency at light loads while keeping output ripple low. In Burst Mode operation, the LT3689 delivers single cycle bursts of current to the output capacitor followed by sleep periods. Between bursts, all circuitry associated with controlling the output switch is shutdown, reducing the V_{IN} pin and OUT pin currents in a typical application to a mere 50 μ A and 75 μ A, respectively. As the load current decreases to a no load condition, the percentage of sleep time increases, thus decreasing average input current.

A logic high on SYNC disables Burst Mode operation, allowing the part to skip pulses at light loads. The advantage of this pulse-skipping mode over Burst Mode operation is that the part continues to switch at the programmed frequency (set by R_T) down to very low load currents, above 15mA at 12V_{IN} in a typical application.

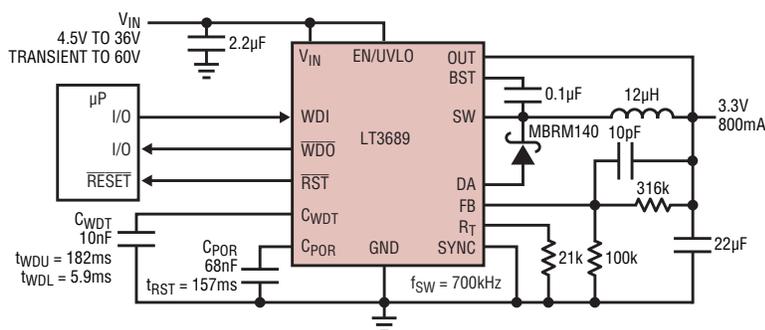


Figure 1. LT3689 typical application circuit with reset time set to 157ms and watchdog timeout period set to 182ms

Programmable Undervoltage Lockout

The LT3689 can be shutdown by pulling the EN/UVLO pin below 0.3V. In shutdown, quiescent current is less than 0.5 μ A. The EN/UVLO pin can also be used to perform an accurate undervoltage lockout (UVLO) function. A resistor divider from V_{IN} pin can be used to program the UVLO threshold of the circuit using the 1.26V accurate threshold of the EN/UVLO pin. A 4 μ A current hysteresis on this pin is also provided to allow the user to program desired voltage hysteresis. The LT3689 also has an internal UVLO that prevents the part from switching if V_{IN} pin ever goes below 3.3V (typical). The part only starts switching when V_{IN} is higher than 3.4V and EN/UVLO pin is above the 1.26V threshold.

Low Dropout

The LT3689 features low dropout for output voltages above 3V. The minimum operating voltage of the device is determined either by the LT3689's internal undervoltage lockout or by its maximum duty cycle. Unlike many buck regulators, the LT3689 can extend its duty cycle by staying on for multiple cycles, provided that the boost capacitor is charged above the minimum voltage of 2.5V. Eventually, after several switching cycles, the boost capacitor discharges. Internal circuitry detects this condition and charges the boost capacitor only when needed. Also, a bigger boost capacitor allows even higher duty cycle, allowing extremely low dropout operation. The dropout voltage for a 5V typical application is about 400mV at 200mA load and 900mV at 800mA load.

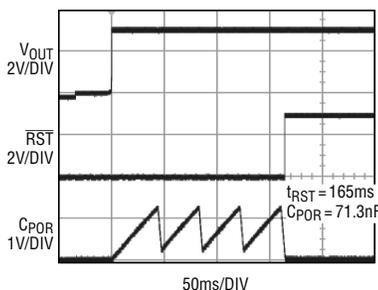


Figure 2. Power-on reset feature of LT3689

Power-On Reset (POR)

Many microprocessor-based applications powered by the output of a switching regulator must know when the regulator output is ready and stable before the microprocessor starts operating. Likewise, once running, the electronic system must be warned when the regulator output has dropped below a minimum tolerable threshold, such as during overload or shutdown conditions. This is required to prevent unreliable operation and to allow the microprocessor to perform housekeeping operations before power is completely lost.

The LT3689's accurate internal voltage reference and glitch immune precision POR comparator and timer circuit feed these specific needs of microprocessor-based applications. The switcher's output voltage must be above 90% of programmed value for its \overline{RST} pin to remain high (refer to Figure 2). The LT3689 asserts \overline{RST} during power-up, power-down and brown-out conditions. Once the output voltage rises above the \overline{RST} threshold, the adjustable reset timer is started and \overline{RST} is released after the reset timeout period. On power-down, once output voltage drops below \overline{RST} threshold, \overline{RST} is held at a logic low. The reset timer is adjustable using an external capacitor. The \overline{RST} pin has a weak pull up to the OUT pin.

The POR comparator is designed to avoid false triggering. High frequency noise on the FB pin can falsely trip \overline{RST} , particularly when the monitored output is already near the reset threshold. This can cause oscillatory behavior at the \overline{RST} pin. The traditional way of tackling this problem is to add some DC hysteresis in the comparator input, which changes the threshold point once the output flips. The problem is that the addition of DC hysteresis makes the trip voltage less accurate, since the trip point changes once the output changes. The LT3689 does not use hysteresis. Instead, it performs an integration-like function on transient events at the comparator. In this way the magnitude and duration of the event are both important to the comparator threshold. Figure 3 illustrates

the typical transient duration versus comparator overdrive (as a percentage of trip threshold) required to trip the comparator.

Selecting the Reset Timing Capacitor

The reset timeout period is adjustable in order to accommodate a variety of microprocessor applications. The reset timeout period, t_{RST} , is adjusted by connecting a capacitor between the C_{POR} pin and ground. The value of this capacitor is determined by:

$$C_{POR} = t_{RST} \cdot 432 \cdot 10^{-9}$$

with C_{POR} in Farads and t_{RST} in seconds. The C_{POR} value per millisecond of delay can also be expressed as $C_{POR}/ms = 432$ (pF/ms).

Leaving the C_{POR} pin unconnected generates a minimum reset timeout of approximately 25 μ s with 10k Ω pull-up to 5V on \overline{RST} pin. Maximum reset timeout is limited by the largest available low leakage capacitor. The accuracy of the timeout period will be affected by capacitor leakage (the nominal charging current is 2 μ A) and capacitor tolerance. A low leakage ceramic capacitor is recommended.

Watchdog Modes: Timeout or Window

The LT3689 also includes an adjustable watchdog timer that monitors a microprocessor's activity. If a code execution error occurs in a μ P, the watchdog detects the error and sets the \overline{WDO} pin low. This signal can be used to interrupt a routine or to reset a μ P.

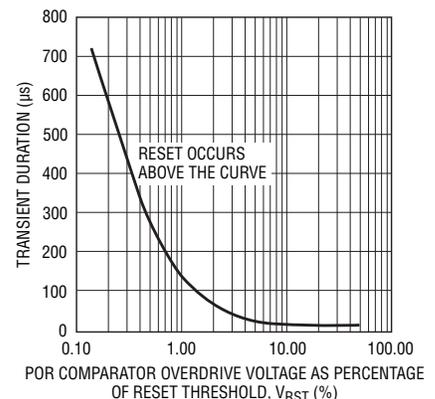


Figure 3. Typical transient duration vs POR comparator overdrive

The watchdog is operated either in timeout or window mode (refer to Figure 4). In timeout mode, the microprocessor needs to toggle the WDI pin before the watchdog timer expires to keep the \overline{WDO} pin high. If the voltage on the WDI pin does not transition during the programmed timeout period then the circuitry pulls \overline{WDO} low.

In window mode, the WDI pin's negative-going pulses must appear inside a programmed time window to prevent \overline{WDO} from going low. If more than two falling pulses are registered in the lower boundary period (t_{WDL}), the \overline{WDO} pin is forced low. The \overline{WDO} pin also goes low if no negative edge is supplied to the WDI pin within the upper boundary period (t_{WDU}).

During a code execution error, the microprocessor outputs WDI pulses that are either too fast or too slow. This condition asserts \overline{WDO} low and forces the microprocessor to reset the program.

In window mode, the WDI signal is bounded by an upper and lower boundary periods for normal operation. The period of the WDI input signal should be longer than the window mode's lower boundary period and shorter than the upper boundary period to keep \overline{WDO} high under normal conditions. The window mode's lower and upper boundary periods have a fixed ratio of 31. These times can be increased or decreased by adjusting an external capacitor on the C_{WDT} pin.

In both watchdog modes, when \overline{WDO} is asserted, the reset timer is enabled. Any WDI pulses that appear while the reset timer is running are ignored. When the reset timer expires, the \overline{WDO} is allowed to go back high again. Therefore, if no input is applied to the WDI pin then the watchdog circuitry produces a train of pulses on the \overline{WDO} pin. The high time of this pulse train is equal to the upper boundary period and low time is equal to the reset period. Also, \overline{WDO} and \overline{RST} cannot be logic low simultaneously. If \overline{WDO} is low and there is an undervoltage lockout fault, \overline{RST} goes low and \overline{WDO} will go high.

The \overline{WDE} pin allows the user to turn on or off the watchdog function. This

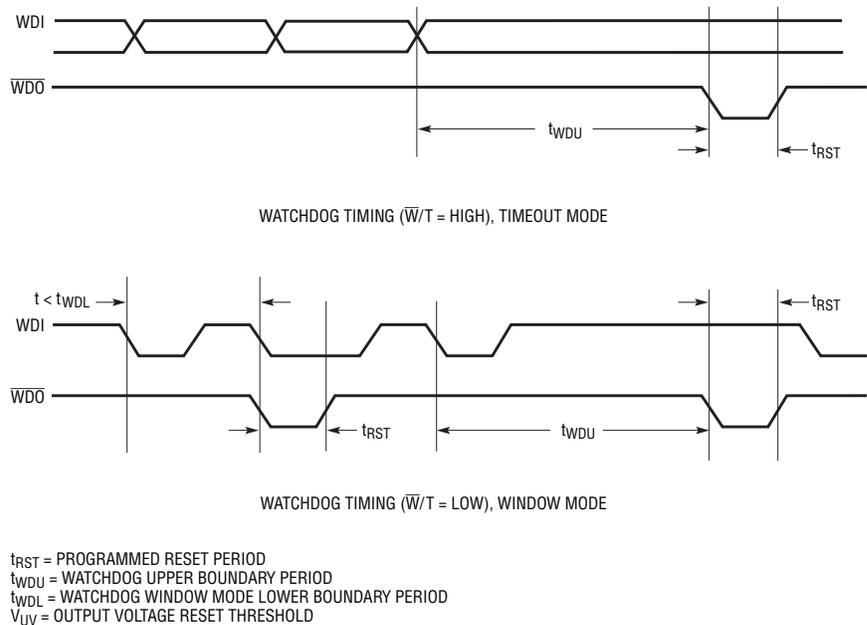


Figure 4. Watchdog timing diagram

feature can be used to reliably program the connected microprocessor in the factory. During factory programming of the microprocessor, \overline{WDE} pin can be kept high to prevent \overline{WDO} from toggling and thus prevents \overline{WDO} from interfering with the microprocessor's programming procedure.

Tying the \overline{WDO} and \overline{RST} pins together will generate a reset signal when either the output voltage falls 10% below the regulation value or if there is a watchdog error.

Selecting the Watchdog Timing Capacitor

The watchdog upper boundary period is adjustable and can be optimized for software execution. The watchdog upper boundary period is adjusted by connecting a capacitor between the C_{WDT} pin and ground. Given a specified watchdog upper boundary period, the capacitor is determined by:

$$C_{WDT} = t_{WDU} \cdot 55 \text{ (pF/ms)}$$

The window mode lower boundary period has a fixed relationship to upper boundary period for a given capacitor. The lower boundary period is related to the upper boundary period by the following:

$$t_{WDL} = 1/31 \cdot t_{WDU}$$

Leaving the C_{WDT} pin unconnected generates a minimum watchdog upper boundary period of approximately 200 μ s with 10k Ω pull-up to 5V on \overline{WDO} pin. Maximum timeout is limited by the largest available low leakage capacitor. The accuracy of the upper and lower boundary periods is affected by capacitor leakage (the nominal charging current is 2 μ A) and capacitor tolerance. A low leakage ceramic capacitor is recommended.

Conclusion

The wide input range, low quiescent current, supervisory features, robustness and small size of the LT3689 makes it an ideal candidate to power automotive and industrial applications. The part withstands 60V V_{IN} transients and normal operation is guaranteed for max V_{IN} of 36V, and the part is robust against inrush and short circuit conditions. The Burst Mode circuitry provides high efficiencies at light loads. Programmable switching frequency allows the designer to trade off between component size and efficiency. The accurate POR and Watchdog circuitry of LT3689 allows complete supervisory control of a microprocessor connected to the output of the LT3689 switching regulator.