Quad Output Regulator Meets Varied Demands of Multiple Power Supplies

by Michael Nootbaar

Introduction

Many modern electronic devices require a number of power domains to satisfy the needs of a wide variety of devices and subsystems. A power supply designer’s job would be relatively easy if the design constraints were limited to simply providing well-regulated voltages, but power supply requirements are typically much more complicated. For example, multiple power rails must be sequenced and/or track each other to ensure proper system behavior. High power sections of the design are often powered down when not in use, requiring multiple shutdown options. Powering analog circuitry adds the demand for clean, low noise supplies—no switching transients or excessive voltage ripple allowed. And, of course, all supplies must be generated as efficiently as possible to minimize power consumption.

The LT3507 meets these requirements by combining three switching regulators and a low dropout linear regulator in a compact 5mm × 7mm QFN package. The switching regulators have internal power switches, independent input supplies, run and track/soft-start controls, and power good indicators. The LDO requires an external NPN pass transistor and includes track/soft-start control.

Three Independent Switching Regulators...

The LT3507 includes three independent, monolithic switching regulators to achieve a space saving solution. Channel 1 is capable of providing up to 2.4A of output current. Channels 2 and 3 are each capable of providing up to 1.6A of output current. Each of the three switching regulators has its own input supply pin to the power switch. The regulators may be operated from different supplies in order to maximize system efficiency.

The maximum voltage on any of the $$V_{IN}$$ pins is 36V. The LT3507 internal circuitry is powered from $$V_{IN1}$$, which requires a minimum operating voltage for $$V_{IN1}$$ of 4V. The minimum operating voltage for $$V_{IN2}$$ and $$V_{IN3}$$ is 3V. Since $$V_{IN1}$$ powers the internal circuitry, it must always be at least 4V when any channel is running, even if Channel 1 is off.

All three regulators use a current mode, constant frequency

Figure 1. The LT3507 in a wide input range, quad output application
architecture, which simplifies loop compensation. External compensation allows custom tailoring of loop bandwidth, transient response and phase margin. The feedback reference is 0.8V, allowing output voltages as low as 0.8V.

The regulators share a master oscillator that is resistor programmable from 250kHz to 2.5MHz, or can be synchronized to an external frequency in the same range. Each regulator features frequency foldback in overload conditions to improve short circuit tolerance. Channel 1 operates 180° out of phase with respect to channels 2 and 3 to reduce input current ripple.

…and a Low Dropout Linear Regulator

The LT3507 also includes an LDO linear regulator that uses an external NPN pass transistor to provide up to 0.5A of output current. The base drive can supply up to 10mA of base current to the pass transistor and is current limited. The LDO is internally compensated and is stable with output capacitance of 2.2µF or greater. It uses the same 0.8V feedback reference as the switching regulators.

The LDO drive current is drawn from the BIAS pin if it’s at least 1.5V higher than the DRIVE pin voltage, otherwise it’s drawn from VIN. This reduces the power consumption of the LDO, especially when VIN is at high voltages.

The LDO does not have a separate RUN pin; it is powered up when any of the RUN pins are high. The LDO can be shut down when it is not used by pulling the FB pin above 1.25V with at least 30µA. If independent control of the LDO is needed, the LDO output can be forced to 0V by pulling the TRK/SS4 pin low. If the track or soft-start functions are needed, use an open drain output in parallel with the track or soft-start circuitry described below. If track and soft-start are not necessary, then a standard CMOS output (from 1.8V to 5V) is sufficient.

Run Control

Each of the switching regulators has a RUN pin to allow flexibility in shutting off power domains. The RUN pin is 0.8V, allowing output voltages as low as 0.8V. This current is about 3µA at 0.8V. If the regulator is not used by the RUN pins are high. The LDO can be shut down when it is not used by pulling the FB pin above 1.25V with at least 30µA. If independent control of the LDO is needed, the LDO output can be forced to 0V by pulling the TRK/SS4 pin low. If the track or soft-start functions are needed, use an open drain output in parallel with the track or soft-start circuitry described below. If track and soft-start are not necessary, then a standard CMOS output (from 1.8V to 5V) is sufficient.

Track/Soft-Start Control

Each of the switching regulators has a RUN pin to allow flexibility in shutting off power domains. The RUN pin is 0.8V, allowing output voltages as low as 0.8V. If the regulator is not used by the RUN pins are high. The LDO can be shut down when it is not used by pulling the FB pin above 1.25V with at least 30µA. If independent control of the LDO is needed, the LDO output can be forced to 0V by pulling the TRK/SS4 pin low. If the track or soft-start functions are needed, use an open drain output in parallel with the track or soft-start circuitry described below. If track and soft-start are not necessary, then a standard CMOS output (from 1.8V to 5V) is sufficient.

Undervoltage and Overvoltage Protection

Each switching regulator has its own input undervoltage shutdown to prevent the circuit from operating erratically in undervoltage conditions. VIN1 shuts down at 4.0V, and because it’s the primary input voltage, it turns off the entire LT3507. VIN2 and VIN3 shut off at 3.0V and only shut off the switch on the affected channel.

The LT3507 also has a user programmable undervoltage and overvoltage lockout. The undervoltage lockout can protect against pulse stretching and regulator dropout. It can also protect the input source from excessive current since the buck regulator is a constant power load and draws more current when the input source is low. The overvoltage lockout
can protect the rectifier diodes from excessive reverse voltage and can prevent pulse-skipping by limiting the minimum duty cycle. Both of these lockouts shut off all four regulators whenever the LT3507 is powered up. This leads to a dilemma if the clock source is to be powered from one of the LT3507 regulators: there is no clock until the regulator comes up, but the regulator won’t come up until there’s a clock! This situation is easily overcome with a capacitor, a low leakage diode and a couple of resistors. The capacitor isolates the clock source from the R_T/SYNC pin until the power is up and the resistor on the R_T/SYNC pin sets the initial clock frequency. The application in Figure 1 shows how this is done.

**Typical Application**

Figure 1 shows a typical LT3507 application. This application allows a very wide input range, from 6V to 36V. It generates four outputs: 5V, 3.3V, 2.5V and 1.8V. Efficiencies for three of the outputs are shown in Figure 2. The LDO produces a particularly low noise output at 2.5V, as shown in Figure 3.

The outputs are set to coincident tracking using the 5V supply as the master. But wait, there’s no resistor divider on the TRK/SS4 pin! It’s no mistake; the LDO output coincidently tracks the supply it’s sourced from (the 3.3V supply in this case) as long as Q1 is a low V_CE transistor, such as the NSS30101 used here. Just remember that this little cheat only works for coincident tracking. Figure 4 shows the start-up waveforms of the four outputs.

In this application, the clock is synchronized to an external source that is powered from the 3.3V output. A capacitor isolates the clock until the 3.3V supply is good, and then passes the clock signal to the RT/SYNC pin. It should be noted that the LDO can actually supply up to 0.5A as long as \( I_{OUT4} + I_{OUT2} \leq 1.5A \).

**Conclusion**

The LT3507 provides a compact solution for four power supplies. Its tiny 5mm × 7mm QFN package includes three highly efficient switching regulators and a low dropout linear regulator. Just a few small inductors and ceramic capacitors are needed to create four high efficiency step-down regulators. Plenty of options insure that the LT3507 meets the needs of a wide variety of multiple output applications.

A MATLAB simulation performed using a pseudo-random channel predicts distortion at LT5575 output of –135.8dBm. This result agrees well with the equation 8, which predicts a distortion power of –135.7dBm. Refer this signal back to the receiver input:

- RF gain preceding LT5575: 20dB
- Equivalent interference level at Rx input: –155.8dBm
- Thermal noise at receiver input: –101.2dBm
- Equivalent interference in this case is 54.6dB below the thermal noise at the receiver input. The resulting degradation in sensitivity is <0.1dB, so the receiver easily meets the specification of –121dBm.

**Conclusion**

The calculations given here using the LT5575 I/Q demodulator show that a WCDMA wide area basestation receiver can be successfully implemented using a direct conversion architecture. The high 2nd order linearity and input 1dB compression point of the LT5575 are critical to meeting the performance requirements of such a design.

**Design Features**

The switching frequency is set by a single resistor to the R_T/SYNC pin. The value is adjustable from 250kHz to 2.5MHz. Higher frequencies allow smaller inductors and capacitors, but efficiency is lower and the supply has a smaller allowable range of step-down ratios due to the minimum on and off time constraints.

The frequency can also be synchronized to an external clock by connecting it to the R_T/SYNC pin. The clock source must supply a clock signal whenever the LT3507 is powered up. This leads to a dilemma if the clock source is to be powered from one of the LT3507 regulators: there is no clock until the regulator comes up, but the regulator won’t come up until there’s a clock! This situation is easily overcome with a capacitor, a low leakage diode and a couple of resistors. The capacitor isolates the clock source from the R_T/SYNC pin until the power is up and the resistor on the R_T/SYNC pin sets the initial clock frequency. The application in Figure 1 shows how this is done.

**Frequency Control**

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