500nA Supply Supervisors Extend Battery Life in Portable Electronics

by Bob Jurgilewicz

Introduction

Power consumption is an important concern in the design of electronic devices, particularly battery-powered products. The challenge facing a device designer is how to add features without significantly degrading the device's battery run time. For instance, take apart any modern portable device and you will find a number of integrated circuits that draw some current even when they are idle. It is important to minimize both quiescent and operating currents of the embedded circuits to maximize the operating battery life of the application.

Sometimes, under weak battery conditions, you may turn on a device only to find it unresponsive and partially configured after premature termination of its power-on sequence. One way to avoid this is to monitor the system power with supply supervisors that require very little power, allowing them to respond even when a battery is significantly drained. The LTC2934 and LTC2935 ultra-low power supervisors provide accurate voltage monitoring and microprocessor control during all phases of equipment operation. System initialization, early power-fail warning, manual reset and power-on/off reset generation are all included, requiring a scant 500nA from your power source.

While ideal for battery powered products, the LTC2934 and LTC2935 can be used in any system requiring voltage monitoring and/or microprocessor control. The supervisors' ultra-low load current allows products to use smaller batteries and have longer operating life. Typical applications include portable data-loggers, medical devices, remote systems and intrinsically safe equipment.

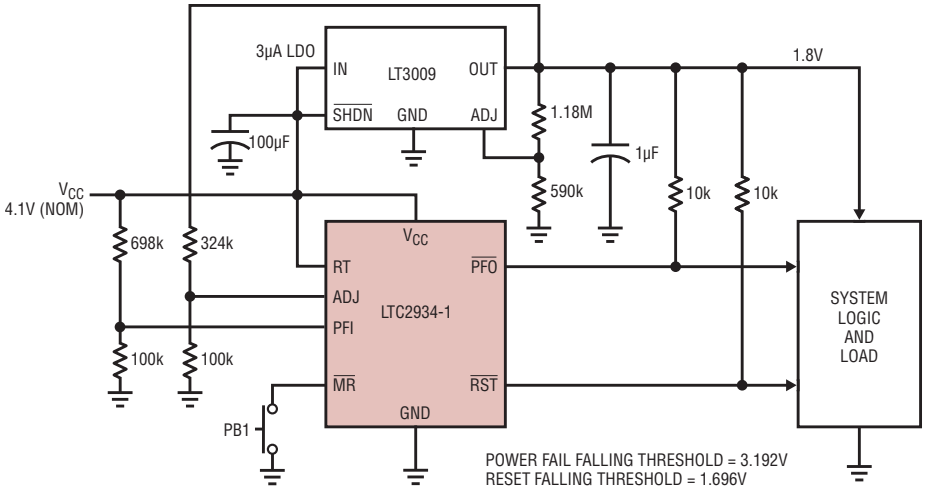

Figure 1. Typical supply monitor application

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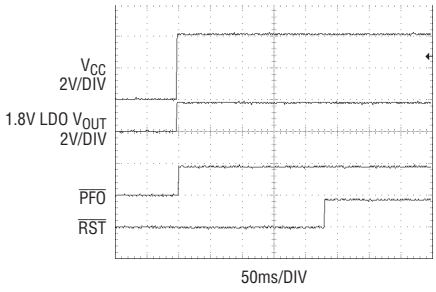

Figure 2. Typical power-up waveforms

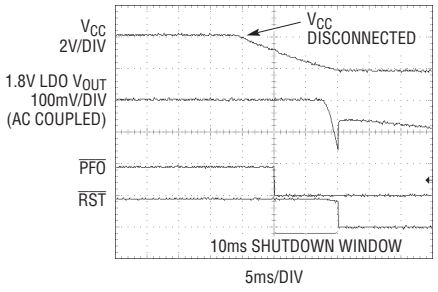

Figure 3. Typical power-down waveforms

Rising Supplies: Start-Up is Im-POR-tant

It is important to control the start-up of devices as power supplies come online. The LTC2934/35 power-on reset (POR) function provides voltage monitoring and logic control to prevent starting a microprocessor at insufficient supply voltage. The POR function also generates a time delay to provide some margin for supply voltage settling. This time delay also allows a processor oscillator to build up and reach a stable frequency before permitting the microprocessor to execute code.

The reset output ($\overline{RST}$) from the supervisor typically connects to the reset input of the microprocessor. During system start-up, the supervisor holds the $\overline{RST}$ output low. Once the voltage reaches a prescribed minimum value, the internal reset timer begins to run, holding the $\overline{RST}$ output low for an ad-

ditional time (typically 200ms). When the reset timer expires, the $\overline{RST}$ output pulls high and releases the microprocessor from its reset condition.

Figure 2 shows the supply rising waveforms obtained from the typical application shown in Figure 1. When V_{CC} exceeds the power-fail threshold plus 2.5% hysteresis (3.192V × 1.025 = 3.272V), the power-fail output ($\overline{PFO}$) is allowed to pull high. The LT3009 (a 3µA LDO) is powered from V_{CC}. Since the $\overline{PFO}$ output is pulled up by the LDO output, $\overline{PFO}$ will follow the LDO. When the LDO output exceeds the reset threshold plus 5% hysteresis (1.696V × 1.05 = 1.781V), the internal reset timer begins to run. After 200ms, $\overline{RST}$ pulls high and system logic connected to $\overline{RST}$ is released from its reset condition.

Falling Supplies: Heed the Early Warning

Unmanaged power loss can cause many system problems. The LTC2934 and LTC2935 contain a power-fail logic output ($\overline{PFO}$) that pulls low to provide an early warning of impending power loss. To be useful, an early warning should occur before the monitored supply falls to insufficient levels and well before the $\overline{RST}$ output pulls low. The time between $\overline{PFO}$ and $\overline{RST}$ pulling low can be used to initiate a variety of critical operations prior to shutdown. Once the supervisor pulls the microprocessor reset low, it may be impossible to execute operations. Operations initiated by a power-fail warning include shutting off non-critical components to conserve energy and writing important data to memory. Some secure applications may also require erasing data to thwart memory snoopers.

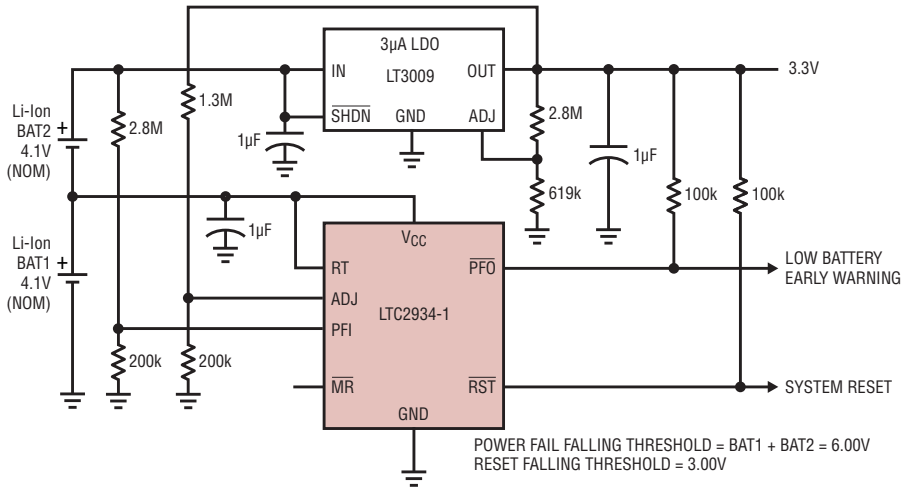

Figure 4. Stacked Li-ion cell and LDO supervisor

Figure 3 shows the supply falling waveforms obtained from the application shown in Figure 1. The waveforms demonstrate how $\overline{PFO}$ provides ample warning when V_{CC} is suddenly disconnected from the system. The LT3009 supplies a constant 10mA to a load at 1.8V. The 100µF input capacitor begins to discharge when V_{CC} (4.1V nominal) is disconnected. The power-fail threshold is configured for 3.192V.

Because the power-fail condition persists and is not merely transitory, logic output $\overline{PFO}$ pulls low and remains low after a small comparator delay. This is when the system logic (typically connected to $\overline{PFO}$) should take appropriate shutdown action(s). In this application, the remaining operating time beyond power fail is approximately 10ms. Eventually V_{CC} becomes so low that the LDO begins to drop out. $\overline{RST}$ asserts low shortly after the LDO output falls below the reset threshold (1.696V). At this point, the system load is removed and the LDO output begins to recover. However, the remaining loads and built-in hysteresis prevent the LDO recovery from glitching the $\overline{RST}$ output.

Table 1. Falling threshold selection table

Reset Threshold (V)	Power-Fail Threshold (V)	S1	S2	S0
3.30	3.45	Low	Low	Low
3.15	3.30	Low	Low	High
3.00	3.15	Low	High	High
2.85	3.00	Low	High	Low
2.70	2.85	High	High	Low
2.55	2.70	High	Low	Low
2.40	2.55	High	Low	High
2.25	2.40	High	High	High

Select Fixed or Adjustable Thresholds

The LTC2935 integrates eight precision reset and power-fail threshold pairs. Configure any one of the eight threshold pairs using three digital select inputs (see Table 1). Typical applications using the LTC2935 require no additional external components. As a result, solutions require little board space and are extremely low power.

Use the LTC2934 when custom (adjustable) thresholds are necessary. The LTC2934 monitors voltage applied to its PFI and ADJ inputs, typically through an external resistive divider. External divider resistance values can be large which helps keep the current low. Divider errors due to input leakage current (1nA maximum over temperature) are often too small to worry about. The PFI and ADJ inputs have precision 400mV thresholds

(falling), so low voltage monitoring is possible.

The falling threshold accuracy for both the LTC2934 and LTC2935 is ±1.5% over the full operating temperature range. Minimum V_{CC} is a low 1.6V. Configuration details are discussed in the LTC2934 and LTC2935 data sheets.

Manual Reset and Reset Timing

The LTC2934 has two selectable reset timeout periods. Tie the RT input low for a 15ms timeout. Tie the RT input high for a 200ms timeout. The LTC2935 has a fixed 200ms timeout. Both parts have a manual reset input which asserts $\overline{RST}$ low when the $\overline{MR}$ input is pulled low (typically with a switch). The $\overline{MR}$ input has an internal 900k pull-up resistor to V_{CC}, used to pull up the $\overline{MR}$ input when the switch is open. Alternatively, the $\overline{MR}$ input may be pulled low with an external logic signal. When the $\overline{MR}$ input returns high, $\overline{RST}$ pulls high after the reset timeout period has elapsed, assuming that the monitored input voltage is above the reset threshold.

Monitoring a 2-Cell Li-Ion Stack

Some portable applications utilize a stack of batteries to achieve greater product operating lifetime. For a product using two stacked 4.1V Li-ion cells (or similar), the total stack voltage (8.2V) exceeds the maximum operating voltage (5.5V) of the LTC2934. However, if the center tap of the 2-cell stack is available, cell monitoring is still possible. Figure 4 shows how the center tap of the stack is used to bias the LTC2934. The total stack voltage is monitored at the power-fail input (PFI). The application is configured to pull the $\overline{PFO}$ output low when the sum of the battery voltages drops below 6.00V. The adjustable input (ADJ) monitors the LDO output. $\overline{RST}$ pulls low when the LDO output drops below 3.00V.

Super Hysteresis

Some applications have a large load transient when powered. This transient can cause significant supply voltage drop if battery series resistance is large. If the load is enabled after the reset output pulls high, the subsequent voltage drop could put the voltage at the V_{CC} monitor input below threshold, causing the reset and power-fail outputs to pull low. In such cases, active threshold control (shown in Figure 5) is helpful. The LTC2935 power-fail output ($\overline{PFO}$) can be used to change any (or all) of the threshold control input states (S2, S1, S0). The power fail comparator threshold is always 150mV larger than the reset threshold and the power-fail output does not experience the 200ms reset timeout delay. If the power-fail output pulls high before the reset output (which is almost always the case with rising supplies), it can then be used to lower the falling thresholds to one of the other seven threshold selections. In Figure 5, the reset falling threshold is changed from 3.3V ($\overline{PFO}$ low) to 2.25V ($\overline{PFO}$ high), which provides a generous 1.05V of falling hysteresis.

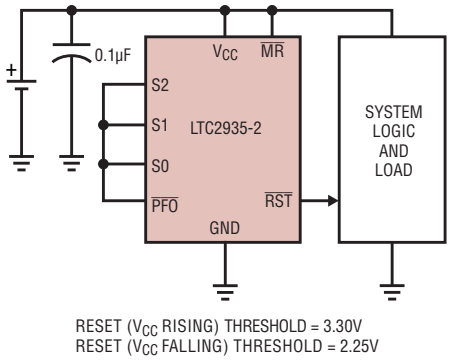

Figure 5. Active threshold control

Conclusion

The 500nA current required by the LTC2934 and LTC2935 supervisors is so small, it can be placed into the "Don't Care" column of your device power budget. Although the power is low, these supervisors don't discard features. The power-on reset and early power-fail warning signals provide glitch-free logic controls to your system logic. Reset delay time is built in. Manual reset is available in both parts. Configuring these supervisors is easy, and few if any external components are necessary. Ultra-low input leakage specifications make high impedance applications possible. Specifications are guaranteed from –45°C to 85°C. Both parts are available in space saving 8-lead, 2mm × 2mm DFN and TSOT-23 (ThinSOT™) packages.

LTC4110, continued from page 21

at all times. However, if you do not have SMBus in the product, the LTC4110 can be configured to enable preset status information to drive the GPIO bits on power up. This information can be used to drive status LEDs.

Micropower Shutdown and Shipping

The LTC4110 shutdown pin is designed to prevent false shutdowns on power up or power down. Reading the pin status is pre-qualified such that it is only honored under normal conditions. This qualification allows the product to ship with the battery installed without fear of the part entering into battery backup mode and draining the battery. The shutdown current only draws 20µA from the battery. This is the same shutdown mode that the LTC4110 enters when the backup battery reaches its end of discharge point.

Conclusion

The LTC4110 is a flexible standalone battery backup controller. By integrating key features into a single IC, functions work together seamlessly, allowing the designer to offer a reliable and complete battery backup system with minimal design effort.

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