

Hot Swap Controller Enables Standard Power Supplies to Share Load

by Vladimir Ostrerov

Introduction

The LTC4350 Hot Swap™ and load share controller is a powerful tool for developing high availability redundant and load sharing power supply systems. It has the unique ability to work with supplies with any output stage topology, including output stages using synchronous rectification.

Although the LTC4350 does much of the heavy lifting in maintaining a well balanced load share system, there are a number of important considerations in designing a stable system.

This article deals with some of the more complex design details of the LTC4350. If you are designing a load share system and LTC4350 is new to you, it may be helpful to first read introductory details in the LTC4350 data sheet, and the article “Combo/Hot Swap Load Share Controller Allows the use of Standard Power Modules in Redundant Power Systems” in the June, 2003 issue of *Linear Technology* magazine.

A Little Background

DC/DC converters are paralleled for any of several reasons:

- ❑ **One converter may be insufficient for the required power level.** For example, an existing single regulator design may be able to handle 100W, but a new application calls for up to 200W. Paralleling two, production-proven 100W converters saves time over developing a new converter capable of twice the power.
- ❑ **The product may need to be scalable.** Many rack-based systems feature multiple slots, which may be populated at some future date, but why install power supply sufficient to operate the entire rack when only a fraction of the slots are in use? Paralleling supplies allows addition of power on an as-needed basis.

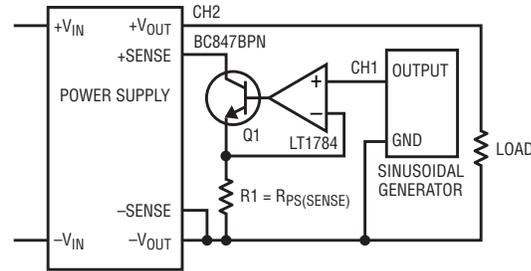


Figure 1. Power supply closed-loop Bode plot measurement block diagram

- ❑ **Redundancy.** These systems, often called N + 1 redundant, use a number of small supplies where N units are needed to power the load, but a “+1” supply is added for redundancy. The theory is, if one supply fails, N units remain to carry the load.
- ❑ **Efficiency.** If the power system must support widely ranging loads, efficiency can be optimized by adjusting the number of operating supplies to the load.

the output current of each supply must be proportional to the rated supply power.

The LTC4350 performs this function. It forces multiple, paralleled power supplies to share current. The concept behind a LTC4350-based load share controller is simple: a single, overall voltage loop controls the common output while each power converter is controlled by a local current loop and contributes current in the common output. Even so, such a multi-loop feedback system requires careful design.

Active control is achieved by sinking additional current from the +SENSE pin found on many common converter modules, and fooling the converter into believing the output voltage is something different than what it would otherwise detect. Increasing this current causes the output to rise; decreasing it causes the output to fall. Thus the LTC4350 has a means of modulating the output voltage, thereby controlling the companion converter’s contribution to the system.

The LTC4350 Hot Swap and load share controller is a powerful tool for developing high availability redundant and load sharing power supply systems.

It has the unique ability to work with supplies with any output stage topology, including output stages using synchronous rectification.

AC Analysis

The design of a current sharing power system involves not only the simple matter of DC operating conditions, but also AC analysis. This article covers the AC design aspects of an LTC4350-based load share system.

The design goal is to build a stable system with maximum bandwidth,

The key to parallel operation is balancing the output current of each supply, so that all are equally loaded if the supplies are identical. If individual supplies with different power ratings are combined for parallel operation,

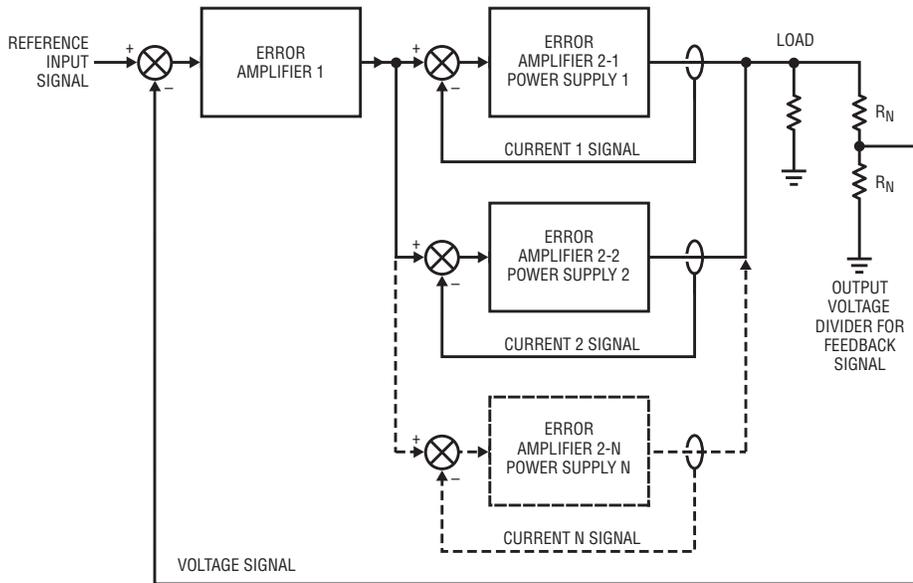


Figure 2. Power system control loop

either synchronize the activation of the LTC4350 controller current share ability with the MOSFET switch turn-on process, or disable synchronous rectification before the LTC4350 load share capability is activated. Detailed descriptions of those actions are presented below.

The power supply output voltage ramp-up behavior during turn on should be checked to eliminate LTC4350 operation in the area where output voltage slew rate experiences significant changes. An undervoltage protection circuit, which is connected with pin 1, performs this function.

Unified Approach to Compensation Components Parameters Evaluation

A power system with K power supplies operating in parallel is a K + 1 loop control system. This system has one voltage loop, which is the highest bandwidth loop, and K current loops. These K current loops work with a common input command signal and individual feedback current signals. All current loops operate in parallel. A block diagram of the control loops is shown in Figure 2.

There are two restrictions on loop bandwidth. All current loops must have equal bandwidths. The voltage loop bandwidth must be wider than any current loop bandwidth to eliminate current oscillation between power supplies.

LTC4350 error amplifiers EA1 and EA2 are transconductance operational amplifiers. This restricts compensation circuit transfer functions to two types: pole or a pole and zero with $T_{POLE} > T_{ZERO}$. A compensation circuit of one capacitor C_C implements a transfer function

$$\frac{G_{EA}}{T_{POLE}S + 1} \quad [1]$$

where G_{EA} is the error amplifier voltage gain, $g_m R_O$, and,

$$T_{POLE} = \frac{1}{2\pi R_O C_C}$$

R_O is the internal error amplifier's output impedance.

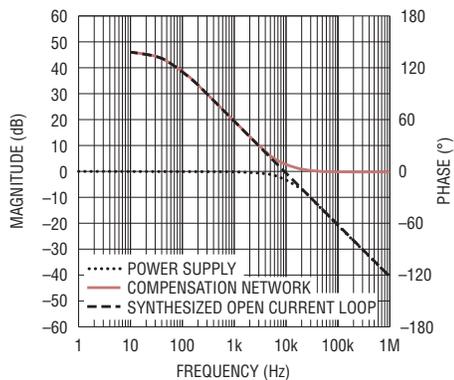


Figure 3. Current loop Bode design with power supply having first order transfer function

with good transient response, and to preserve as much of the inherent performance of the individual power supply as possible.

As each supply in a power system is a fixed configuration component, knowledge of its main characteristics is indispensable for control system design. Among the power supply characteristics essential for design purposes are power supply bandwidth, output stage topology and power supply output voltage ramp up behavior.

Figures for power supply bandwidth can be obtained directly from the power supply manufacturer or measured in the lab. One way to experimentally measure bandwidth is to use a simple driver, a sine wave generator and an oscilloscope. Figure 1 shows the block

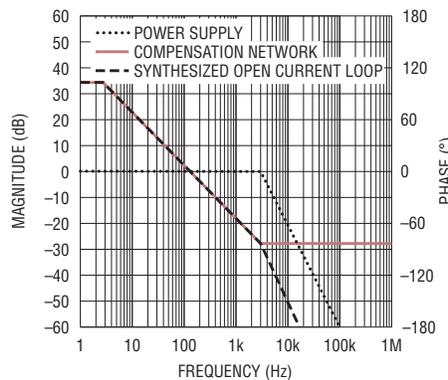


Figure 4. Current loop synthesis with 0,-1,-2 shape

diagram for this measurement. Scope probes are connected to the generator output and power supply output. A power supply Bode plot can be obtained significantly faster using special equipment for frequency response measurement, such as a VENABLE Frequency Response Analyzer or AP's Analog Network Analyzer. Power supply bandwidth should be measured with 90%–100% load.

The power supply output stage topology should be taken into account when designing the load share power system. If it is a synchronously rectified power supply output stage, it is able to provide bidirectional energy flow and as a result the power supply can operate in the second quadrant and sink current. In this case one of two special measures should be taken:

If a compensation circuit has capacitor C_C and resistor R_C series connected, it implements a transfer function

$$\frac{G_{EA}(T_{ZERO}S + 1)}{T_{POLE}S + 1} \quad [2]$$

where

$$T_{ZERO} = \frac{1}{2\pi R_C C_C}$$

The equations shown are based on the assumption that $R_O \gg R_C$.

Current Control Loop Synthesis and Compensation Component Calculation

The Bode amplitude characteristic slope is defined by the integer K (0, 1, 2, etc.) to express the slope

$$SLOPE = (-20 \frac{db}{dec} \cdot K)$$

As an outer loop, the voltage loop must have larger bandwidth than the inner current loop. The closed current loop Bode plot should be shaped as 0,-1 or 0,-1,-2 with the -1 segment at least 1.4 decades long.

1. If the power supply Bode amplitude characteristic has shape 0,-1 or 0,-1,-2, and the -1 segment is 1.4 decades long, the current loop error amplifier compensation network allows for a current loop bandwidth equal to the power supply bandwidth. This can be achieved by tailoring the current loop compensation network so that its zero frequency is equal to the main power supply pole frequency. Figure 3 demonstrates this approach.
2. If the power supply Bode amplitude characteristic has shape 0,-1,-2, and the -1 segment is shorter than 1.4 decades—or at the extreme, the shape is 0,-2—shifting the current loop crossover frequency to the left (this reduces the current loop bandwidth to below the power supply bandwidth) makes it possible to achieve a 0,-1,-2 closed current loop shape with the -1 segment covering least 1.4 decades. In the extreme case when

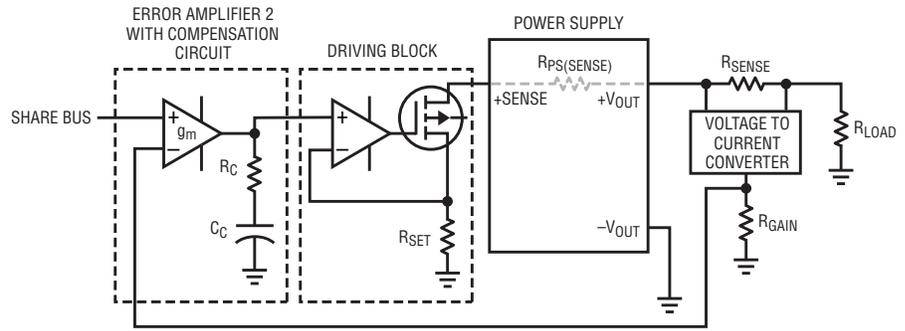


Figure 5. Current loop functional block diagram

the power supply closed loop frequency response characteristic is 0,-2, placing a compensation network zero exactly at the coordinate where the amplitude is -28db and the frequency is the power supply bandwidth, and placing the pole value so that the crossover frequency is 25x lower than the power supply bandwidth achieves the desired result. Figure 4 illustrates synthesis of a current loop with shape 0,-1,-2.

A current loop block diagram and current loop control diagram are shown in Figures 5 and 6.

Current open-loop gain is proportional to load and it must be calculated at the power supply's maximum available current. At maximum load current (I_{LIMIT}), an additional 1V output on the

power supply produces additional current in the load as given by

$$\Delta I = \frac{I_{LIMIT}}{V_{OUT}}$$

and produces a corresponding signal on the sense resistor as follows

$$\Delta V_{SENSE} = \frac{I_{LIMIT} R_{SENSE}}{V_{OUT}}$$

Current open-loop gain equals

$$G_{CO} = G_{EA2} \cdot G_{DB} \cdot G_{CSA}$$

where G_{EA2} is the error amplifier EA2 gain, G_{DB} is the driving block gain, and G_{CSA} is the current sense amplifier gain, which is given by

$$G_{CSA} = \frac{I_{LIMIT} R_{SENSE}}{V_{OUT}} \cdot 10^{-3} \cdot R_{GAIN}$$

It should be noted that R_{SENSE} is a resistor connecting the power sup-

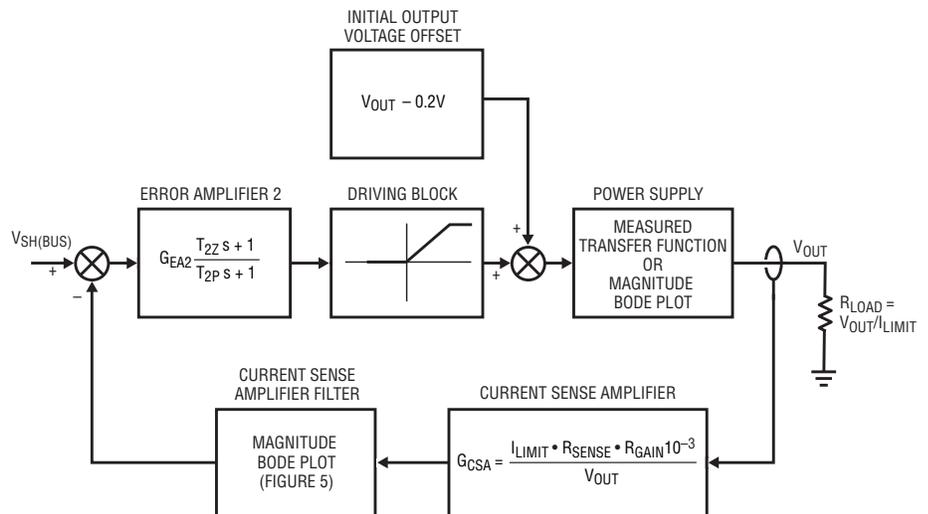


Figure 6. Current loop control block diagram

ply output to the load. Driving block gain is

$$G_{DB} = \frac{R_{PS(SENSE)}}{R_{SET}}$$

where $R_{PS(SENSE)}$ is a power supply resistor value and R_{SET} is a resistor connected to the LTC4350 SET pin.

The LTC4350's voltage-to-current converter in the current sensing block has a flat response from low frequencies up to 10kHz, where a low frequency pass filter is implemented.

Measured Error Amplifier 2 voltage gain is 500–1000.

Voltage Control Loop Synthesis and Compensation Component Calculation

The voltage loop forward path contains an error amplifier (Error Amplifier 1) and the current loop, and the feedback path contains an output voltage divider. A control diagram for the voltage loop is shown in Figure 7.

Measured Error Amplifier 1 voltage gain is 1800–2200.

Bode design for the voltage loop is demonstrated in Figures 8 and 9. The first plot explains the design when the current closed-loop magnitude response has shape 0,-1. To have a voltage loop crossover frequency 6 to 7 times wider than the current closed-loop bandwidth, the compensation should have a zero at the same frequency as the bandwidth, but the magnitude of the gain must be 15dB - 17dB [$20\log(6) = 15.5$; $20\log(7) = 16.9$]. The pole frequency equals

$$f_{1(POLE)} = (3 - 6) \frac{f_{1(ZERO)}}{G_{V(OPEN)}}$$

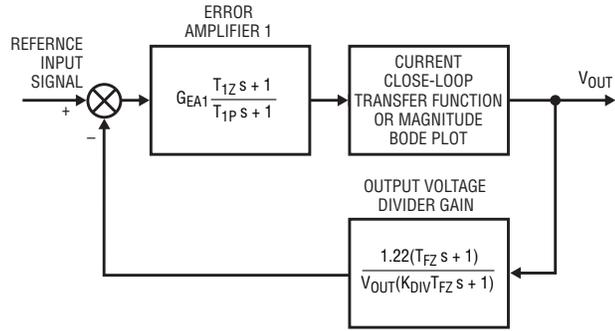


Figure 7. Voltage loop control block diagram

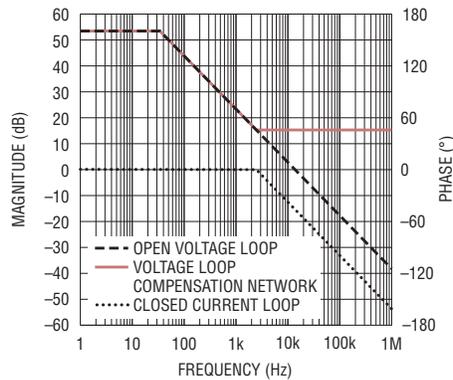


Figure 8. Voltage loop Bode design with current closed loop having 0,-1 shape

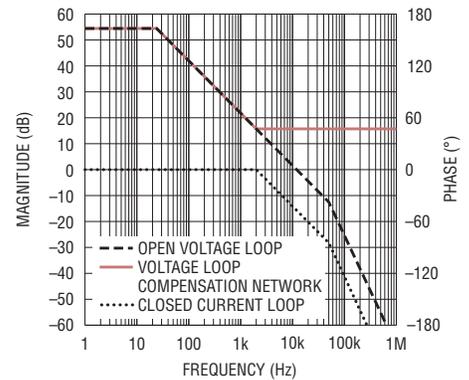


Figure 9. Voltage loop Bode design with closed current loop having 0,-1,-2 shape

where $G_{V(OPEN)}$ is the voltage open-loop gain.

The same relationship between voltage loop crossover frequency and the current closed-loop bandwidth should hold in the second case, when the current closed-loop magnitude response is shaped as 0,-1,-2. The compensation provided should be the same as the first case, as shown in Figure 9.

An additional option exists for improvement of the voltage open-loop magnitude response by placing in the feedback path lead compensation

with lead ratio $1.22/V_{OUT}$. Shunting the top resistor in the output voltage divider with a capacitor implements the transfer function

$$\frac{T_{f(ZERO)}S + 1}{T_{f(POLE)}S + 1} \cdot \frac{1.22}{V_{OUT}}$$

where

$$T_{f(ZERO)} = R_{f1}C_f$$

and

$$T_{f(POLE)} = T_{f(ZERO)} \cdot \frac{V_{OUT}}{1.22}$$

R_{f1} is the top resistor in the voltage divider and C_f is the shunting capacitor. This compensation allows bending of the magnitude response and gives a slope of -20db/dec around the crossover frequency in the restricted frequency area. It is the maximum area for a 12V system; it takes

$$20\log \frac{12}{1.22} = 19.85\text{db}$$

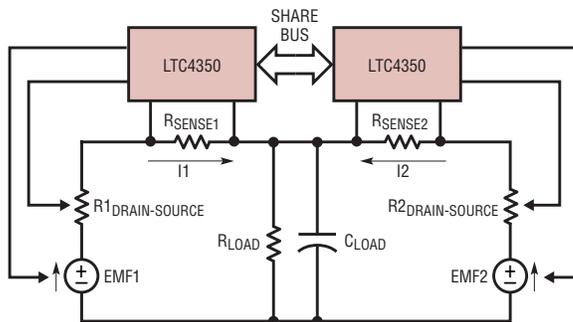


Figure 10. Output power stage equivalent circuitry. The power supply output characteristic exists in the second quadrant

continued on page 16

output on separate parallel busses or multiplexed onto a single parallel bus to save processor pins.

Interfacing to the Analog Inputs

The analog inputs of the LTM9002 present a differential 50Ω resistive input impedance, which in most cases exactly matches the signal path. The input common mode level should be approximately $V_{CC}/2$. Traditionally, the input of an ADC requires considerable care in terms of drive current, settling time and response to the nonlinear characteristics of sample-and-hold switching. For lowest distortion performance, the common mode level at the ADC inputs must be optimized for the particular ADC front-end; for best signal-to-noise (SNR) performance, the signal swing must utilize the maximize ADC input range. All this is taken care of within the LTM9002.

Interfacing to the Digital Outputs

The LTM9002 uses standard CMOS output buffers that switch from OV_{DD}

to OGND. OV_{DD} can range from 0.5V to 3.6V, accommodating many different logic families and OGND can be as high as 1V. Because the LTM9002 supplies are internally bypassed, no local supply bypass capacitors are required. The power supply for the digital output buffers should be tied to the same supply that powers the logic being driven. For example, if the converter drives a DSP powered by a 1.8V supply, then OV_{DD} should be tied to that same 1.8V supply. Lower OV_{DD} voltages also help reduce interference from the digital outputs to the analog or clock circuitry. OV_{DD} and OGND are isolated from the ADC power and ground. An internal resistor in series with the output makes the output appear as 50Ω to external circuitry and may eliminate the need for external damping resistors.

Power Supplies and Bypassing

The LTM9002 requires a 3.0V supply. To optimize performance for each block within the LTM9002, multiple supply pins are used. Internally, each supply is bypassed to ground very close to the die to minimize coupled noise.

A common problem with traditional ADC board layouts is long traces from the bypass capacitors to the ADC degrade system performance. The bare die construction with internal bypass capacitors in the LTM9002 provides the closest possible decoupling and eliminates the need for external bypass capacitors.

Conclusion

Multichannel ADC applications need good channel-to-channel matching and isolation without consuming valuable board space. Driving high performance ADCs is challenging enough without the matching, isolation and board space constraints. The LTM9002 integrated dual IF/baseband receiver subsystem manages to address all of these requirements while eliminating the design task of mating an ADC and its driver. By integrating the passive filtering and supply bypassing, the overall size is dramatically smaller than otherwise possible with discrete implementations. The LTM9002's μ Module packaging is itself developed to maximize the performance of the integrated components. 

LTC4350, continued from page 9

Specifics of Power System Design With a Bidirectional Energy Flow Power Supply

Certain switcher topologies, such as a synchronously rectified buck converter, permit large, uncontrolled reverse current if the output voltage is forced to a potential that is higher than the regulation point. In addition, an unwelcome transient can occur when one LTC4350 power channel is added to an operating system. Due to the difference between the initial power supply output voltage and the operating output voltage (usually 200mV–300mV), significant negative current can be induced in the newly added power supply. This current can disable the LTC4350 if the voltage drop at R_{SENSE} exceeds 50mV. After the negative current drops, the LTC4350 goes into its initial start-up cycle and the process may repeat indefinitely. This current can also damage the

power supply, as it does not have the ability to transform energy to the primary side.

An equivalent output power stage circuit that exemplifies this case is shown in Figure 10.

To reduce or eliminate negative current, it is necessary to reduce the difference between voltages when the MOSFET switch is first turned on. The newly activated power supply output voltage starts to increase when the LTC4350 load share capability is brought into operation. The LTC4350 is designed to launch the load share mechanism when the gate pin voltage exceeds V_{CC} by 4V but the MOSFET's gate threshold is in the range of 1V to 5.5V. To synchronize both events, activating load share capability and turning on the power switch, the MOSFET threshold voltage must be higher than or equal to 4V. This is easily satisfied by using a sub-logic

level MOSFET and placing a low knee current Zener diode (Central Semiconductor's CMPZ4676-CMPZ4682) in the MOSFET gate circuit.

An alternative solution involves disabling synchronized rectification until the LTC4350 STATUS pin signal is low and load share capability is active, but this method is restricted by the power supply controller's ability to power up non-synchronously in a condition of unidirectional energy flow.

Conclusion

The calculations and methods described here show how the LTC4350 can be used to build a stable and accurate load share power system with any kind of power supply, including a mix of power modules. The LTC4350 also has the unique feature of operating with bidirectional power flow converters. 