A J-FET’s self-biasing characteristic can be utilized to construct a DC/DC converter powered from as little as 300mV. Solar cells, thermopiles and single stage fuel cells, all with outputs below 600mV, are typical power sources for such a converter.

Figure 1 shows the zero volt biased JFET I-V plot, which demonstrates a current of 10mA at 100mV and rises above 40mA at 500mV. This characteristic enables construction of a DC/DC converter powered from 300mV supply.

Figure 2 shows the circuit. Q1 and T1 form an oscillator with T1’s secondary providing regenerative feedback to Q1’s gate. When power is applied, Q1’s gate is at zero volts and its drain conducts current via T1’s primary. T1’s phase inverting secondary responds by going negative at Q1’s gate, turning it off. T1’s primary current ceases, its secondary collapses and oscillation commences. T1’s primary action causes positive going “flyback” events at Q1’s drain, which are rectified and filtered. Q2’s approximately 2V turning on potential isolates the load, aiding start-up. When Q2 turns on, circuit output heads towards 5V. C1, powered from Q2’s source, enforces output regulation by comparing a portion of the output with its internal voltage reference. C1’s switched output controls Q1’s on-time via Q3, forming a control loop.

Waveforms for the circuit include the AC coupled output (Figure 3, trace A), C1’s output (trace B) and Q1’s drain flyback events (trace C). When the output drops below 5V, C1 goes low, turning on Q1. Q1’s resultant flyback events continue until the 5V output is restored. This pattern repeats, maintaining the output.

The 5V output can supply up to 2mA, sufficient to power circuitry or supply bias to a higher power switching regulator when more current is required. Figure 4 plots minimum input voltage vs output current over a range of loads.

Figure 3 shows the circuit operations. VOUT decays, C1 (trace B) switches, allowing Q1 to oscillate. Resultant flyback events at Q1 drain (trace C) restore supply output.

Figure 4 plots minimum input voltage vs output current over a range of loads.

Figure 5 illustrates the quiescent current control circuitry. With quiescent control circuitry, the output voltage can be regulated down to approximately 2mA, although required VOUT rises to 500mV. Without quiescent control circuitry, the output voltage drops significantly with load.

Figure 5 shows the quiescent current control circuitry.

**Table:**

<table>
<thead>
<tr>
<th>Minimum Input Voltage (V)</th>
<th>Output Current (µA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.3V to 1.6V</td>
<td>100mA/DIV</td>
</tr>
<tr>
<td>0.3V</td>
<td>10mA/DIV</td>
</tr>
<tr>
<td>0.3V</td>
<td>1mA/DIV</td>
</tr>
</tbody>
</table>

**Figure 3:** J-FET based DC/DC converter waveforms. When output decays, C1 switches, allowing Q1 to oscillate. Resultant flyback events at Q1 drain restore supply output.

**Figure 4:** J-FET based DC/DC converter of Figure 2 starts and runs into 100µA load at VIN = 275mV. Regulation to 2mA is possible, although required VIN rises to 500mV.

**Figure 5:** Quiescent current control circuitry of Figure 5 slightly increases input voltage required to support load at VIN < 500mV.
Q3’s shunt control of Q1 is simple and effective, but results in a 25mA quiescent current drain. Figure 5’s modifications reduce this figure to 1mA by series switching T1’s secondary. Here, Q3 switches series-connected Q4, more efficiently controlling Q1’s gate drive. Negative turn-off bias for Q4 is bootstrapped from T1’s secondary; the 6.8V zener holds off bias supply loading during initial power application, aiding start-up. Figure 4 shows minimal penalty imposed by the added quiescent current control circuitry.}

**Output Disconnect**

In a standard boost regulator, the inductor and Schottky diode provide a DC current path from the input to the output, even when the regulator is shut down. Any load at the output when the chip is shut down can continue to drain the $V_{IN}$ source. The LT3487 addresses this issue with an on-chip output disconnect. The output disconnect is a PNP pass transistor that eliminates the DC loss path. The pass transistor is controlled by a circuit that varies its base current to keep it at the edge of saturation, yielding the best compromise between voltage drop across the PNP and quiescent current.

The disconnect in the LT3487 can support loads of 50mA with a $V_{CE}$ of less than 210mV.

**$V_{BAT}$ Pin**

The $V_{BAT}$ pin is an innovation that allows output disconnect operation in a wide range of applications. $V_{BAT}$ monitors the voltage at the input of the boost inductor and allows the positive output to stay active until the CAP node falls to 1.2V above $V_{BAT}$. This ensures that output disconnect continues operating even after the part goes into shutdown. Since output disconnect continues to work, the positive output doesn’t fall sharply to ground before the negative bias discharges. The $V_{BAT}$ pin allows the inductors to be powered from a different source than $V_{IN}$ while still maintaining the disconnect operation. This can be useful in a system using a 2-cell supply where a low voltage boost provides 3.3V for the $V_{IN}$ supply. By connecting $V_{BAT}$ as well as the inductors to the 2-cell supply, the positive output is able to stay on as long as possible when the part goes into shutdown.

**Applications**

The LT3487 can be used in a CCD bias as well as other applications that require a positive and negative bias such as ±12V data acquisition systems. The boost channel can produce voltages up to 30V as long as the part can meet the required duty cycle. Similarly, the inverting channel can produce voltages down to –30V. This high voltage capability allows the LT3487 to be used in many LCD applications.

**Conclusion**

The LT3487 simplifies and shrinks CCD bias supplies without compromising on performance or features. The soft-start and output disconnect features ensure that the input battery doesn’t encounter current spikes or shutdown leakage. The high current capability satiates even the most power-hungry video applications.