

# J-FET-Based DC/DC Converter Starts and Runs from 300mV Supply

by Jim Williams

A J-FET's self-biasing characteristic can be utilized to construct a DC/DC converter powered from as little as 300mV. Solar cells, thermopiles and single stage fuel cells, all with outputs below 600mV, are typical power sources for such a converter.

Figure 1, an N-channel J-FET I-V plot, shows drain-source conduction under zero bias (gate and source tied together) conditions. This property can be exploited to produce a self-starting DC/DC converter that runs from 0.3V to 1.6V inputs.

Figure 2 shows the circuit. Q1 and T1 form an oscillator with T1's secondary providing regenerative feedback to Q1's gate. When power is applied, Q1's gate is at zero volts and its drain conducts current via T1's primary. T1's phase inverting secondary responds by going negative at Q1's gate, turning it off. T1's primary current ceases, its secondary collapses and oscillation commences. T1's primary action causes positive going "flyback" events

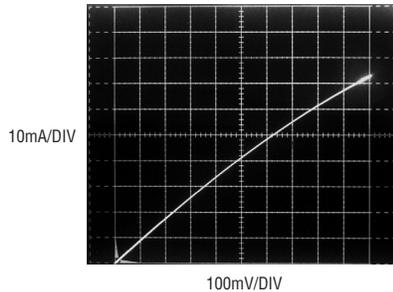


Figure 1. Zero volt biased JFET I-V curve shows 10mA conduction at 100mV, rising above 40mA at 500mV. Characteristic enables construction of DC/DC converter powered from 300mV supply.

at Q1's drain, which are rectified and filtered. Q2's approximately 2V turn-on potential isolates the load, aiding start-up. When Q2 turns on, circuit output heads towards 5V. C1, powered from Q2's source, enforces output regulation by comparing a portion of the output with its internal voltage reference. C1's switched output controls Q1's on-time via Q3, forming a control loop.

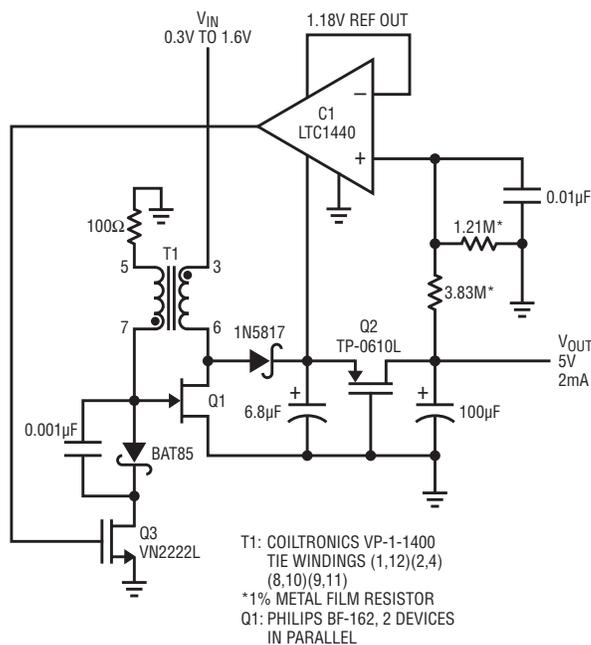


Figure 2. J-FET based DC/DC converter runs from 300mV input. Q1-T1 oscillator output is rectified and filtered. Load is isolated until Q2 source arrives at approximately 2V, aiding start-up. Comparator and Q3 close loop around oscillator, controlling Q1's on-time to stabilize 5V output.

Waveforms for the circuit include the AC coupled output (Figure 3, trace A), C1's output (trace B) and Q1's drain flyback events (trace C). When the output drops below 5V, C1 goes low, turning on Q1. Q1's resultant flyback events continue until the 5V output is restored. This pattern repeats, maintaining the output.

The 5V output can supply up to 2mA, sufficient to power circuitry or supply bias to a higher power switching regulator when more current is required. The circuit will start into loads of 300μA at 300mV input; 2mA loading requires a 475mV supply. Figure 4 plots minimum input voltage vs output current over a range of loads.

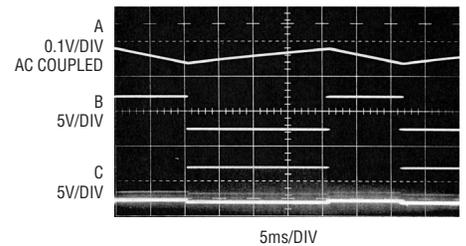


Figure 3. J-FET based DC/DC converter waveforms. When supply output (trace A) decays, C1 (trace B) switches, allowing Q1 to oscillate. Resultant flyback events at Q1 drain (trace C) restore supply output.

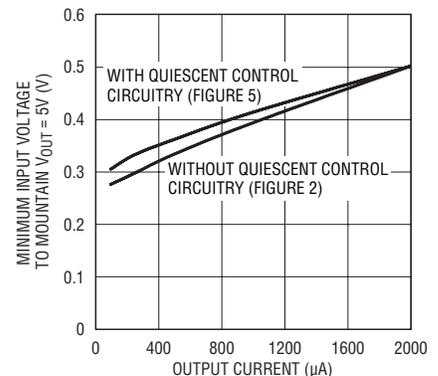


Figure 4. J-FET based DC/DC converter of Figure 2 starts and runs into 100μA load at V<sub>IN</sub> = 275mV. Regulation to 2mA is possible, although required V<sub>IN</sub> rises to 500mV. Quiescent current control circuitry of Figure 5 slightly increases input voltage required to support load at V<sub>IN</sub> < 500mV.

