

up. When it rises above 1.236V, the glitch filter trips the ECB. The GATE pin is immediately pulled to ground and the $\overline{\text{FAULT}}$ pin goes low.

Electronic Circuit Breaker

The Electronic Circuit Breaker (ECB) can be tripped by an overcurrent fault, a power good timeout fault or by a glitch filter fault. When the ECB trips, the GATE pin is pulled down to ground immediately to disconnect the board from the backplane supply. The $\overline{\text{FAULT}}$ pin is pulled low whenever the ECB trips. In order to reconnect the board, the ON pin must be taken low for at least 120 μ s to reset the ECB or the V_{CC} must be below 2.2V for more than 30 μ s.

Overcurrent Protection

The load current is sensed by monitoring the voltage across an external sense resistor (R_{SENSE} in Figure 1). During power-up, a soft-start circuit limits the load current to $50\text{mV}/R_{\text{SENSE}}$. After normal power-up, 2 comparators, FASTCOMP and SLOWCOMP, monitor the load current. FASTCOMP trips the ECB if the load current exceeds $150\text{mV}/R_{\text{SENSE}}$ for 500ns and protects the external MOSFET and load against fast and large overcurrent conditions. SLOWCOMP trips the ECB if the load current exceeds $50\text{mV}/R_{\text{SENSE}}$ for more than 18 μ s.

Typical Application

Figure 1 shows LTC1727-2.5 triple supply monitor providing three comparators to monitor the voltage at the V_{CCA} , V_{CC3} and V_{CC25} pins. Each comparator responds to a 10% overdrive in 50 μ s and exhibits a response time that decreases with overdrive. With a 1% overdrive, the response slows to 150 μ s. The maximum trip point of each comparator is -5% for V_{CC3} and V_{CC25} and varies with R5 and R6 for V_{CCA} . Setting R5 to 11.8k and R6 to 3.01k sets the trip-point for the V_{CCA} comparator to 4.75V or 5V-5%. When any of the three monitored supplies are below -5% for about 60 μ s, the corresponding open drain output COMP3, COMP25 or COMPA is pulled

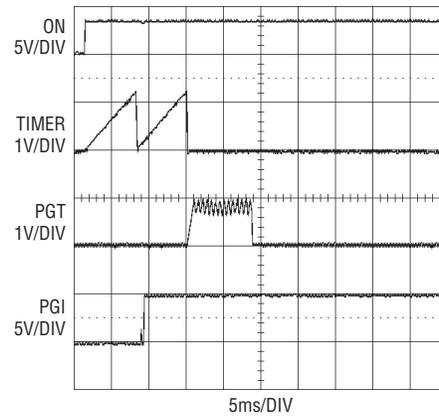


Figure 2. Normal power-up sequence (no load)

low. In Figure 1, all three open drain outputs are shorted to the PGI pin of the LTC4212 and share a single pull-up resistor, R4.

The LT1963-2.5 and LT1963-3.3 are fast transient response LDO regulators that can supply 1.5A of output current at voltages of 2.5V (+3%, -3.5%) and 3.3V (\pm 3%) respectively. A minimum output capacitor of 10 μ F (ESR of 3 Ω or less) is needed to prevent oscillations, and larger capacitors may be required to limit ripple or improve transient response with large transient loads.

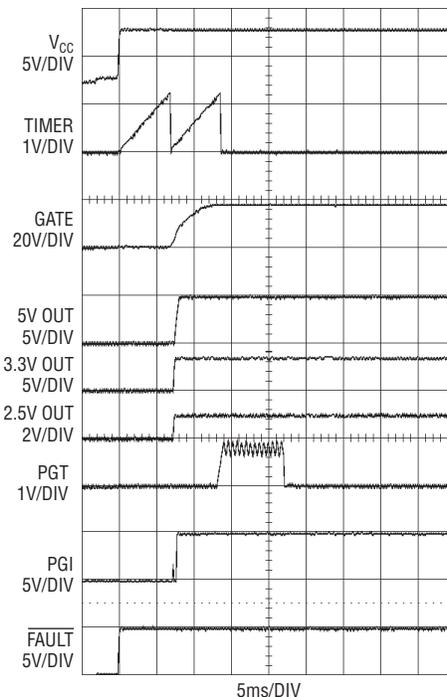


Figure 3. Power-up with load

Normal Power-Up Sequence

Figure 2 shows a normal power-up sequence with unloaded 2.5V, 3.3V and 5V outputs. When V_{CC} rises above 2.2V and the ON pin is greater than 1.316V, the LTC4212 starts the 1st timing cycle. A 2 μ A current source charges an external capacitor (C_{TIMER}) connected from the TIMER pin to ground. When V_{TIMER} rises above 1.236V, the TIMER pin is pulled immediately to ground and C_{TIMER} is discharged. The second timing cycle is started and FASTCOMP is enabled.

During the second timing cycle, a soft-start circuit in the LTC4212 servos the GATE pin to regulate the inrush current at $50\text{mV}/R_{\text{SENSE}}$. The 2 μ A current source is re-enabled to charge C_{TIMER} . From the start of the 2nd cycle, the GATE rises to its final value in around 7ms. The outputs of the linear regulators rise up in 1ms. At the end of the second timing cycle (when V_{TIMER} rises above 1.236V again), the soft-start circuit is disabled and a 10 μ A current source continues to pull-up the GATE pin. At the same time, SLOWCOMP is enabled, the TIMER pin is pulled back to ground and the LTC4212 starts the power good timer. At timeout, the PGI pin is sampled. In Figure 2, PGI goes high (>1.236V) well before timeout and the board remains powered up as is normal. Since the PGI pin is only sampled at timeout, any transients at the PGI pin during supply ramping are ignored.

Figure 3 shows a normal power-up sequence with the 2.5V and 3.3V outputs loaded with 1A.

Power-Up with Fault Sequence

Figure 4 shows power-up with a short at the 5V board supply output, V_{CCA} . During the 2nd timing cycle, the gate voltage ramps up initially to the point where the FET just turns on. After that it flattens out due to action of the soft-start circuit to limit the load current to $50\text{mV}/R_{\text{SENSE}}$ or roughly 7A. The V_{CC} backplane supply dips 0.5V due to the 7A flowing in the interconnection to the 5V, 10A limited supply. At the end of the 2nd cycle, the soft-start circuit is replaced with a 10 μ A pull-up current

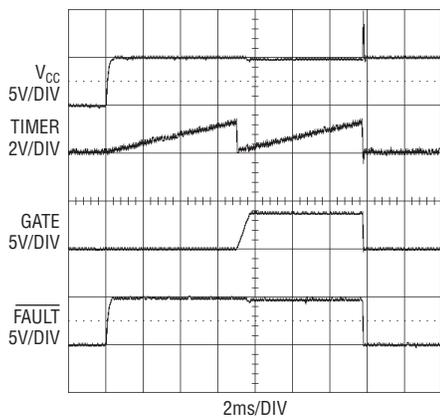


Figure 4. Power-up with the 5V output shorted to GND

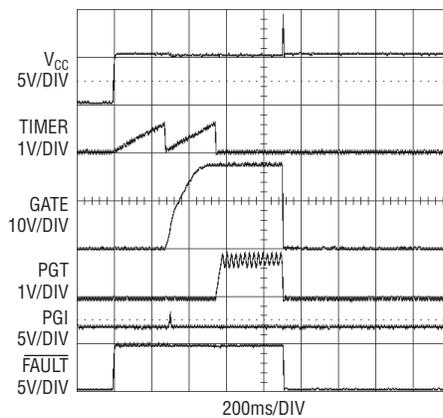


Figure 5. Power-up with the 3.3V output shorted to GND

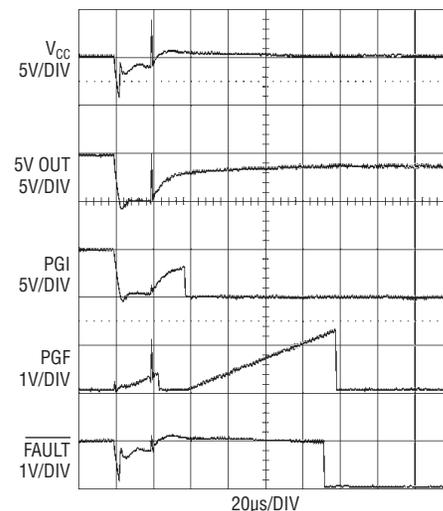


Figure 6. Glitch filter operation

source. This ramps the gate of the FET up and the load current rises until the SLOWCOMP trips the ECB. The gate voltage pulls down in 1µs to 2µs when the fast pulldown circuit is activated. Stray inductance causes the V_{CC} supply to spike when the load current is terminated. The power good timer and glitch filter are disabled when the ECB has been tripped.

If any of the LDO outputs are shorted to ground, the short circuit protection in the LDO reduces the fault current and the board does not latch off after the second timing cycle. As shown in Figure 5, the power good timer samples the PGI pin at timeout and trips the ECB since PGI is low. The GATE pin is pulled to ground immediately to disconnect the board from the backplane supply.

Figure 6 shows the response of the glitch filter to a 20µs overload at the

5V output after normal power-up. The comparators in the LTC1727-2.5 take PGI low whenever the 5V supply or any of the LDO outputs drop below their lower thresholds. The glitch filter capacitor (C_{PGF}) is charged by a 5µA pull-up current source whenever PGI goes low. The first PGF ramp is due to the 20µs overload but V_{PGF} does not ramp above 1.236V. The second pulse is a result of the time it takes the 5V linear regulator to recover from the over load and is long enough for V_{PGF} to ramp above 1.236V, causing the glitch filter to trip the ECB. The GATE pin is pulled immediately to ground to disconnect the board from the backplane supply. If the PGF pin is tied to ground, the PGF pin remains permanently below 1.236V and the glitch filter is effectively disabled. Tying PGF to ground causes the LTC4212 to ignore a low PGI state after normal power-up.

Interfacing with the \overline{RST} Pin

The PGI pin of the LTC4212 can be connected to the \overline{RST} pin instead of the COMPx pins of the LTC1727-2.5. The \overline{RST} pin is delayed by 200ms compared to the COMPn pins and C_{PGT} must be adjusted to include the 200ms delay for the board to power-up normally. In addition, any transients on the monitored supplies that exceed the response time of the comparators in the LTC1727-2.5 will cause \overline{RST} to go low for at least 200ms. This causes the glitch filter to trip the ECB.

Auto-Retry Application

Figure 7 shows an application that automatically tries to power-up the board after the ECB has been tripped due to a shorted load supply output. This circuit uses the LTC1326-2.5 supply monitor chip and ties its \overline{RST} output

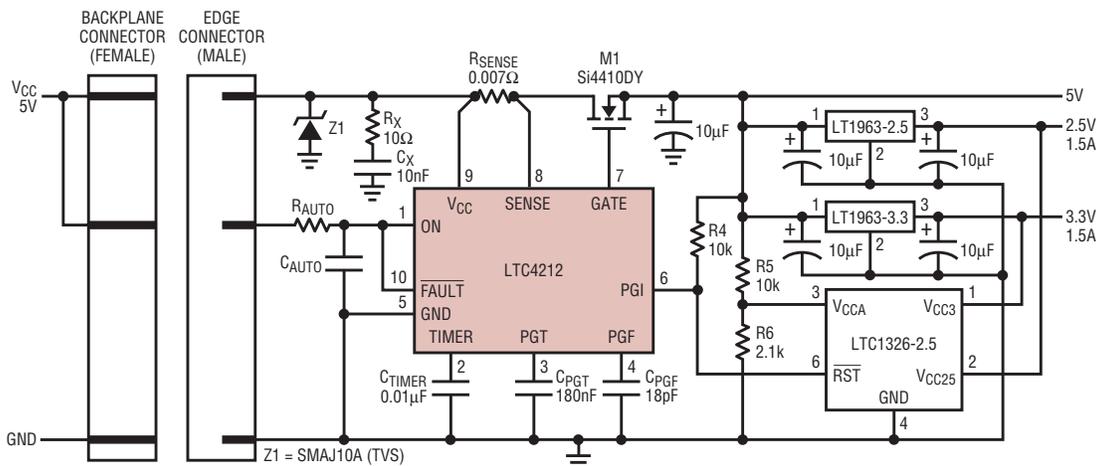


Figure 7. Auto-retry application

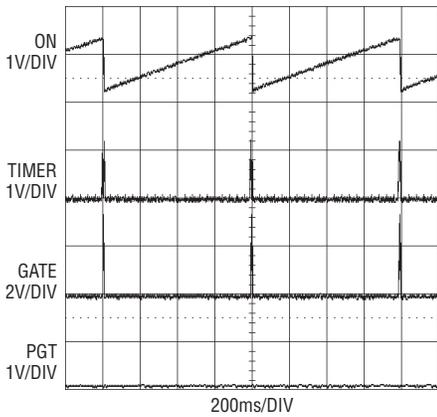


Figure 8. Auto-retry with short at 5V output

to the PGI pin of the LTC4212. The $\overline{\text{RST}}$ signal goes high 200ms after all the monitored voltages rise above the thresholds of the V_{CCA} , V_{CC3} and V_{CC25} comparators in the LTC1326-2.5. The ON pin is shorted to the $\overline{\text{FAULT}}$ pin and is pulled up by a $1\text{M}\Omega$ resistor (R_{AUTO}) to V_{CC} . A $2\mu\text{F}$ capacitor (C_{AUTO}) connected from the lower end of R_{AUTO} to ground sets the auto-retry duty cycle. The LTC4212 will retry as long as the short persists. R_{AUTO} and C_{AUTO} must be selected to keep the duty cycle low in order to prevent overheating in the external N-channel MOSFET.

Figure 8 shows the auto-retry cycle when the 5V output is shorted to ground. SLOWCOMP trips the ECB after the 2nd timing cycle. This causes the $\overline{\text{FAULT}}$ pin to be pulled low by an internal N-channel FET and C_{AUTO} is discharged to ground. The GATE pin is pulled immediately to ground to disconnect the board. Note that in Figure 8, the time-base setting causes the first and second timing cycles to appear as a single spike. When the ON pin goes below its lower threshold of 0.455V (typical) for more than $120\mu\text{s}$, the ECB is reset. The internal N-channel FET at the $\overline{\text{FAULT}}$ pin is switched off and R_{AUTO} starts to charge C_{AUTO} slowly towards V_{CC} .

When the ON pin rises above its upper threshold of 1.316V , the LTC4212 attempts to reconnect the board and start the first timing cycle. With a dead short at the 5V output as in Figure 8, the ECB trips after the second timing cycle when the soft-start circuit is

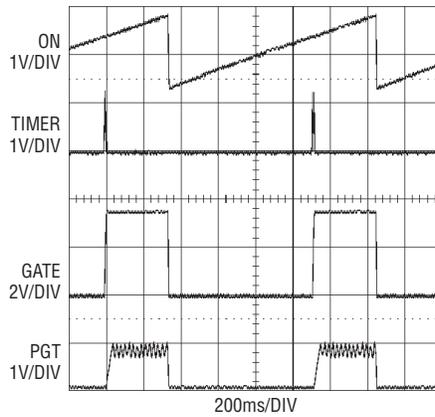


Figure 9. Auto-retry with short at LDO output

disabled and a $10\mu\text{A}$ pull-up current source is connected to the GATE pin. The entire cycle is repeated until the short is removed. The duration of each cycle is dominated by the time needed to charge C_{AUTO} between the lower and the upper threshold voltages of the ON pin. With $R_{\text{AUTO}} = 1\text{M}\Omega$ and $C_{\text{AUTO}} = 2\mu\text{F}$, the cycle time is 800ms. The switch is on for about 6ms giving a duty cycle of 0.75%.

At the end of the 2nd timing cycle, the GATE pin is about 3V due to the action of the soft-start circuit (which limits the current to $50\text{mV}/R_{\text{SENSE}}$) and the presence of the short at the

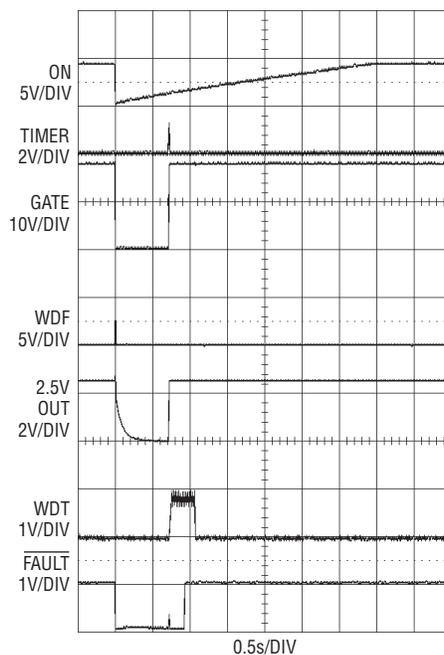


Figure 10. Auto-retry caused by a transient short at the 2.5V output

5V output. The $10\mu\text{A}$ current source takes several milliseconds to ramp up the 3.3nF of GATE pin capacitance. As a result, SLOWCOMP tends to trip the ECB instead of FASTCOMP.

When powering up with a short at the output of either LDO, the short circuit protection in LDO reduces the fault current. At the end of the Power Good timeout period, the PGI pin is still low due to the short circuit. As shown in Figure 9, the external N-channel MOSFET is turned on for a longer part of each auto-retry cycle if the overload is not enough to trip both SLOWCOMP and FASTCOMP. With $R_{\text{AUTO}} = 1\text{M}\Omega$ and $C_{\text{AUTO}} = 2\mu\text{F}$, the duty cycle increases to 29% causing the LT1963-2.5 LDO to heat up to a case temperature of 106°C at an ambient temperature of 25°C . A larger value of C_{AUTO} is required when operating from higher ambient temperatures. The Si4410DY MOSFET does not heat up appreciably due to its low $R_{\text{DS(ON)}}$.

If a transient short at the output of an LDO is long enough to cause the monitoring comparators in the LTC1326-2.5 ($13\mu\text{s}$ typical delay) to switch, the $\overline{\text{RST}}$ output will go low for at least 200ms. As shown in Figure 10, the Power Good glitch filter trips the ECB and initiates an auto-retry cycle.

Conclusion

The LTC4212 simplifies the design of hot swapping boards with multiple power supplies. The status outputs from power supply ICs or supply monitor ICs—such as $\overline{\text{RST}}$, PGOOD and COMPn—are typically open drain outputs and can be connected together and monitored by the PGI pin of the LTC4212. The power good timer automatically disconnects the card from the backplane supply should any of the supplies fail to power-up within the programmed time period. After normal power-up, the glitch filter provides a means to detect out of regulation supplies while rejecting dips that last shorter than a programmable time period. 