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IN THIS ISSUE...

World's Smallest 24-Bit ADC Packs High Accuracy, Ease of Use, into SO-8

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Introduction

Linear Technology enters the delta-sigma[1, 2] analog-to-digital converter market with a tiny, high performance, 24-bit ADC, the LTC2400. The device's superiority to existing delta-sigma ADC's results from the combination of an accurate analog modulator with an innovative new digital architecture. Typically, fine-line, digitally optimized processes are required for a delta-sigma ADC's on-chip digital filter. The resulting ICs have high pin counts, large packages and complex interfaces. The LTC2400's breakthrough in digital filtering allows the use of an analog-optimized process. The result is the smallest (SO-8 package), lowest pin count (8) simplest to use delta-sigma converter on the market. A highly accurate on-chip oscillator, using Linear's high performance CMOS process, sets the digital filter's notch frequency, eliminating the need for an external crystal. Additionally, the part offers exceptional INL, DNL, noise and 50Hz/60Hz rejection. The innovation does not end here; this article will show how performance, ease of use and functionality make this part the new state of the art in high resolution delta-sigma ADCs.

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Overview

The analog modulator is critical to the performance of a delta-sigma ADC. For high DC accuracy, 1st or 2nd order modulators provide insufficient differential nonlinearity (DNL). The LTC2400 achieves optimum DC performance from a 3rd order delta-sigma modulator (see Figure 1). Feedforward compensation and analog processing within the modulator eliminate instability issues associated with high order modulators. The 1-bit ADC and DAC within the modulator guarantee monotonicity and exceptional INL performance of 4ppm.

The output of the delta-sigma modulator is applied to a decimating filter. The sinc[4] filter removes the quantization noise from the modulator output. Additionally, this filter rejects the fundamental frequency and its harmonics. This notch frequency is set by an on-chip oscillator, typically at line frequency for DC applications. The combination of a 4th order sinc filter with a precision thin-film, factory-trimmed oscillator guarantees at least 120dB rejection of line frequency ±2%. Several converters on the market use sinc[3] or sinc[1] filters. Since line frequencies can vary up to 2% over a 24-hour period, converters using these lower order filters cannot achieve 120dB

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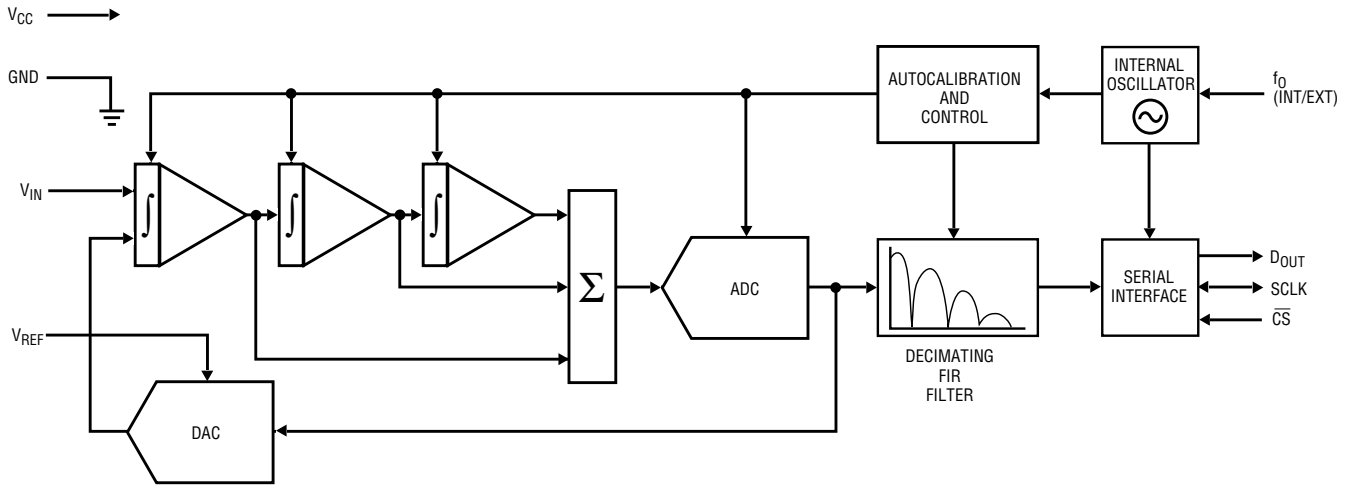

Figure 1. LTC2400 block diagram

LTC2400, continued from page 1

rejection, even with exact external oscillators (refer to Figure 6a).

A simple, SPI-compatible 3-wire interface outputs data with single-cycle settling. This simplifies the user interface by eliminating latency and redundant data normally associated with delta-sigma ADCs. As a black box, the converter resembles traditional, easy-to-use converters.

Performance

Designed on a 2µ, single-metal, analog CMOS process, the LTC2400 is implemented with a die size under 10kmil^2. The key to Linear attaining the nearly impossible is the highly efficient sinc^4 filter. Once the tiny digital circuitry was completed, the analog circuitry was optimized for ultrahigh performance.

The result is 24-bit DNL with no missing codes guaranteed. As shown in Figure 2, the integral nonlinearity is a mere ±2ppm or 0.0002%. This compares favorably with other 24-bit devices' INL performance of 15ppm–30ppm. Transparent to the user, the converter continuously executes self-calibration algorithms automatically adjusting the offset and full-scale. With an initial accuracy of 1ppm, the offset drifts less than 0.01ppm/°C and the full scale drifts less than 0.02ppm/°C (see Figures 3 and 4). Combining these DC parameters with RMS noise performance of 0.3ppm (see Figure 5), the LTC2400 resembles a 6-digit digital voltmeter on a chip.

The modulator consists of operational amplifiers and switched capacitor circuits. Previous delta-sigma converters place limitations on these circuits. Since the LTC2400 was designed on an analog process, these limitations are removed. This allows a power supply range of 2.7V to 5.5V and a reference range of from below 10mV to 90% of V_{CC}. At V_{CC} = 3V, the power consumption is 750µW; it falls to 45µW in power-down mode.

In many applications, the input signal may exceed V_{REF} or fall below ground. Conventional delta-sigma converters are unable to provide the user with any indication of these overrange conditions. The LTC2400 has on-chip overrange circuitry. It continues to output 24-bit valid data over an effective input range of $-12.5\% \times V_{REF}$ to $112.5\% \times V_{REF}$.

One of the main advantages of delta-sigma converters over SAR or flash-type architectures is the inherent rejection of line frequency. In order to achieve good rejection, past delta-sigma converters required an accurate external oscillator or crystal with a precise, uncommon value. The LTC2400 incorporates an on-chip oscillator eliminating the need for

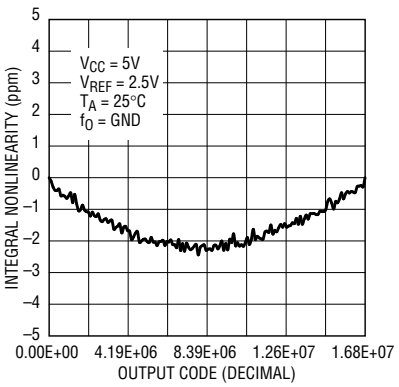

Figure 2. LTC2400 integral nonlinearity error

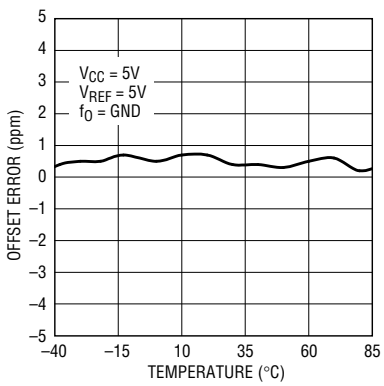

Figure 3. Offset drift

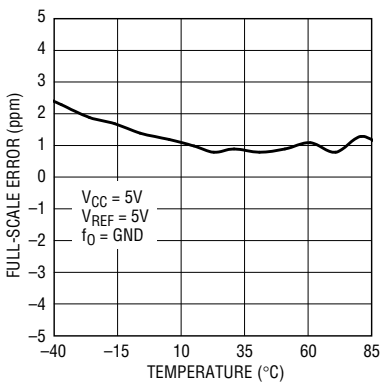

Figure 4. Full-scale drift

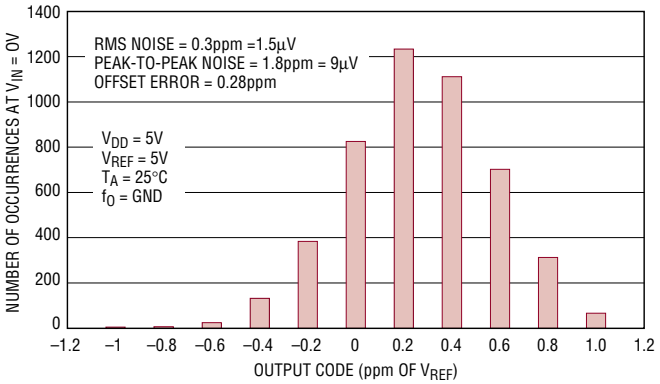

Figure 5. Noise histogram

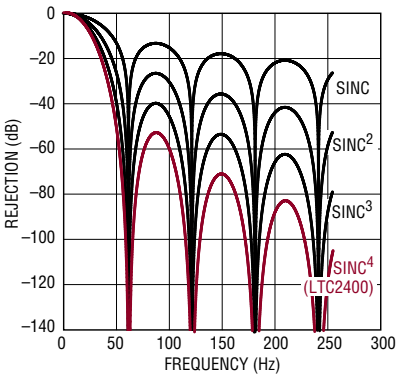

Figure 6a. Filter response vs filter order

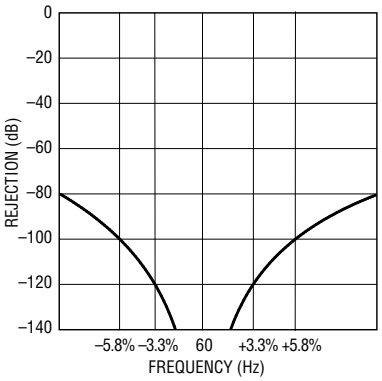

Figure 6b. Filter response at line frequency

external components. The internal oscillator is so precise that the ADC rejects line frequency over a ±2% range, independent of supply or operating temperature (see Figure 6a, where sinc[1], sinc[2] and sinc[3] filters are shown for comparison). Line frequencies of 50Hz or 60Hz are selectable by simply tying the f_O pin to V_{CC} or ground. Other rejection frequencies can be obtained by driving the f_O pin with an external clock.

The converter is so robust that the noise performance and line rejection are insensitive to layout. As shown in Figure 7, large noise errors applied to V_{CC}, V_{REF} or V_{IN} (1.25V_{P-P}, 60Hz, ±2%) have no effect on the ADC's noise and linearity performance.

Ease of Use

At a glance, the LTC2400 looks more like an op amp than a delta-sigma converter. With only eight pins, it's about as easy to use as a common op amp (see Figure 8). Superior noise rejection and internal analog circuitry enable the use of one supply pin, one ground pin and a single-ended input. The internal oscillator eliminates external crystals/capacitors and added device pins. The remaining pins form a standard 3-wire interface, consisting of a three-statable serial data output (D_{OUT}) under the control of a chip select pin ($\overline{CS}$) and a serial data output clock (SCLK).

Applications currently using traditional ADCs can easily migrate to the LTC2400. Single-cycle settling yields a one-to-one correspondence between the start of a conversion and the output word. This allows the user to place a multiplexer in front of the ADC without worrying about latency or data statistically dependent on previous conversion results.

Functionality

Despite its small size and low pin count, the LTC2400 provides many flexible modes of operation. For example, tying $\overline{CS}$ low forces a continuous conversion mode. With $\overline{CS}$ tied high, the device enters a 45µW power-down mode. For applications requiring ultralow power, a capacitor can be tied to $\overline{CS}$. Under this

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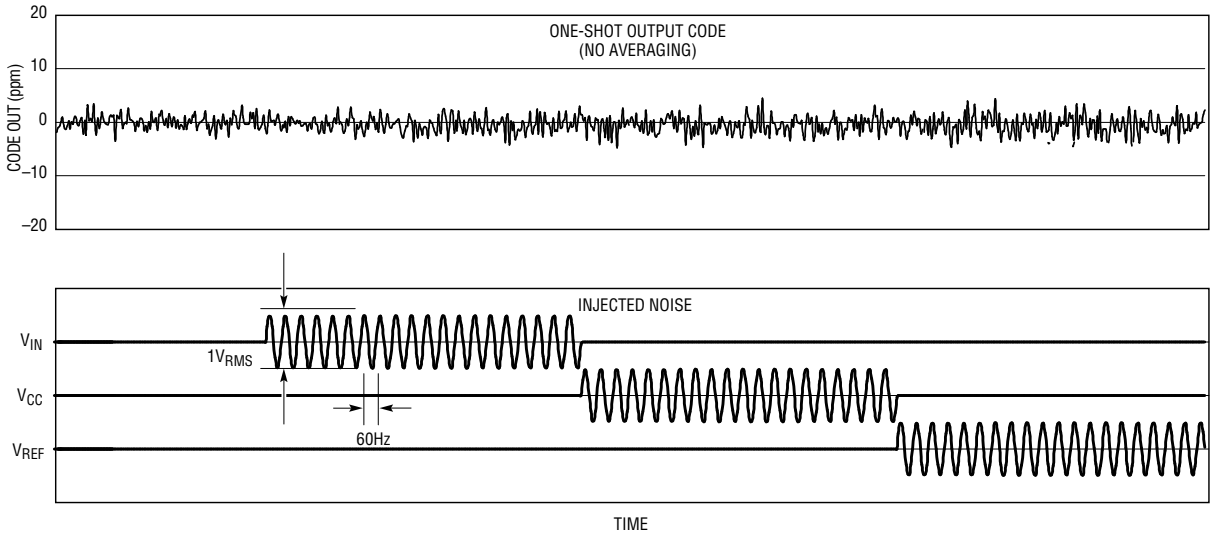

Figure 7. Noise injection

LTC2400, continued from page 4

configuration, the part performs one conversion, then automatically enters the power-down mode. The duration of the power-down mode is proportional to the capacitor value.

While $\overline{CS}$ is held high, the serial data out pin is high impedance. Once $\overline{CS}$ is pulled low, the part begins outputting data under the control of the SCLK pin.

This device can operate with either an internal or external serial clock. If the SCLK pin is left floating, the LTC2400 automatically detects this state and switches to internal clock mode. If the user drives the SCLK pin with his own clock, the part is automatically switched to external clock mode.

Many delta-sigma ADC's on the market include a PGA. These PGAs require that the designer deal with more device pins, status registers and timing sequences. Additionally, they limit the circuit's input range. For example, if the PGA's gain is 256 and the reference is 2.5V the resulting input range is 0mV to 10mV.

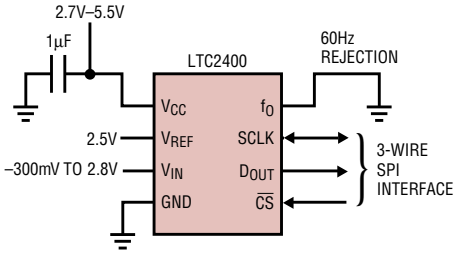

Figure 8. LTC2400 typical application

The LTC2400 provides better noise and TUE (total unadjusted error) performance than previous delta-sigma ADCs; moreover, the user is no longer confined to a 10mV input range. The input can still range between –12.5% × V_{REF} and 112.5% × V_{REF}. The eight MSBs determine the coarse input range. For example, if the eight MSBs = 00h, the input (V_{IN}) is in the range: $0 < V_{IN} < 10mV$, whereas 01h corresponds to $10mV < V_{IN} < 20mV$, and so on. This enables the LTC2400 to directly digitize a variety of low level sensors with large offsets.

The LTC2400 package is the smallest on the market (SO-8). This tiny chip combined with no external components enables the user to greatly reduce the board area required by existing designs.

Conclusion

The LTC2400 is the first of a family of delta-sigma converters from LTC. It offers a combination of the best characteristics of delta-sigma converters and conventional converters. Its attributes include latency-free operation and high precision INL, DNL and offset. It frees the user from adding external components and is easy to use. The on-chip sinc[4] filter reduces line frequency noise and its harmonics by 120dB, making it ideal for use in noisy environments. With only eight pins, an on-chip oscillator, 24-bit DNL, 4ppm INL and 10ppm TUE, the LTC2400 is the new state of the art in analog-to-digital conversion.

Notes:

1. Candy, J.C and G.C. Temes. "Oversampling Methods for A/D and D/A Conversion," in *Oversampling Delta-Sigma Data Converters.* IEEE Press, 1992.

2. Hauser, Max W. "Principles of Oversampling and A/D Conversion." *Journal of the Audio Engineering Society*, Vol. 39, No. 1/2 (January/February 1991) pp. 3–26.