Hot Swapping the PCI Bus Using the LTC1643

by Robert Reay

Hot Circuit Insertion

When a circuit board is inserted into a live PCI slot, the supply bypass capacitors on the board can draw huge transient currents from the PCI power bus as they charge. The transient currents can cause permanent damage to the connector pins and create glitches on the power bus, causing other boards in the system to reset.

The LTC1643 is designed to turn a board's supply voltages on and off in a controlled manner, allowing the board to be safely inserted into or removed from a live PCI slot without causing glitches on the system power supplies. The chip also protects the PCI supplies from short circuits and monitors the supply voltages.

The LTC1643H is designed for motherboard applications, whereas the LTC1643L is designed for CompactPCI applications where the chip resides on the plug-in board. The part is available in the space saving 16-pin SSOP package.

LTC1643 Features

❏ Allows safe insertion into and removal from either a motherboard (LTC1643H) or CompactPCI board (LTC1643L)
❏ Controls all four PCI supplies: –12V, 12V, 3.3V and 5.0V
❏ Programmable foldback current limit: a programmable analog current limit with a value that depends on the output voltage. If the output is shorted to ground, the current limit drops to keep power dissipation and supply glitches to a minimum.
❏ Programmable circuit breaker: if a supply remains in current limit too long, the circuit breaker will trip, the supplies will be turned off and the FAULT pin will be pulled low.
❏ Current-limit power up: the supplies are allowed to power up in current limit. This allows the chip to power-up boards with widely varying capacitive loads without tripping the circuit breaker. The maximum allowable power-up time is programmable using the TIMER pin.

❏ 12V and –12V power switches on-chip
❏ Power-good output: monitors the voltage status of the four supply voltages.

PCI Power Requirements

All PCI connectors require four power rails: 5V, 3.3V, 12V and –12V. Systems implementing the 3.3V signaling environment are always required to provide all four rails in every system. Systems implementing the 5V signaling environment may either ship the 3.3V supply with the system or provide a means to add it afterward. The tolerance of the supplies as measured at the plug-in card is summarized in Table 1.

Table 1. PCI power supply requirements

Power Rail	Current	Typical Capacitance
5V ±5%	5A	<3000µF
3.3V ±0.3V	7.5A	<3000µF
12V ±5%	500mA	<330µF
–12V ±10%	100mA	<120µF

Power-Up Sequence

The power supplies are controlled by external N-channel pass transistors Q1 and Q2 in the 3.3V and 5.0V power paths and internal pass transistors for the 12V and –12V power paths (see Figure 1).

Resistors R1 and R2 provide current-fault detection and R7 and C1 provide current-control loop compensation. Resistors R5 and R6 prevent high frequency oscillations in Q1 and Q2.

When the ON pin (5) is pulled high, the pass transistors are allowed to turn on and a 20µA current source is connected to the TIMER pin (4) (see Figure 2). The current in each pass transistor increases until it reaches the current limit for each supply.
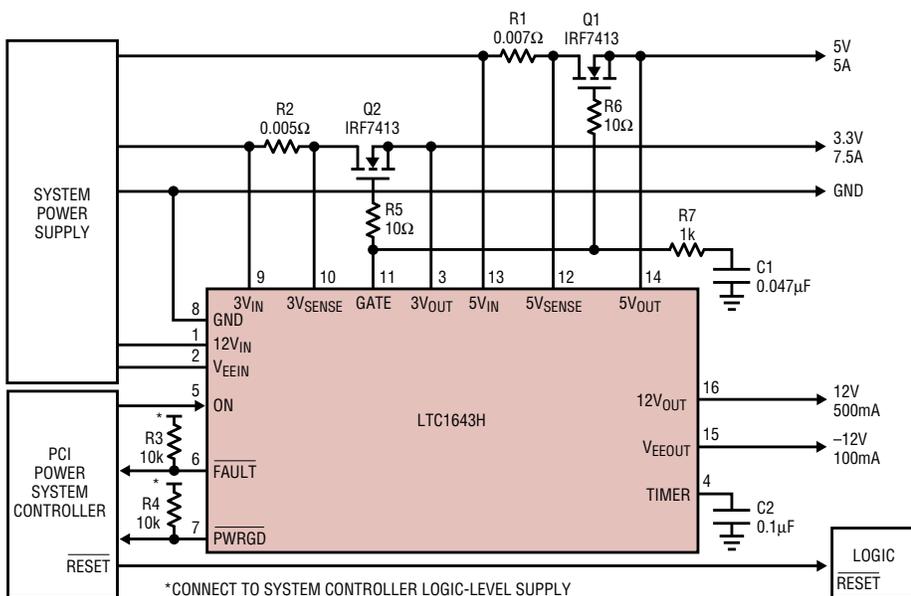

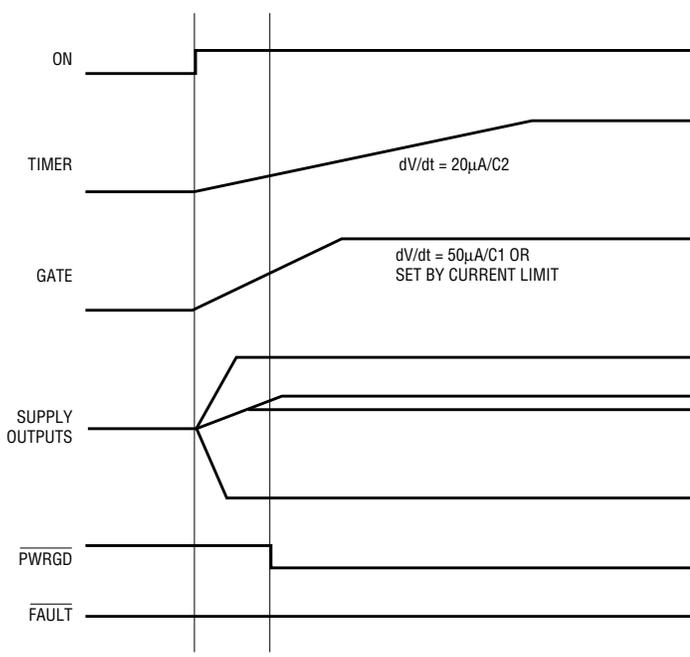
Figure 1. Typical LTC1643H application

Figure 2 (left diagram):

ON

TIMER — dV/dt = 20µA/C2

GATE — dV/dt = 50µA/C1 OR SET BY CURRENT LIMIT

SUPPLY OUTPUTS

PWRGD

FAULT

Figure 2. Normal power-up sequence

Figure 3 (right diagram):

ON

TIMER

GATE — dV/dt = 200µA/C1
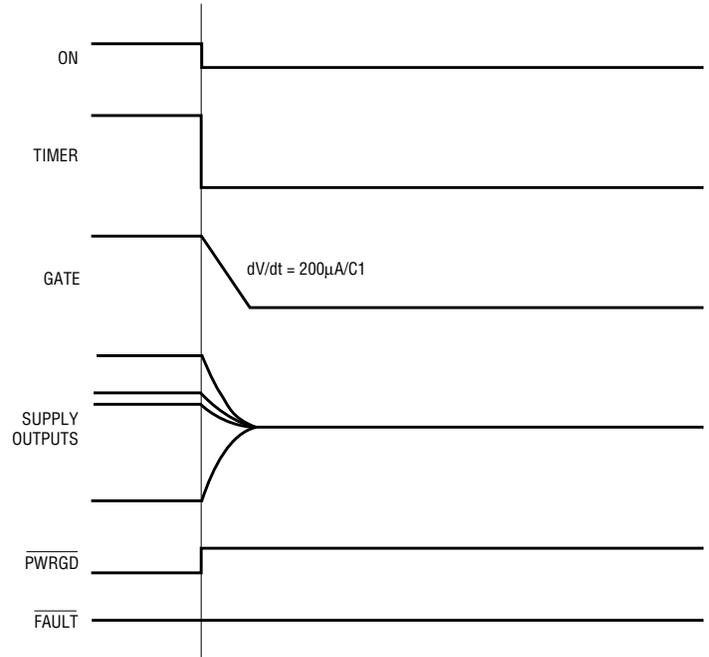
SUPPLY OUTPUTS

PWRGD

FAULT

Figure 3. Normal power-down sequence

Power-Down Sequence

Each supply is then allowed to power up at a rate controlled either by the current limit into the load capacitance or dv/dt = 50µA/C1, whichever is slower. Current limit faults are ignored until the voltage on the TIMER pin (4) reaches 1V below the 12V$_{IN}$ pin (1). Once all four supply voltages are within tolerance, the PWRGD pin (7) will be pulled low.

When the ON pin (5) is pulled low, a power-down sequence begins (see Figure 3). Internal switches are connected to each of the output supply voltage pins to discharge the bypass capacitors to ground. The TIMER pin (4) is immediately pulled low. The voltage on the GATE pin (11) is discharged by a 200µA current source to prevent the load currents on the 3.3V and 5.0V supplies from going to zero instantaneously and causing glitches on the power supplies. When any of the output voltages dips below its threshold, the PWRGD pin (7) is pulled high.

Timer

During a power-up sequence, a 20µA current source is connected to the TIMER pin (4) and current limit faults are ignored until the voltage on this pin increases to within 1V of the 12V$_{IN}$ pin (1). This feature allows the chip to power-up PCI cards with widely varying capacitive loads on the supplies. The power-up time will be:

$$t_{ON} = 2 \times (C_{SUPPLY} \times V_{SUPPLY})/(I_{LIMIT} - I_{LOAD})$$

For C_{SUPPLY} = 2000µF, V_{SUPPLY} = 5V, I_{LIMIT} = 7A, I_{LOAD} = 5A the turn on time will be ~10ms. The timer period should be set longer than the maximum supply turn-on time but short enough to not exceed the maximum safe operating area of the pass transistor during a short circuit. The TIMER period will be:

$$t_{TIMER} = (C_{TIMER} \times 11.1V)/22µA$$

For C_{TIMER} = 0.1µF, the TIMER period will be ~50ms. The TIMER pin

Figure 4 (lower diagram):

ON

TIMER
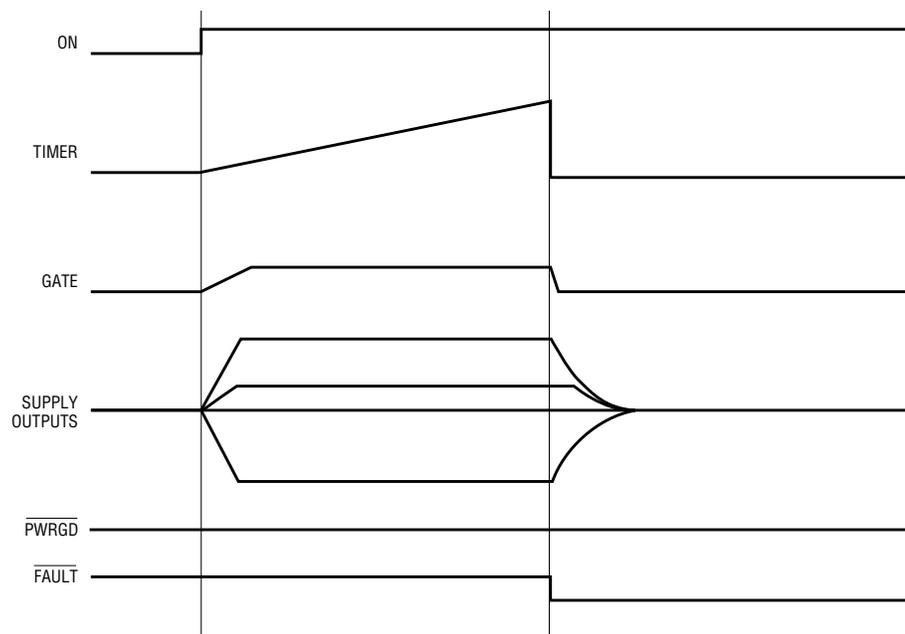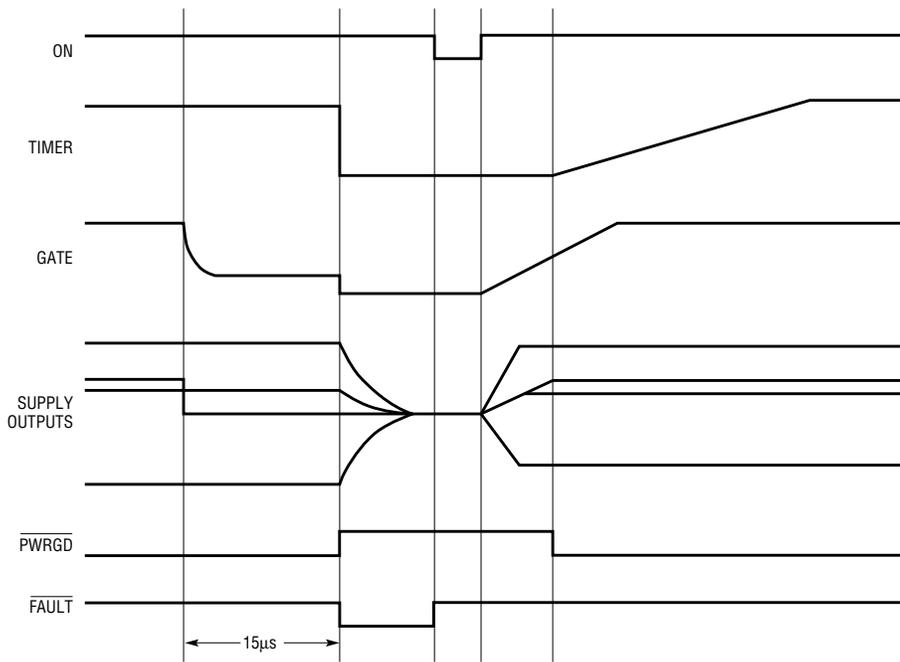
GATE

SUPPLY OUTPUTS

PWRGD

FAULT

Figure 4. Power-up into a short circuit on a 3.3V output

Figure 5. Short circuit on 5V

(4) is immediately pulled low when the ON pin (5) goes low.

Thermal Shutdown

The internal switches for the 12V and –12V supplies are protected by an internal current limit and thermal shutdown circuit. When the temperature of the chip reaches 150°C, all switches will be latched off and the FAULT pin (6) will be pulled low.

Short-Circuit Protection

During a normal power-up sequence, if the voltage on the TIMER pin (4) has reached its maximum and a supply is still in current limit, all of the pass transistors will be immediately turned off and the voltage on the FAULT pin (6) will be a logic low, as shown in Figure 4. If a short circuit occurs after the supplies are powered-up, the shorted supply's current will drop immediately to the limit value (see Figure 5).

If the supply remains in current limit for more than 15µs, all of the supplies will be latched off. The 15µs delay prevents quick current spikes, for example from a fan turning on, from causing false trips of the circuit breaker. The chip will stay in the latched-off state until the ON pin (5)

is cycled low then high or the $12V_{IN}$ power supply is cycled.

To prevent excessive power dissipation in the pass transistors and prevent voltage spikes on the supplies during short-circuit conditions, the current limit on each supply is designed to be a function of the output voltage. As the output voltage drops, the current limit decreases. Unlike a traditional circuit breaker function, where huge currents can flow before the breaker trips, the cur-

rent foldback feature ensures that the supply current will be kept at a safe level and prevent voltage glitches while applying power into a short.

The current limit for the 5.0V and 3.3V supplies is set by placing a sense resistor between $5V_{IN}$ (pin 13) and $5V_{SENSE}$ (pin 12) and between $3V_{IN}$ (pin 9) and $3V_{SENSE}$ (pin 10). The current limit will be set by:

$$I_{LIMIT} = 53mV/R_{SENSE}$$

For a 0.005Ω resistor, the current limit will be set at 10.6A and foldback will be set to 1.5A when the output is shorted. For a 0.007Ω resistor, the current limit will be set at 7.6A and foldback to 1.1A when the output is shorted. The current for the internal 12V switch is set at 1A, folding back to 300mA, and that for the –12V switch is set at 450mA, folding back to 150mA.

A CompactPCI Application

CompactPCI is an open standard for a hot swappable industrial PCI bus supported by the PCI Industrial Manufacturer's Group. The CompactPCI specification calls for the power control to be located on the plug-in board rather than the backplane. The typical application is shown in Figure 6. Because the turn-on signal is active low for CompactPCI, the LTC1643L must be used. **LT**
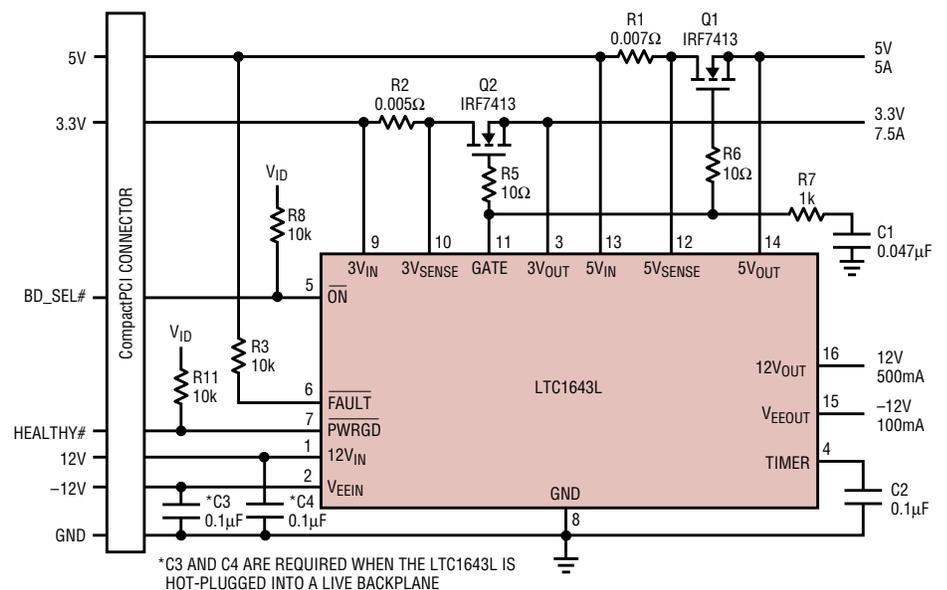
Figure 6. Typical CompactPCI application