Tiny MSOP Dual Switch Driver is SMBus Controlled

by Peter Guan

Introduction
The LTC1623 SMBus™ switch controller offers an inexpensive, space-saving alternative for controlling peripherals in today’s complex portable computer systems. Pin-to-pin connections between the system controller and each peripheral device not only result in complicated wiring, but also limit the number and type of peripheral devices connected to the system controller. Using the SMBus architecture, the LTC1623 eliminates these problems by requiring only two bus wires and allowing easy upgrades and additions of new peripherals.

The SMBus
The SMBus is a low power serial bus developed by Intel and Duracell. Only two bus lines, DATA and CLK, are needed to establish a set of protocols for communication between the bus master and slaves. Using the SEND BYTE protocol of the SMBus to receive and execute commands from the bus master, each LTC1623 controls the operation of two independent external switches. To identify itself on the SMBus, the LTC1623 has two three-state address pins. In other words, up to eight LTC1623s can be programmed to control up to sixteen different switches.

LTC1623 Design Information
A timing diagram of the SEND BYTE protocol is shown in Figure 1. After detecting the Start signal from the bus master (a high-to-low transition on the DATA line while CLK is high), the LTC1623 shifts in the address byte, which consists of seven address bits and one read/write bit. If the address byte matches, the LTC1623 acknowledges the master and then shifts in the command byte whose two LSBs are the controlling signals for the two external switches. Afterwards, the LTC1623 again acknowledges the master so that the master can terminate the transaction by sending a Stop signal (a DATA transition from low to high while CLK is high).

The LTC1623 adheres strictly to the SMBus specification of 0.6V VIL and 1.4V VIH over the entire operating range of 2.7V to 5.5V. The two built-in charge pump triplers with micropower feedback networks guarantee full enhancement of the two external logic-level MOSFET switches without excess gate overdrive. The output gate-drive voltage is regulated to a maximum of 6V above VIN.

Applications
The main application of the LTC1623 is to control two external high-side N-channel switches (Figure 2). As seen in the figure, a 0.1μF capacitor and a 1k resistor are placed on each gate-drive output to respectively slow down the turn-on time of the external switch and to eliminate any oscillations caused by the parasitic capacitance of the external switch and the parasitic inductance of the connecting wires.

SMBus is a trademark of Intel Corp.
Tracking the growing popularity of portable communication systems, the LTC1623 makes a very handy single-slot 3.3V/5V PC Card switch matrix. As shown in Figure 3, this circuit enables a system controller to switch either a 3.3V or a 5V supply to any of its SMBus-addressed peripherals. Besides N-channel switches, the LTC1623 can also be used to control a P-channel switch, as shown in Figure 4. As a result, the load connected to the P-channel switch will be turned on upon power-up of the LTC1623, whereas the other load must wait for a valid address and command to be powered.

**Conclusion**

With a standby current of only 17µA and a tiny 8-lead MSOP (or SO) footprint, the LTC1623 offers a simple and efficient solution for managing system peripherals using the SMBus architecture.

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The mode pins are routed to the connector and are left unconnected (1) or wired to ground (0) in the cable. The internal pull-up current sources ensure a binary 1 when a pin is left unconnected and also ensure that the LTC1543/LTC1544/LTC1344A enter the no-cable mode when the cable is removed. In the no-cable mode, the LTC1543/LTC1544 power supply current drops to less than 200µA and all of the LTC1543/LTC1544 driver outputs will be forced into the high impedance state.

**Adding Optional Test Signal**

In some cases, the optional test signals local loopback (LL), remote loopback (RL) and test mode (TM) are required but there are not enough drivers and receivers available in the LTC1543/LTC1544 to handle these extra signals. The solution is to combine the LTC1544 with the LTC1343. By using the LTC1343 to handle the clock and data signals, the chip set gains one extra single-ended driver/receiver pair. This configuration is shown in Figure 5.

**Compliance Testing**

A European standard EN 45001 test report is available for the LTC1543/LTC1544/LTC1344A chip set. The report provides documentation on the compliance of the chip set to Layer 1 of the NET1 and NET2 standard. A copy of this test report is available from LTC or from Detecon, Inc. at 1175 Old Highway 8, St. Paul, MN 55112.

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**Quadruple 3rd Order 100kHz Butterworth Lowpass Filter**

Another example of the flexibility of the virtual-ground inputs is the ability to add an extra, independent real pole by replacing the input resistor in Figure 2 with an R-C-R "T" network. In Figure 10, a 10k input resistor has been split into two parts and the parallel combination of the two forms a 100kHz real pole with the 680pF external capacitor. Four such 3rd order Butterworth lowpass filters can be built from one LTC1562. The same technique can add additional real poles to other filter configurations as well, for example, augmenting Figure 4’s circuit to obtain a dual 5th order filter from a single LTC1562.

**Conclusion**

The LTC1562 is the first truly compact universal active filter, yet it offers instrumentation-grade performance rivaling much larger discrete-component designs. It serves applications in the 10kHz–150kHz range with an SNR as high as 100dB or more (16+ equivalent bits). The LTC1562 is ideal for modems and other communications systems and for DSP antialiasing or reconstruction filtering.