Versatile Hot Swap Controller with Open Circuit Detect, Foldback Current Limiting and Much More

by Mark Belch

Introduction

When a circuit board is inserted into a live backplane, the input capacitors on the board can draw high inrush currents from the backplane power bus as they charge. The inrush current can permanently damage the connector pins and board components as well as glitch the system supply, causing other boards in the system to reset. The new LT4254 provides a compact and robust solution to eliminate these hot plugging issues.

The LT4254 is designed to turn on a board's supply voltage in a controlled manner, allowing the board to be safely inserted or removed from a live backplane having a supply voltage from 10.8V to 36V. The device features programmable inrush current control, current foldback, programmable 1% tolerance on the undervoltage and overvoltage thresholds, overcurrent protection, and a power good output signal that indicates when the output supply voltage is ready.

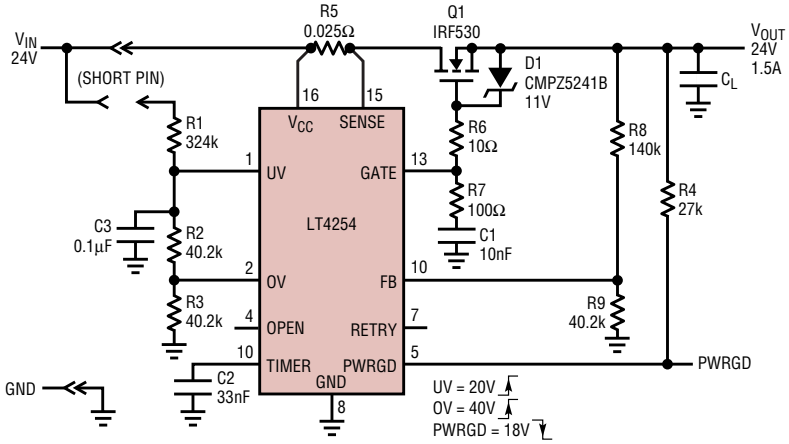

Figure 1. 24V, 1.5A application

Power-Up Sequence

Figure 1 shows a typical LT4254 application. An external N-channel MOSFET pass transistor (Q1) is placed in the power path to control the turn-on/turn-off characteristics of the supply voltage. Capacitor C1 controls the GATE slew rate, R7 provides compensation for the current control loop and R6 prevents high frequency oscillations in Q1.

When the power pins first make contact, transistor Q1 is held off. The V_{IN} and GND connector pins should be longer than the pin that goes to R1 so they connect first and keep the LT4254 off until the board is completely seated in its connector. When the voltage on the V_{CC} pin is between the externally programmed undervoltage and overvoltage thresholds, transistor Q1 is turned on (Figure 2). The voltage at the GATE pin rises with a slope equal to 35µA/C1 and the supply inrush current is $I_{INRUSH} = C_L \bullet 35\mu A/C1$, where C1 is the total load capacitance, provided the part is not in current limit. When the FB pin voltage goes above 4.45V, the PWRGD pin goes high.

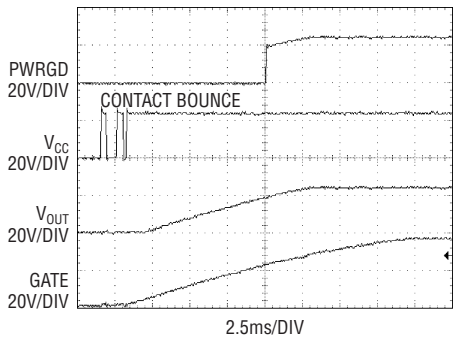

Figure 2. Startup waveforms

Short-Circuit Protection

The LT4254 features a programmable foldback current limit with an electronic circuit breaker that protects against short circuits or excessive load currents. The current limit is set by placing a sense resistor (R5) between V_{CC} and SENSE. To limit excessive power dissipation in the pass transistor and to reduce voltage spikes on the input supply during short-circuit conditions at the output, the current folds back as a function of the output voltage, which is sensed internally on the FB pin. When the voltage at the FB pin is 0V, if the part goes into current limit, the current limit circuitry drives the GATE pin to force a constant 12mV drop across the sense resistor.

Under high current (but not short-circuit) conditions, as the FB voltage increases linearly from 0V to 2V, the voltage across the sense resistor increases linearly from 12mV to 50mV (see Figure 3). With FB above 2V, a

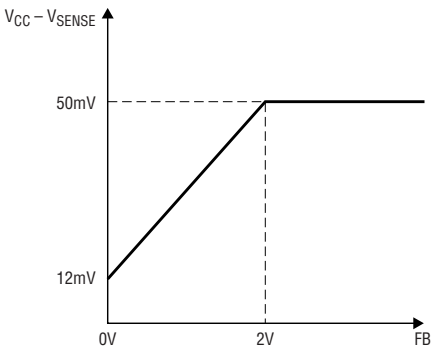

Figure 3. Current limit sense voltage vs FB pin voltage

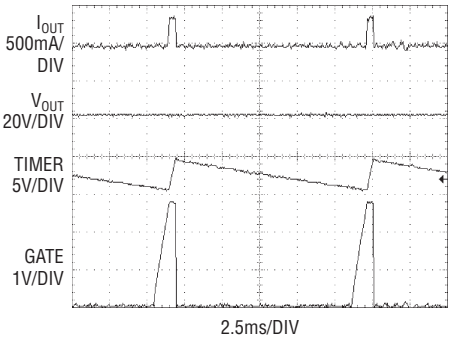

Figure 4. Retry waveforms

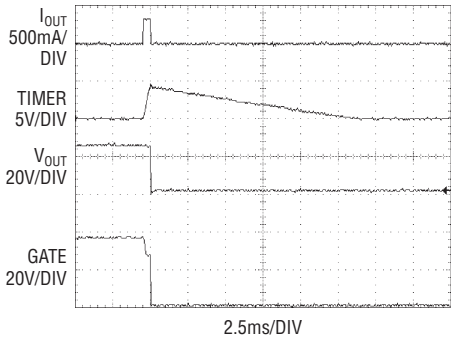

Figure 5. Latch off waveforms

constant 50mV is maintained across the sense resistor.

During startup, a large output capacitance can cause the LT4254 to go into current limit. The current limit level when V_{OUT} is low is only one quarter of the current limit level under normal operation, and it is time limited, so careful attention is needed to insure proper start up. The maximum time the LT4254 is allowed to stay in current limit is defined by the TIMER pin capacitor.

The current limit threshold (during normal operation) is I_{LIMIT} = 50mV/R5, where R5 is the sense resistor. For a 0.025Ω sense resistor, the current limit is set at 2A and folds back to 480mA when the output is shorted to ground. For a 24V application, MOSFET dissipation under short circuit conditions is reduced from 48W to 11.5W.

The LT4254 also features a variable overcurrent response time. The time required for the part to regulate the GATE pin voltage is a function of the voltage across the sense resistor, R5. This helps to eliminate sensitivity to current spikes and transients that might otherwise unnecessarily trigger a current limit response and increase MOSFET dissipation.

Current Limit TIMER

The TIMER pin provides a method for programming the maximum time the part is allowed to operate in current limit. When the current limit circuitry is not active, the TIMER pin is pulled to GND by a 3µA current source. When the current limit circuitry becomes active, a 120µA pull-up current source is connected to the TIMER pin and the voltage rises with a slope equal to 117µA/C_{TIMER}. Once the desired maximum current limit time is chosen, the capacitor value is:

$$C(nF) = 25 \bullet t(ms)$$

If the TIMER pin reaches 4.65V (typ), the internal fault latch is set causing the GATE to be pulled low and the TIMER pin to be discharged to GND by the 3µA current source. The LT4254 does not turn on again until the voltage at the TIMER pin falls below 0.65V (typ).

Undervoltage and Overvoltage Detection

The LT4254 uses the UV (undervoltage) and OV (overvoltage) pins to monitor V_{CC} and allow the user the greatest flexibility for setting the operational thresholds. Figure 1 also shows the UV and OV level programming via a 3-resistor divider (R1, R2, and R3). The UV and OV pins are internally connected to an analog window comparator.

If the UV pin goes below 3.6V or the OV pin rises above 4V, the GATE pin will be immediately pulled low until the UV/OV pin voltages return to the normal operating voltage window (4V and 3.65V on UV and OV, respectively).

Automatic Restart and Latch Off Operation

The RETRY pin can be configured either to latch off the LT4254 or force it into a hiccup mode after an overcurrent fault condition.

If the RETRY pin is floating, when the voltage at the TIMER pin ramps back down to 0.65V (typ), the LT4254 turns Q1 on again. If the short-circuit condition at the output still exists, the cycle will repeat itself indefinitely. The duty cycle under short-circuit conditions is 3%, which limits the power dissipated by Q1, preventing overheating (see Figure 4).

If the RETRY pin is grounded, the LT4254 latches off after a current fault (see Figure 5). After the part latches off, it can be commanded to start back up by cycling the UV pin to ground and then back high. This command can only be accepted after the TIMER pin discharges below the 0.65V typ threshold (to prevent overheating transistor Q1).

Power Good Detection

The LT4254 includes a comparator for monitoring the output voltage. The output voltage is sensed through the FB pin via an external resistor string. If the FB pin goes above 4.45V, the comparator's output releases the PWRGD pin so it can be externally pulled up. The comparator's output (PWRGD pin) is an open collector capable of operating from a pull-up voltage as high as 36V, independent of V_{CC}.

Open MOSFET Detection

The LT4254 can be used to detect the presence of an open MOSFET through the OPEN and PWRGD pins. When the voltage across the sense resistor is less than 3.5mV, the open collector pull-down device is shut off allowing the OPEN pin to be externally pulled high.

An open MOSFET condition is inferred when the OPEN pin is high and the PWRGD pin is low (after the part has completed its start-up cycle). This condition can be falsely signaled during start-up if the load is not activated until after PWRGD goes high; or if the inrush current during start-up is too small, OPEN will not go low until the load is enabled (by the PWRGD signal) as shown in Figure 6. During this time, the OPEN pin is high and the PWRGD pin is low falsely signaling an open MOSFET condition (unless this start-up period is ignored). To avoid this false indication, the OPEN and PWRGD pins should not be polled for a period of time, $T_{STARTUP}$, given by:

$$T_{STARTUP} = (3 \bullet V_{CC} \bullet C1)/35\mu A$$

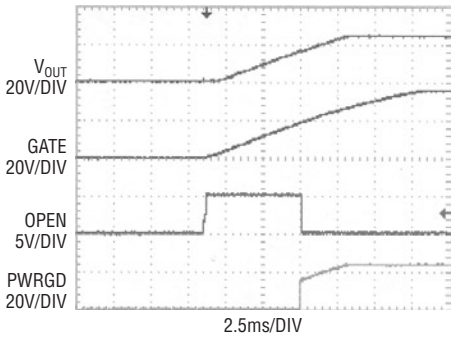

Figure 6. Normal MOSFET start-up waveforms

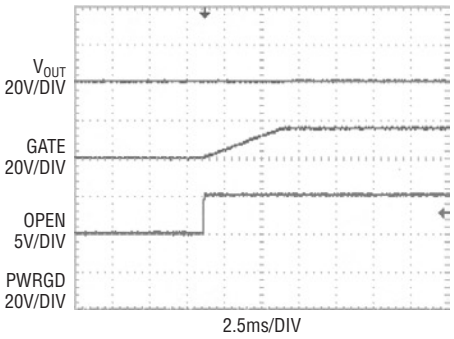

Figure 7. Open MOSFET start-up waveforms.

For example, in Figure 6, $T_{STARTUP}$ is equal to 3 times the typical start-up time, which is 25.5ms (3 × 8.5ms).

This can be accomplished either by using a microcontroller and not polling the logic signals during $T_{STARTUP}$ or by placing an RC filter on the OPEN pin. Once the OPEN voltage exceeds the monitoring logic threshold (signaling an undercurrent condition lasting longer than the start-up period), and PWRGD is low (signaling that the output is not high after the start-up period has finished), an open MOSFET condition is indicated.

Figure 7 shows the typical waveforms for an actual open MOSFET condition. Since the MOSFET is open, V_{OUT} and PWRGD never go high. OPEN goes high as soon as the part is powered up while GATE is clamped to the external Zener voltage above V_{OUT}.

Another condition that can cause a false open MOSFET indication is if the LT4254 goes into current limit during start-up. This causes $T_{STARTUP}$ to be longer than anticipated. Also, if the LT4254 stays in current limit long enough for the TIMER pin to fully charge up to its threshold, the LT4254 will either latch off (RETRY = 0) or go into the current limit hiccup mode (RETRY = floating). In either case, an open MOSFET condition will be falsely signaled. If the LT4254 does go into current limit during start-up, C1 can be increased (to reduce inrush current).

GATE Pin

The GATE pin is clamped to a maximum of 12V above the V_{CC} voltage. This clamp is designed to withstand the internal charge pump current. An external Zener diode must be used if the possibility exists for an instantaneous low resistance short from V_{OUT} to GND. When the input supply voltage is between 12V and 15V, the minimum gate drive voltage is 4.5V, and a logic level MOSFET must be used. When the input supply voltage is higher than 20V, the gate drive voltage is at least 10V, and a standard threshold MOSFET is recommended.

Conclusion

The LT4254's comprehensive set of advanced protection and monitoring features make it applicable in a wide variety of Hot Swap solutions. It can be programmed to control the output voltage slew rate and inrush current. It has programmable undervoltage and overvoltage protection, and monitors the output voltage via the PWRGD pin. The part also indicates if an open MOSFET condition exists. The LT4254 provides a simple and flexible Hot Swap solution with the addition only a few external components.

LT6011, continued from page 12

Differential pair Q1 and Q2, together with load resistors R3 and R4, form a first gain stage. The PNPs Q5 and Q6, and current mirror Q9 and Q10 form the second gain stage. The output stage is designed to be able to both source and sink much larger currents than the stage biasing current. The current-sinking device NPN Q20 is driven directly by Q12, while the current-sourcing PNP Q19 is driven through level-shifting bias network Q13 and Q14.

The level-shifter works as follows: The fixed current flowing into diodes D3–D5 establishes a bias voltage at the base of Q13. As the base of Q14 is driven lower, the V_{BE} of both Q13 and Q14 increases. This increases their current, which flows through Q18/R6 and is mirrored as sourcing current in Q19. Since only collectors are connected to the output, a mere 40mV V_{CE} saturation voltage limits the output swing to either supply rail.

Input devices Q1 and Q2 are super-beta transistors. Their lightly doped base region results in a current gain of more than 1000. In addition, the already low base current is internally compensated by a base current-cancellation circuit. Current mirror Q21 biases Q11 with the exact same current as the input devices. Q17 measures the base current of Q11 and feeds this same current back into the bases of Q1 and Q2. The resulting input bias current is limited only by mismatch and is typically just 20pA.

The input offset voltage of the amplifier is a result of mismatch in Q1/Q2 as well as R3/R4. These internal load resistors are trimmed at the factory to cancel out the total offset voltage to less than 60µV (A-grade). A high degree of balance is maintained through the second stage, which virtually eliminates second-order temperature drift contributions.

Conclusion

Rail-to-rail output swing to supplies as low as 2.7V, power consumption as low as 400µW, and availability in tiny packages make the LT6011 op amp the ideal precision op amp for low voltage, low power, or space constrained applications.