Component and Measurement Advances Ensure 16-Bit DAC Settling Time (Part One)

by Jim Williams

Introduction

Instrumentation, waveform generation, data acquisition, feedback control systems and other application areas are beginning to utilize 16-bit data converters. More specifically, 16-bit digital-to-analog converters (DACs) have seen increasing use. New components (see the sidebar "Components for 16-Bit Digital-to-Analog Conversion" on page 31) have made 16-bit DACs a practical design alternative. These ICs provide 16-bit performance at reasonable cost compared to previous modular and hybrid technologies. The DC and AC specifications of the monolithic DACs approach or equal previous converters at significantly lower cost.

DAC Settling Time

DAC DC specifications are relatively easy to verify. Measurement techniques are well understood, albeit often tedious. AC specifications require more sophisticated approaches to produce reliable information. In particular, the settling time of the DAC and its output amplifier is extraordinarily difficult to determine to 16-bit resolution. DAC settling time is the elapsed time from input code application until the output arrives at and remains within a specified error band around the final value. It is usually specified for a full-scale 10V transition. Figure 1 shows that DAC settling time has three distinct components. The *delay time* is very small and is almost entirely due to propagation delay through the DAC and output amplifier. During this interval there is no output movement. During *slew time* the output amplifier moves at its highest possible speed towards the final value. *Ring time* defines the region where the amplifier recovers from slewing and ceases movement within some defined error band. There is normally a trade-off between slew and ring time. Fast-slewing amplifiers generally have extended ring times, complicating amplifier choice and frequency compensation. Additionally, the architecture of very fast amplifiers usually dictates trade-offs that degrade DC error terms.

Measuring anything at any speed to 16 bits (≈0.0015%) is hard. Dynamic measurement to 16-bit resolution is particularly challenging. Reliable 16-bit settling-time measurement constitutes a high order difficulty problem requiring exceptional care in approach and experimental technique.

Considerations for Measuring DAC Settling Time

Historically, DAC settling time has been measured with circuits similar to that in Figure 2. The circuit uses the "false sum node" technique. The resistors and DAC-amplifier form a bridge-type network. Assuming ideal resistors, the amplifier output will step to V_{IN} when the DAC inputs move to all ones. During slew, the settle node is bounded by the diodes, limiting voltage excursion. When settling occurs, the oscilloscope probe voltage should be zero. Note that the resistor divider's attenuation means the probe's output will be one-half of the actual settled voltage.

In theory, this circuit allows settling to be observed to small amplitudes. In practice, it cannot be relied upon to produce useful measurements. The oscilloscope connection presents problems. As probe capacitance rises, AC loading of the resistor junction influences observed settling waveforms. A 10pF probe alleviates this problem but its 10× attenuation sacrifices oscilloscope gain. 1× probes are not suitable because of their excessive input capacitance. An active

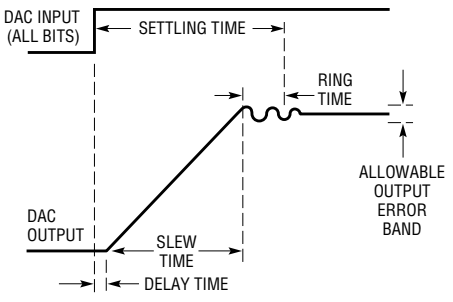

Figure 1. DAC-settling-time components include delay, slew and ring times. Fast amplifiers reduce slew time, although longer ring time usually results. Delay time is normally a small term.

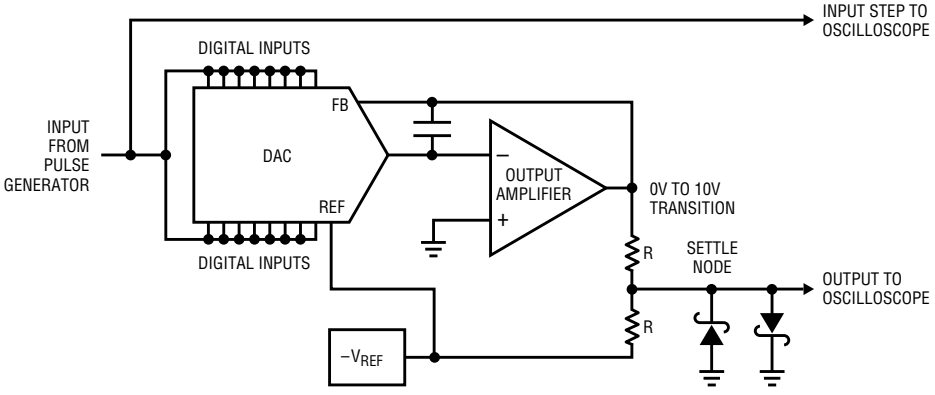

Figure 2. Popular summing scheme for DAC-settling-time measurement provides misleading results. 16-bit measurement causes >200× oscilloscope overdrive. Displayed information is meaningless.

Components for 16-Bit D/A Conversion

Components suitable for 16-bit D/A conversion are members of an elite class. 16 binary bits is one part in 65,536—just 0.0015% or 15 parts-per-million. This mandates a vanishingly small error budget and the demands on components are high. The digital-to-analog converters listed in Table A all use Si-Chrome thin-film resistors for high stability and linearity over temperature. Gain drift is typically 1ppm/°C or about 2LSBs over 0°C to 70°C. The amplifiers shown contribute less than 1LSB error over 0°C to 70°C with 16-bit DAC driven settling times of 1.7µs available. The references offer drifts as low as 1LSB over 0°C to 70°C with initial trimmed accuracy to 0.05%

Table A. Short-form descriptions of components suitable for 16-bit digital-to-analog conversion

Component Type	Error Contribution Over 0°C to 70°C	Comments
LTC1597 DAC	≈2LSB Gain Drift 1LSB Linearity	Full Parallel Inputs Current Outputs
LTC1595 DAC	≈2LSB Gain Drift 1LSB Linearity	Serial Input 8-Pin Package Current Output
LTC1650 DAC	≈3.5LSB Gain Drift 6LSB Offset 4LSB Linearity	Complete Voltage Output DAC
LT1001 Amplifier	<1LSB	Good Low Speed Choice 10mA Output Capability
LT1012 Amplifier	<1LSB	Good Low Speed Choice Low Power Consumption
LT1468 Amplifier	<2LSB	1.7µs Settling to 16 Bits Fastest Available
LM199A Reference: 6.95V	≈1LSB	Lowest Drift Reference in this Group
LT1021 Reference: 10V	≈4LSB	Good General Purpose Choice
LT1027 Reference: 5V	≈4LSB	Good General Purpose Choice
LT1236 Reference: 10V	≈10LSB	Trimmed to 0.05% Absolute Accuracy
LT1461 Reference: 4.096V	≈10LSB	Recommended for LTC1650 DACs (see Above)

1× FET probe will work, but another issue remains.

The clamp diodes at the settle node are intended to reduce swing during amplifier slewing, preventing excessive oscilloscope overdrive. Unfortunately, oscilloscope overdrive recovery characteristics vary widely among different types and are not usually specified. The Schottky diodes' 400mV drop means the oscilloscope may see an unacceptable overload, bringing displayed results into question.

At 10-bit resolution (10mV at the DAC output—5mV at the oscilloscope), the oscilloscope typically undergoes a 2× overdrive at 50mV/DIV and the desired 5mV baseline is just discernible. At 12-bit or higher resolution, the measurement becomes hopeless with this arrangement. Increasing oscilloscope gain brings commensurate increased vulnerability to overdrive induced errors. At 16 bits, there is clearly no chance of measurement integrity.

The preceding discussion indicates that measuring 16-bit settling time requires a high gain oscilloscope that is somehow immune to overdrive. The gain issue is addressable with an external wideband preamplifier that accurately amplifies the diode-clamped settle node. Getting around the overdrive problem is more difficult.

The only oscilloscope technology that offers inherent overdrive immunity is the classical sampling 'scope.

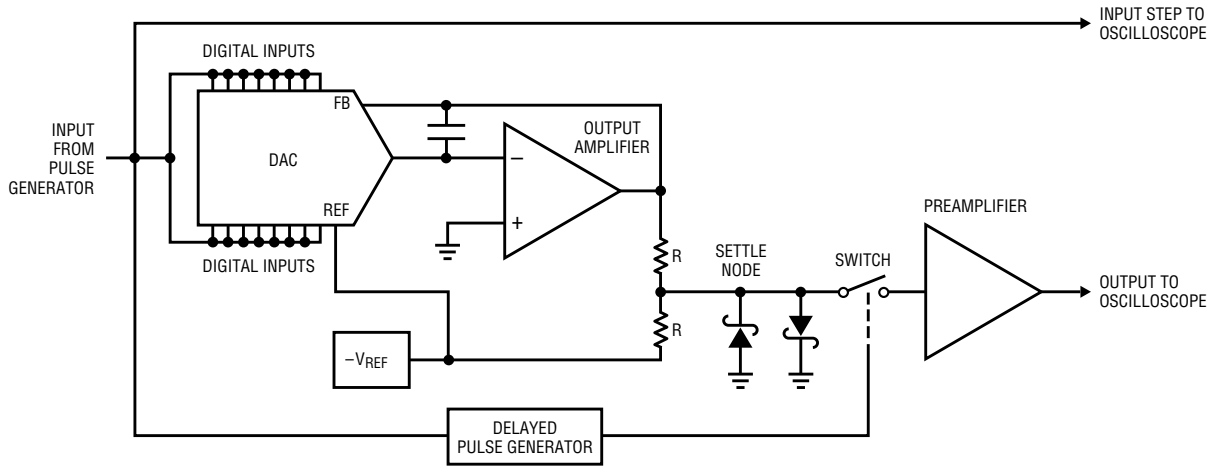

Figure 3. Conceptual arrangement eliminates oscilloscope overdrive. A delayed pulse generator controls the switch, preventing the oscilloscope from monitoring settle node until settling is nearly complete.

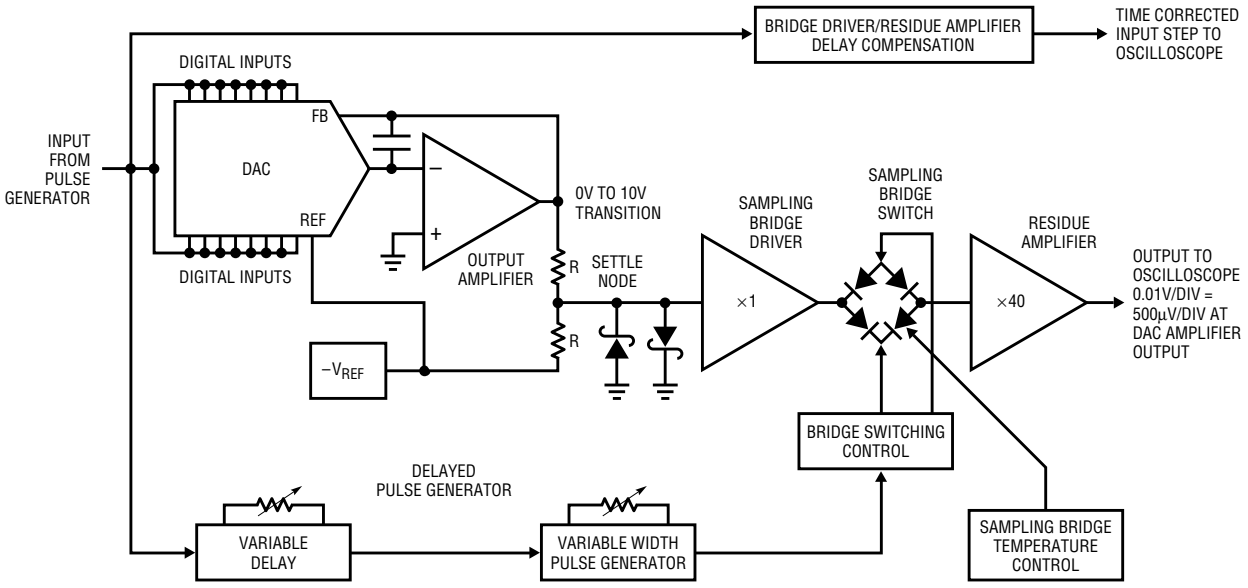

Figure 4. Block diagram of DAC-settling-time measurement scheme: diode bridge switch minimizes switching feedthrough, preventing residue-amplifier oscilloscope overdrive. Temperature control maintains 10µV switch offset baseline. Input step-time reference is compensated for ×1 and ×40 amplifier delays.

Unfortunately, these instruments are no longer manufactured (although still available on the secondary market). It is possible, however, to construct a circuit that borrows the overload advantages of classical sampling 'scope technology. Additionally, the circuit can be endowed with features particularly suited for measuring 16-bit DAC settling time.

Practical DAC-Settling-Time Measurement

Figure 3 is a conceptual diagram of a 16-bit DAC-settling-time measurement circuit. This figure shares attributes with Figure 2, although some new features appear. In this case, the preamplified oscilloscope is connected to the settle point by a switch. The switch state is determined by a delayed pulse generator, which is triggered from the same pulse that controls the DAC. The delayed pulse generator's timing is arranged so that the switch does not close until settling is very nearly complete. In this way the incoming waveform is sampled in time, as well as amplitude. The oscilloscope is never subjected to overdrive—no off-screen activity ever occurs.

Figure 4 is a more complete representation of the DAC settling time scheme. Figure 3's blocks appear in greater detail and some new refinements show up. The DAC-amplifier summing area is unchanged. Figure 3's delayed pulse generator has been split into two blocks; a delay and a pulse generator, both independently variable. The input step to the oscilloscope runs through a section that compensates for the propagation delay of the settling-time-measurement path. The most striking new aspect of the diagram is the diode bridge switch. Borrowed from classical sampling oscilloscope circuitry, it is the key to the measurement. The diode bridge's inherent balance eliminates charge-injection-based errors in the output. It is far superior to other electronic switches in this characteristic. Any other high speed switch technology contributes excessive output spikes due to charge-based feedthrough. FET switches are not suitable because their gate-channel capacitance permits such feedthrough. This capacitance allows gate-drive artifacts to corrupt the oscilloscope display, inducing overload and defeating the switch's purpose.

The diode bridge's balance, combined with matched, low capacitance, monolithic diodes and complementary high speed switching, yields a cleanly

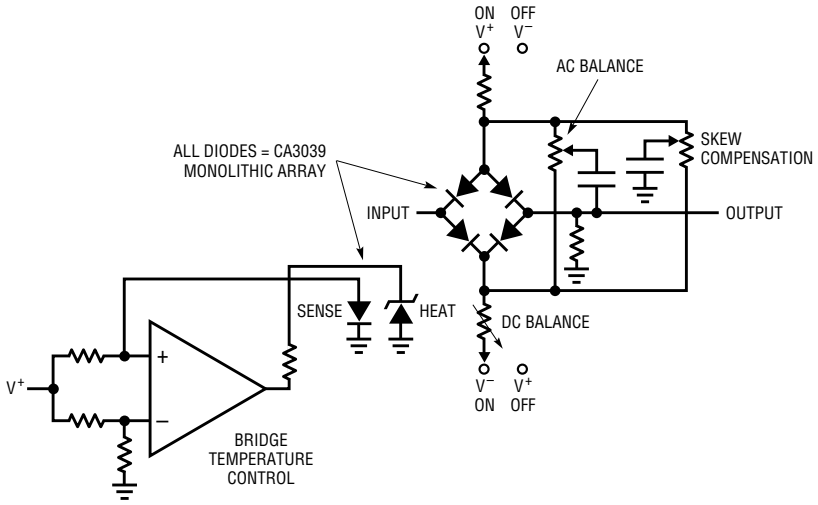

Figure 5. Diode bridge switch trims include AC and DC balance and switch drive timing skew. Remaining diodes in monolithic array are used for temperature control.

switched output. The monolithic diode bridge is also temperature controlled, providing a bridge offset error below 10µV, stabilizing the measurement baseline. The temperature control is implemented using uncommitted diodes in the monolithic array as heater and sensor.

Figure 5 details considerations for the diode bridge switch. The bridge diodes tend to cancel each other's temperature coefficient—unstabilized bridge drift is about 100µV/°C and the temperature control reduces residual drift to a few microvolts/°C.

Bridge temperature control is achieved by using one diode as a sensor. Another diode, running in reverse breakdown ($V_Z \approx 7V$), serves as the heater. The control amplifier, comparing the sensor diode to a voltage at its negative terminal, drives the heater diode to temperature stabilize the array.

DC balance is achieved by trimming the bridge on-current for zero input–output offset voltage. Two AC trims are required. The "AC balance" corrects for diode and layout capacitive imbalances and the "skew compensation" corrects for any timing asymmetry in the nominally complementary bridge drive. These AC trims compensate small dynamic imbalances that could result in parasitic bridge outputs.

Conclusion

This concludes part one of this article. Part two, which will appear in the November issue of *Linear Technology* magazine, details the settling time circuitry and presents results. Both parts represent a distillation of a full-length LTC application note, *AN74, Component and Measurement Advances Ensure 16-Bit DAC Settling Time.*