AD4116
Frequently Asked Questions (FAQs)

Q1. What is the difference of AD4116 to AD4111/AD4112/AD4114/AD4115?

AD4116 is the only is the only member of the family with a 10 MΩ input impedance and with additional low input voltage specifically design to have better performance at lower input ranges useful for current measurements which allowed extra rooms for any errors introduced by external sense resistor. Key differences are summarized in Table 1 below.

Q2. On the AD4116 can I detect if the input signals are floating due to faulty wiring?

AD4116 do not have a built-in open wire detection feature, this can be implemented by a pull up resistor, biased to for example 15V and an external input buffer between the pull up and ADC inputs. When the input is disconnected, the input voltage will be pulled out and recognized as overrange in the ADC data. Note that VIN=+15V won't cause the ADC Data result to saturate at full-scale, so any detection of 'overrange' must be done by user software. Please take note also that a +15V can only be assumed to be due to the pull-up if VIN (−) is always 0V. With a differential input, another resistor from VIN (−) to -15V might be needed, in case both wires break.

If customer is looking for a built-in open wire detect the AD4111 provides a unique solution for open wire detection on the voltage inputs from a single 5V/3.3V supply. Open wire detection is calculated by comparing the difference between the two channel conversions to a certain threshold. Details can be found on page 27 in the Open Wire Detection section of the AD4111 datasheet.

Q3. What is the recommended anti-aliasing filter required for the AD4116 Voltage Inputs?

For the AD4116 the recommend anti-aliasing is 4.7nF/180Ω as this combination will give you the optimum performance and were used in the EMC evaluation.

Q4. Why are the Analog input buffers required for voltage measurements AD4116?

The Analog input buffers should be enabled for voltage Analog inputs as these provide a low source impedance to the sampling ADC. If these buffers were disabled, then a large resistance would exist. This combined with any parasitic capacitance from the resistive front end driving the ADC input will result in a very large gain error.

Table 1. AD411x Summary

Specification/ Product	Voltage Measurement Channel	Current Measurement Channel	Speed (SPS)	VIN Max Ratings	AVDD Supply	Open wire Detection
AD4111	4 Differential/ 8 Single Ended	4 Single Ended 0 to 20mA	31,250	±50V	3V to 5.5V	YES
AD4112	4 Differential/ 8 Single Ended	4 Single Ended 0 to 20mA	31,250	±50V	3V to 5.5V	N/A
AD4114	8 Differential/ 16 Single Ended	N/A	31,250	±65V	3V to 5.5V	N/A
AD4115	8 Differential/ 16 Single Ended	N/A	125,00	±65V	4.5V to 5.5V	N/A
AD4116	6 Differential/ 11 Single Ended Low-level Inputs: 2 Differential/ 4 Single Ended	N/A	62,500	±65V	4.5V to 5.5V	N/A

Q5. What's the equivalent input impedance for a pair of voltage input pins of AD4116?

Figure 1 below is the detailed figure of the voltage input stage. The ideal input impedance is 11MΩ, therefore the differential impedance is 22MΩ. The actual value may vary from part to part.

Q6. What's the maximum VIN input voltage range allowed for AD4116?

The A4116 can operate with the ±10V differential input voltage range is functional up to a differential input signal of ±VREF× 10. However, AD4116 only operates with AVDD range from 4.5V to 5.5V, thus the absolute input pin voltage range is up to ±20V.

Q7. On the AD4116 what's the equivalent TUE (total uncompensated error) spec across different input voltage ranges for example ±10V, ±5V, ±2.5V or 0-10V, 0-5V, 0-2.5V?

The AD4116 is specified for a TUE spec at ±10V full scale range. When input span is reduced the error will change as TUE is specified as a percentage of Full-scale range (%FSR).

To calculate the equivalent TUE spec for smaller ranges, we would take the assumption that gain-error and offset error both account for 50% of the total TUE. Please take note that this method provides only an estimated value, the actual performance could be better or worse as we only guaranteed the TUE spec at ±10V input range.

We can start by working through the errors in mV or V initially and then translating to a final TUE Specification

If we take an input span of ±10V and take the TUE from the datasheet specification for ±10V input at 25°C,192.5 µs settling.

For **AD4116**, TUE specs at 25°C,192.5 µs settling is specified as 0.1%. Thus,

Offset error = 0.05% of 20V span =>10mV

Full-Scale error at +10V (after correcting for offset error) = 0.05% of 20V span =>10mV

TUE = (10mV+10mV)/20 *100 = 0.1%

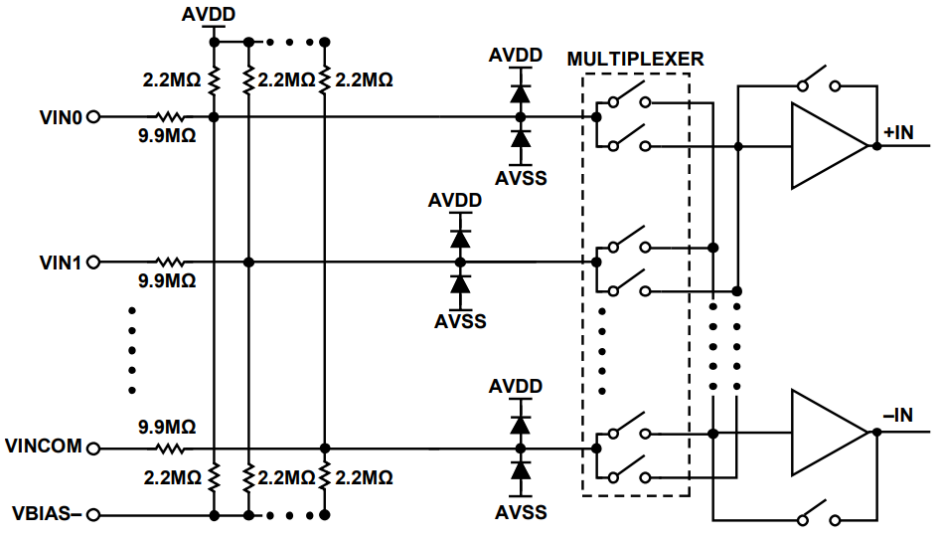

Figure 1 Simplified Voltage input circuit of AD4116

Table 2 shows the TUE estimation at 25°C across different ranges. The same approach can be applied when calculating TUE across different temperature.

Table 2. AD4116 TUE estimation at 25°C

Input span	AD4116
±5V	Offset error = 10mV; Full-Scale error = 10mV*(5V/10V) = 5mV; TUE = (10mV + 5mV)/10 *100 = 0.155%
±2.5V	Offset error = 10mV; Full-Scale error = 10mV*(2.5V/10V) = 2.5mV; TUE = (10mV + 2.5mV)/5*100 = 0.25%
0 – 10 V	Offset error = 10mV; Full-Scale error = 10mV*(10V/10V) = 10mV; TUE = (10mV + 10mV)/10 *100 = 0.2%
0 – 5 V	Offset error = 10mV; Full-Scale error = 10mV*(5V/10V) = 5mV; TUE = (10mV + 5mV)/5*100 = 0.3%
0 – 2.5 V	Offset error = 10mV; Full-Scale error = 10mV*(2.5V/10V) = 2.5mV; TUE = (10mV + 2.5mV)/2.5*100 = 0.5%

Q8. What is the difference in output data rate between multiple channel configuration and single channel configurations for AD4116?

The AD4116 can run at faster output data rates when converting on a single channel. When multiple channels are enabled the digital filter must settle fully for each channel and therefore the result is a slower output data rate.

For AD4116: When the filter is configured to Sinc5+Sinc1 and the fastest output data rate of 62500 SPS is selected.

For a single channel the effective output data rate is 62500 SPS, the time between conversions is 1/ODR = 16us. If "SING_CYC" bit is set or if more than one channel is enabled for the same filter configuration i.e. 62500 SPS then the time between conversions is 80.5us, the delay required is due to the filter settling time.

Q9. What is the SPI mode of operation of the AD4116, what polarity do I need to consider?

The interface operates in SPI Mode 3 (CPOL=1, CPHA=1) wherein SCLK idles high, the falling edge of SCLK is the drive edge, and the rising edge of SCLK is the sample edge. Data is clocked out on the falling/drive edge and data is clocked in on the rising/sample edge.

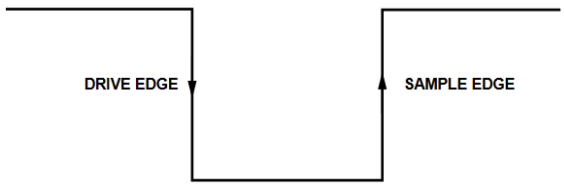

Figure 2 SPI Mode 3

Q10. Where can I find a full and workable sample codes for AD4116 for a ST processor?

We have firmware example code with SDP-K1 EVAL board available on the link below.

ad717x_ad411x_mbed_example

The firmware provides a basic user-interface for interacting with the evaluation-board as it waits for user input over serial interface (UART). All the main functionality of the AD411x is provided in the application-code in abstracted form and the user is

free to customize the software to suit their own needs for working with the AD411x.

Q11. What is the recommended initialization and register configuration sequence for AD4116?

On power-up, it is advisable to perform a reset by writing 64 consecutive ones to the part.

This will reset the serial interface, and it will also reset the on-chip registers to their default conditions. The device does have a power-on reset function. However, any glitches during power-up can cause corruption of the registers, therefore a reset in the initialization routine is advisable.

After the reset, the device can be configured for the application. Please refer to AD4116 Datasheet Register map section.

The recommended flow is as follows:

1. Write to Channel Configuration (Select input and setup for each ADC channel, enable open wire detection in GPIO configuration)
2. Write to Setup Configuration (Select Filter order, Output data rate, etc.)
3. Write to ADC Mode and Interface Mode Configuration (Select ADC operating mode, Clock source, enable CRC, Data+Status, etc.)

Q12. How many data registers does the AD4116 have to store conversion results for each channel?

The AD411x devices have one data register, therefore only one conversion result is stored at any given time. When several channels are enabled, the ADC will automatically sequence through the enabled channels, performing one conversion on each channel before moving to the next. Therefore, it is important to ensure the current conversion result is read before the next conversion is complete. The data register is updated as soon as each conversion is available. The DRDY/RDY output pulses low each time a conversion is available. The user can then read the conversion while the ADC converts the next enabled channel. Figure 3 shows an example of timing diagram when ADC is in continuous conversion mode.

For more details please reference the product page AD4116, Engineer Zone, or AD411x: FAQ

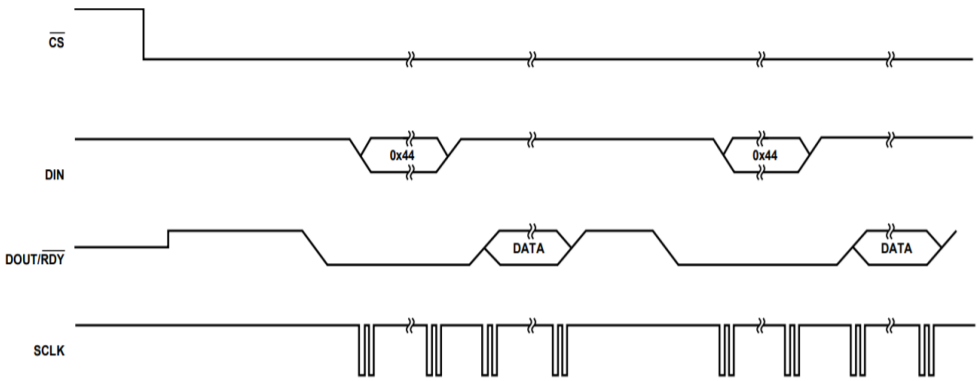

Figure 3 Continuous conversion mode