

	8	7	6	5	4	3	2	1																																																														
D	THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG DEVICES.					JUMPER TABLE <table border="1"><tr><td>JP#</td><td>ON</td><td>OFF</td></tr><tr><td>1</td><td></td><td></td></tr><tr><td>2</td><td></td><td></td></tr><tr><td>3</td><td></td><td></td></tr><tr><td>4</td><td></td><td></td></tr><tr><td>5</td><td></td><td></td></tr></table> * SEE ASSEMBLY INSTRUCTIONS	JP#	ON	OFF	1			2			3			4			5						REVISIONS <table border="1"><tr><td>REV</td><td>DESCRIPTION</td><td>DATE</td><td>APPROVED</td></tr><tr><td></td><td></td><td></td><td></td></tr></table>		REV	DESCRIPTION	DATE	APPROVED																																					
JP#	ON	OFF																																																																				
1																																																																						
2																																																																						
3																																																																						
4																																																																						
5																																																																						
REV	DESCRIPTION	DATE	APPROVED																																																																			
C	RELAY CONTROL CHART <table border="1"><tr><td>CONTROL</td><td>CODE</td><td>DEVICE</td><td>FUNCTION</td><td>CONNECTOR</td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr></table>					CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR																																																												
CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR																																																																		
B																																																																						
A	<table border="1"><tr><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr><tr><td>P.O SPEC.</td><td>BK/BD SPEC.</td><td>SOCKET OEM</td><td>OEM PART#</td><td>HANDLER</td></tr></table>																																								P.O SPEC.	BK/BD SPEC.	SOCKET OEM	OEM PART#	HANDLER	<table border="1"><tr><td>TEMPLATE ENGINEER - HARDWARE SERVICES - HARDWARE SYSTEMS - TEST ENGINEER - COMPONENT ENGINEER - TEST PROCESS - HARDWARE RELEASE -</td><td>DATE</td><td colspan="2">SCHEMATIC</td></tr><tr><td>DESIGNER M. JONES / C. FRICK CHECKER -</td><td></td><td colspan="2">QUAD MXFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9986<DRAWING_TITLE1><DRAWING_TITLE2><DRAWING_TITLE3><DRAWING_TITLE4><DRAWING_TITLE5></td></tr><tr><td colspan="2">PTD ENGINEER</td><td colspan="2">MASTER PROJECT TEMPLATE <DRAWING_TITLE6> UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES</td></tr><tr><td colspan="2">TOLERANCES DECIMALS X.XX +/-0.010 Fractions +1/32 Angles +/-2 SIZE D SCALE 1:1 CODE ID NO. - SHEET 1 OF 79</td></tr></table>					TEMPLATE ENGINEER - HARDWARE SERVICES - HARDWARE SYSTEMS - TEST ENGINEER - COMPONENT ENGINEER - TEST PROCESS - HARDWARE RELEASE -	DATE	SCHEMATIC		DESIGNER M. JONES / C. FRICK CHECKER -		QUAD MXFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9986<DRAWING_TITLE1><DRAWING_TITLE2><DRAWING_TITLE3><DRAWING_TITLE4><DRAWING_TITLE5>		PTD ENGINEER		MASTER PROJECT TEMPLATE <DRAWING_TITLE6> UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		TOLERANCES DECIMALS X.XX +/-0.010 Fractions +1/32 Angles +/-2 SIZE D SCALE 1:1 CODE ID NO. - SHEET 1 OF 79							
P.O SPEC.	BK/BD SPEC.	SOCKET OEM	OEM PART#	HANDLER																																																																		
TEMPLATE ENGINEER - HARDWARE SERVICES - HARDWARE SYSTEMS - TEST ENGINEER - COMPONENT ENGINEER - TEST PROCESS - HARDWARE RELEASE -	DATE	SCHEMATIC																																																																				
DESIGNER M. JONES / C. FRICK CHECKER -		QUAD MXFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9986<DRAWING_TITLE1><DRAWING_TITLE2><DRAWING_TITLE3><DRAWING_TITLE4><DRAWING_TITLE5>																																																																				
PTD ENGINEER		MASTER PROJECT TEMPLATE <DRAWING_TITLE6> UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES																																																																				
TOLERANCES DECIMALS X.XX +/-0.010 Fractions +1/32 Angles +/-2 SIZE D SCALE 1:1 CODE ID NO. - SHEET 1 OF 79																																																																						
	8	7	6	5	4	3	2	1																																																														

QUAD MXFE PHASED-ARRAY PLATFORM

ANALOG DEVICES

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
1	142-0701-201 J41		

SCHEMATIC

QUAD MXFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9986

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
M. JONES / C. FRICK

DRAWING NO.
02-057438

REV
A

SHEET 2 OF 79

SIZE D SCALE 1:1

THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN ANY MANNER, WITHOUT THE WRITTEN PERMISSION OF ANALOG DEVICES INC. THE EQUIPMENT DESIGN HEREON MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG DEVICES INC.

Pin 1: J37 1

Pin 2: 3287-6101

Pin 3: GND

3278-6101

0

AMP_5V_1	AMP_5V_1
AMP_5V_2	AMP_5V_2
AMP_5V_3	AMP_5V_3
AMP_5V_4	AMP_5V_4
MXFE0_DIG_1V	MXFE0_DIG_1V
MXFE0_ANA_1V	MXFE0_ANA_1V
MXFE0_MIX_1V	MXFE0_MIX_1V
MXFE1_DIG_1V	MXFE1_DIG_1V
MXFE1_ANA_1V	MXFE1_ANA_1V
MXFE1_MIX_1V	MXFE1_MIX_1V
MXFE2_DIG_1V	MXFE2_DIG_1V

Timing diagram showing three signals: PLL_V5_1, PLL_V5_2, and PLL_V5_3. The signals are square waves with a period of 2 units and a duty cycle of 50%. The time axis is labeled with 0, 1, and 2.

Signal	Value
PLL_V5_1	1
PLL_V5_2	1
PLL_V5_3	1



SCHEMATIC

OFFICE OF THE SECRETARY OF DEFENSE
 OFFICE OF THE SECRETARY OF DEFENSE GROUP

DRAWING NO.
02-057438

REV
A

SCALE
1:1

SHEET **2** OF **79**

 ANALOG DEVICES	SCHEMATIC				
	QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9986				
THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN CONNECTION WITH ANY OTHER PROJECT OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT DESIGN HEREON MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG DEVICES.	DESIGN VIEW <u><DESIGN_VIEW></u>	DRAWING NO. 02-057438	REV A		
	PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 2	OF 79

MXFE INPUT / OUTPUT

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ADC_P<3..0> SPI_SDIO

ADC_N<3..0>

SERDIN_P<3..0>

SERDIN_N<3..0>

SYNCIN_P

SYNCIN_N

RXEN<1..0>

TXEN<1..0>

SYSREF_P

SYSREF_N

RESETB

CLKIN_P

CLKIN_N

SPI_CS

SPI_SCLK

GPIO<10..0>

DAC_P<3..0>

DAC_N<3..0>

SERDOUT_P<3..0>

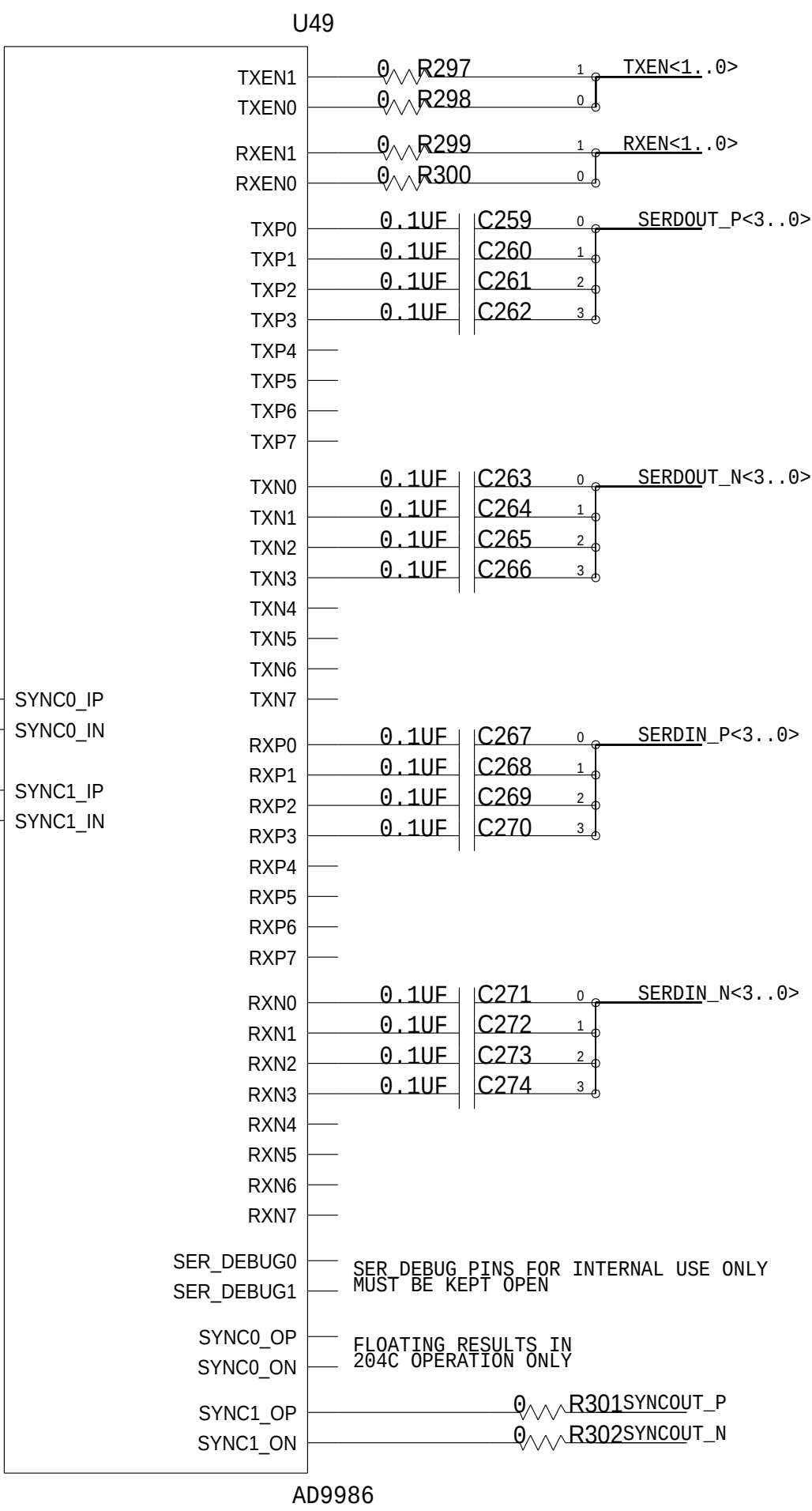
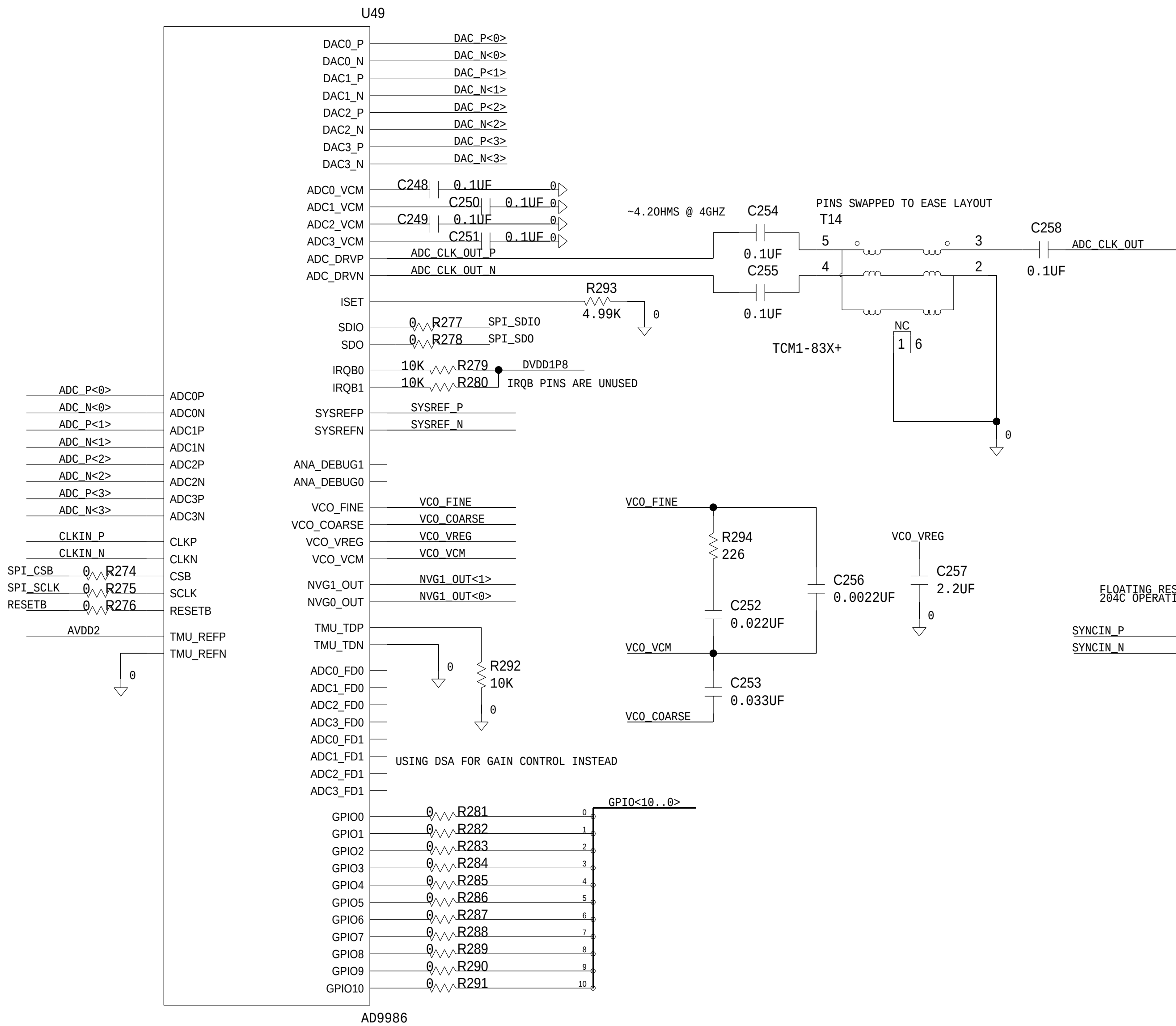
SERDOUT_N<3..0>

SYNCOUT_P

SYNCOUT_N

SPI_SD0

ADC_CLK_OUT

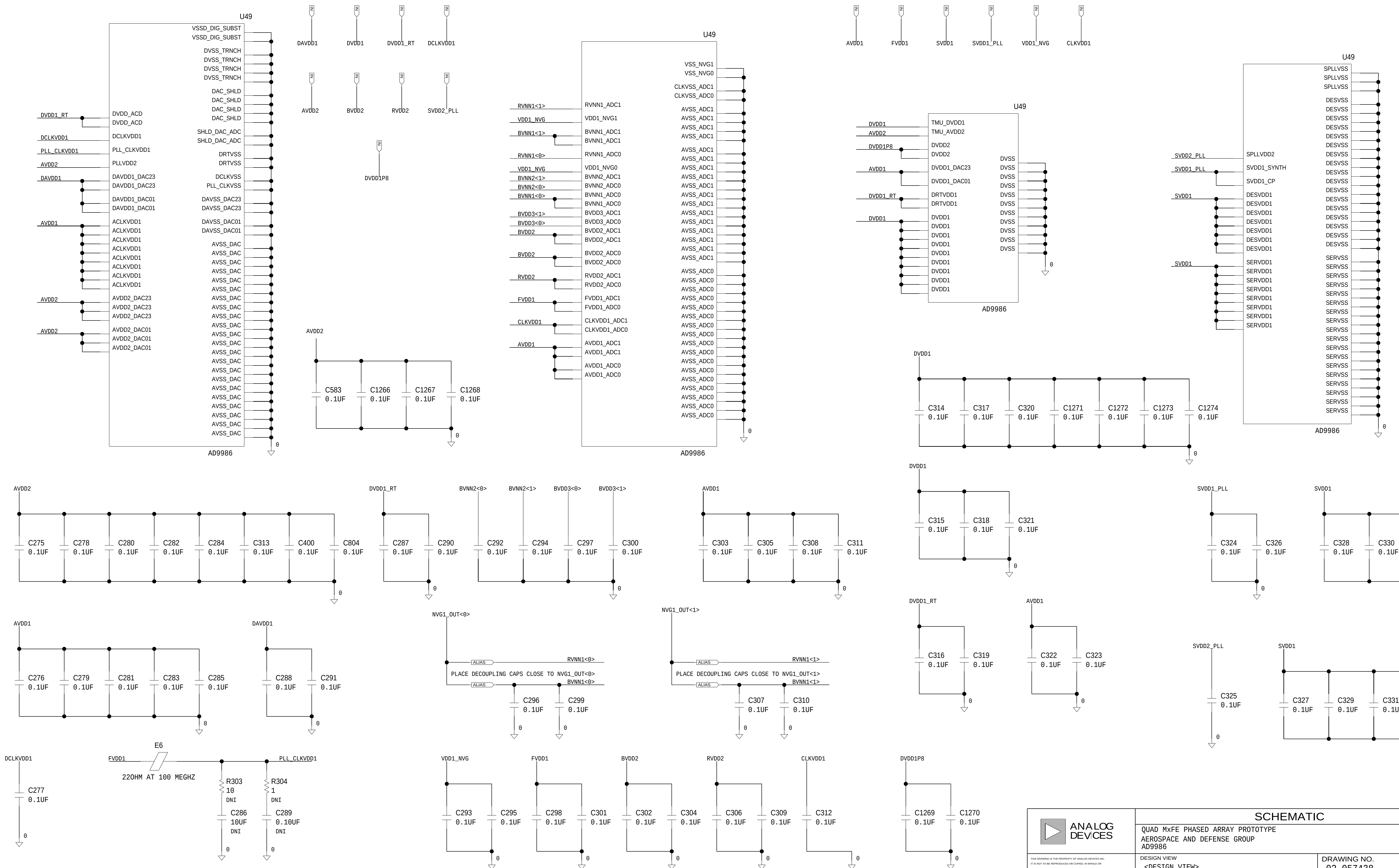


THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC.
IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR
IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS,
OR FOR ANY OTHER PURPOSES DETRIMENTAL TO THE INTERESTS
OF ANALOG DEVICES.
THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS
OWNED OR CONTROLLED BY ANALOG DEVICES.

SCHEMATIC					
QUAD MXFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9986					
DESIGN VIEW <DESIGN_VIEW>			DRAWING NO. 02-057438		REV A
PTD ENGINEER M. JONES / C. FRICK			SIZE D	SCALE 1:1	SHEET 3 OF 79

MXFE SUPPLIES

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



MXFE INPUT / OUTPUT

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ADC_P<3..0> SPI_SDIO

ADC_N<3..0>

SERDIN_P<3..0>

SERDIN_N<3..0>

SYNCIN_P

SYNCIN_N

RXEN<1..0>

TXEN<1..0>

SYSREF_P

SYSREF_N

RESETB

CLKIN_P

CLKIN_N

SPI_CSB

SPI_SCLK

GPIO<10..0>

DAC_P<3..0>

DAC_N<3..0>

SERDOUT_P<3..0>

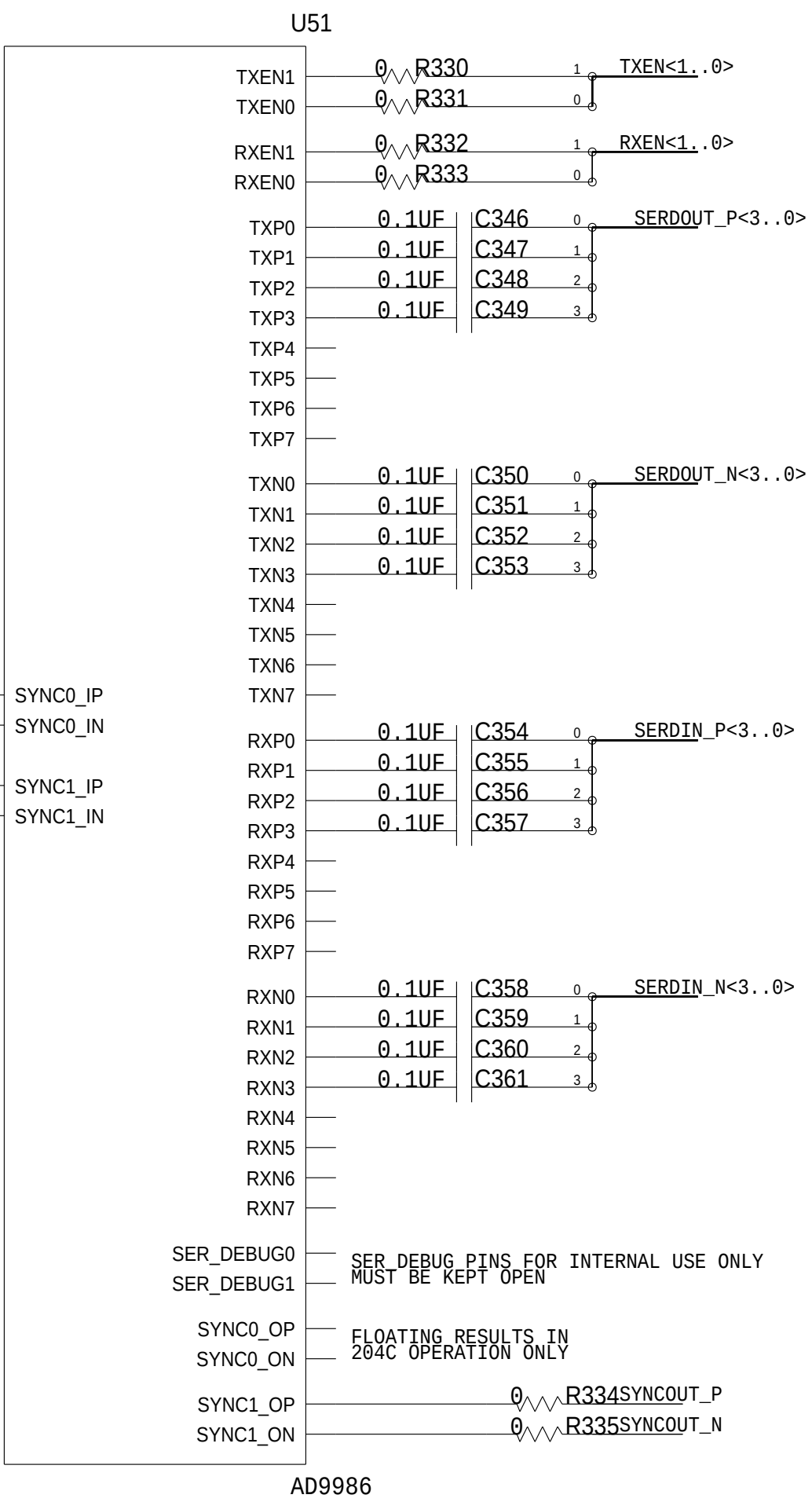
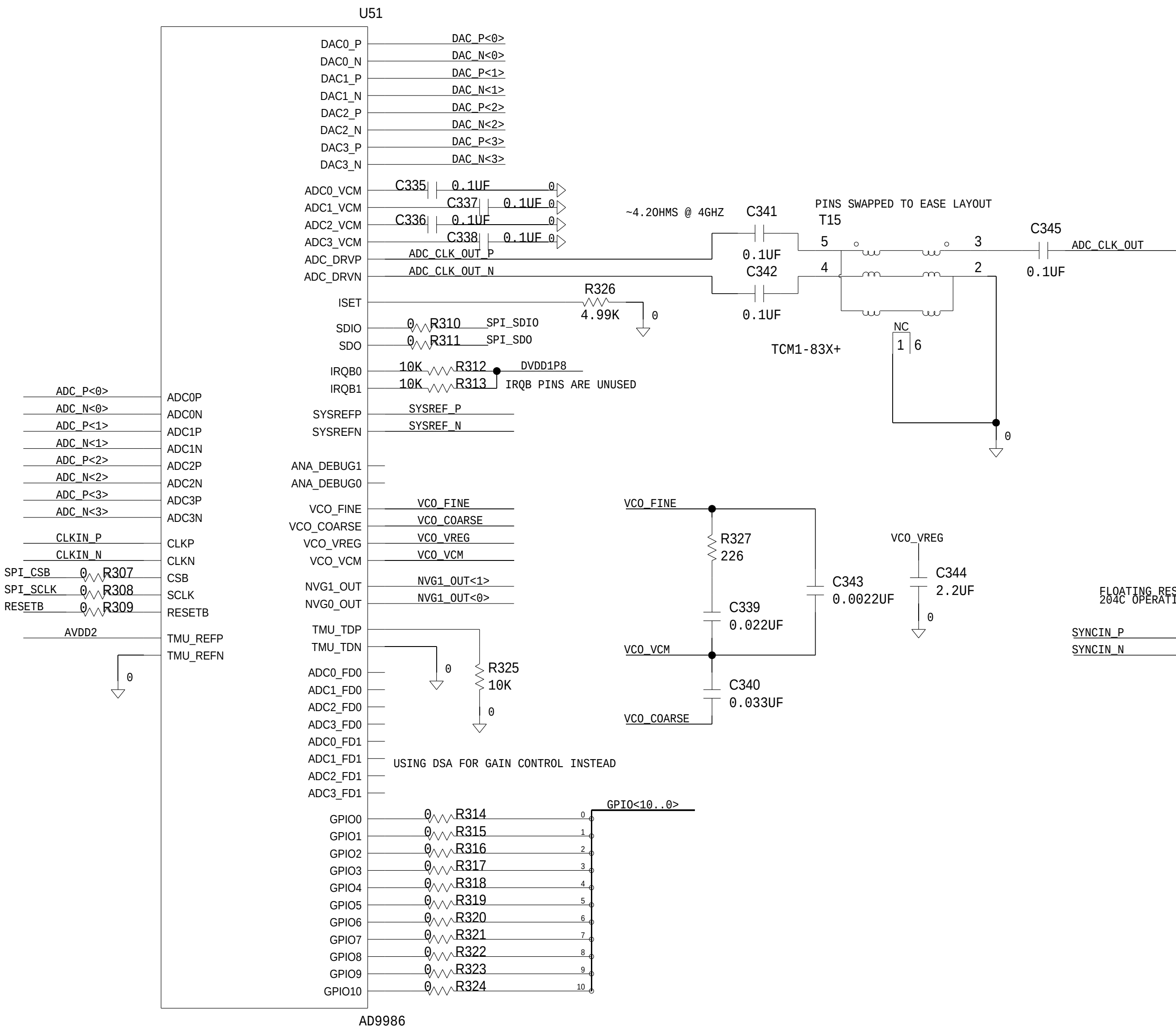
SERDOUT_N<3..0>

SYNCOUT_P

SYNCOUT_N

SPI_SD0

ADC_CLK_OUT

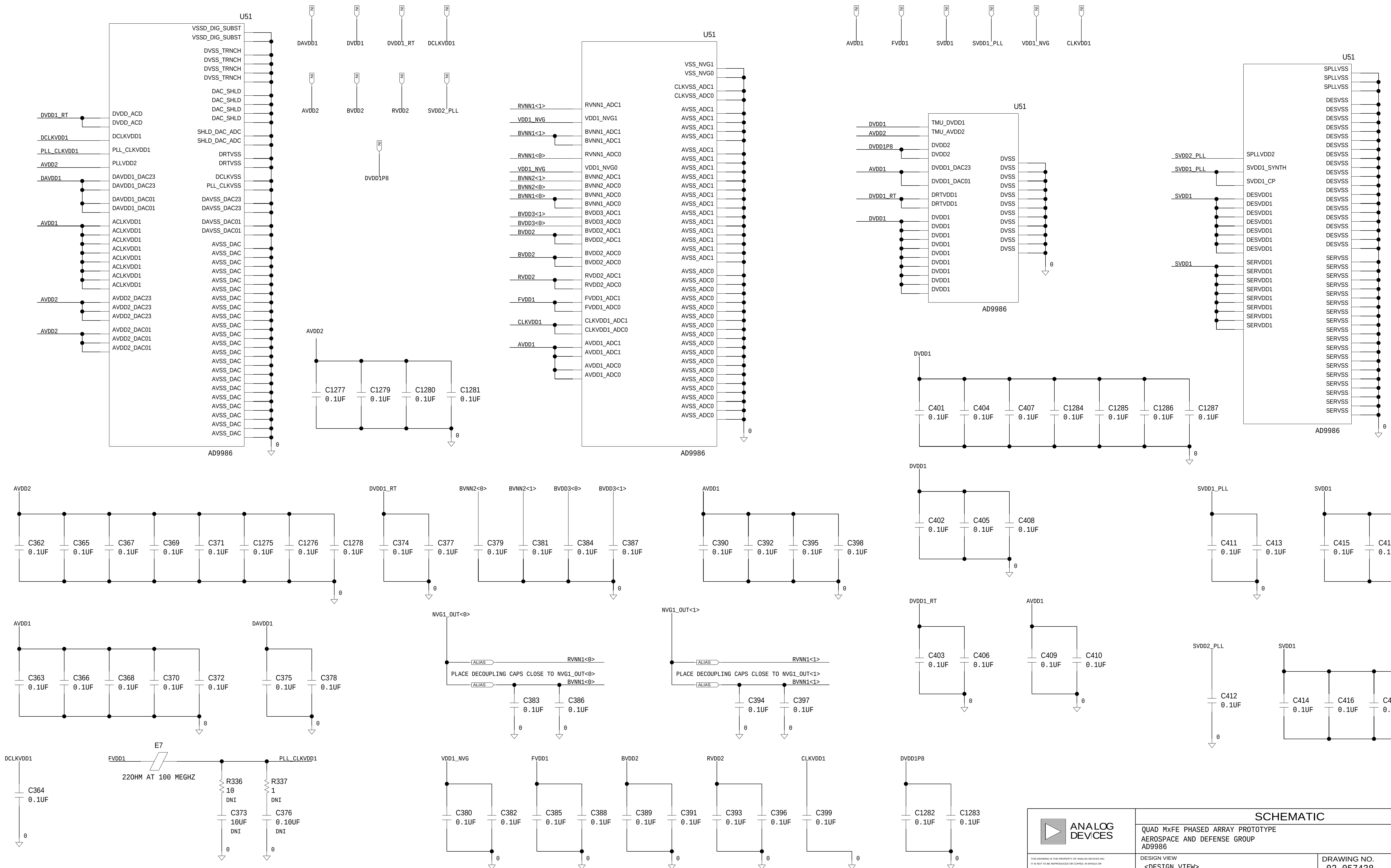


THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC.
IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR
IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS,
OR FOR ANY OTHER PURPOSES DETERMINANTAL TO THE INTERESTS
OF ANALOG DEVICES.
THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS
OWNED OR CONTROLLED BY ANALOG DEVICES.

SCHEMATIC					
QUAD MXFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9986					
DESIGN VIEW <DESIGN_VIEW>			DRAWING NO. 02-057438		REV A
PTD ENGINEER M. JONES / C. FRICK			SIZE D	SCALE 1:1	SHEET 5 OF 79

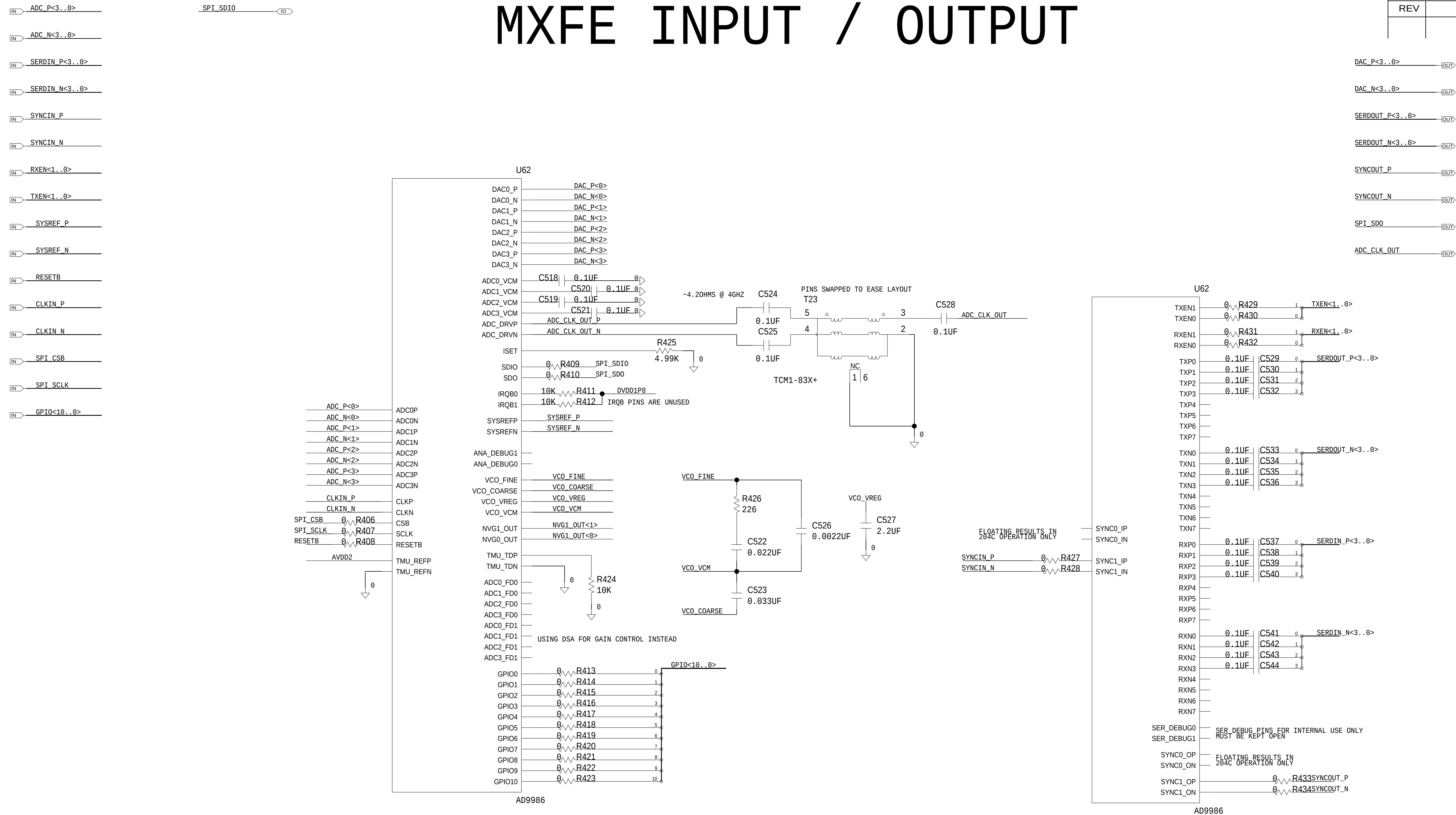
MXFE SUPPLIES

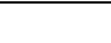
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



MXFE INPUT / OUTPUT

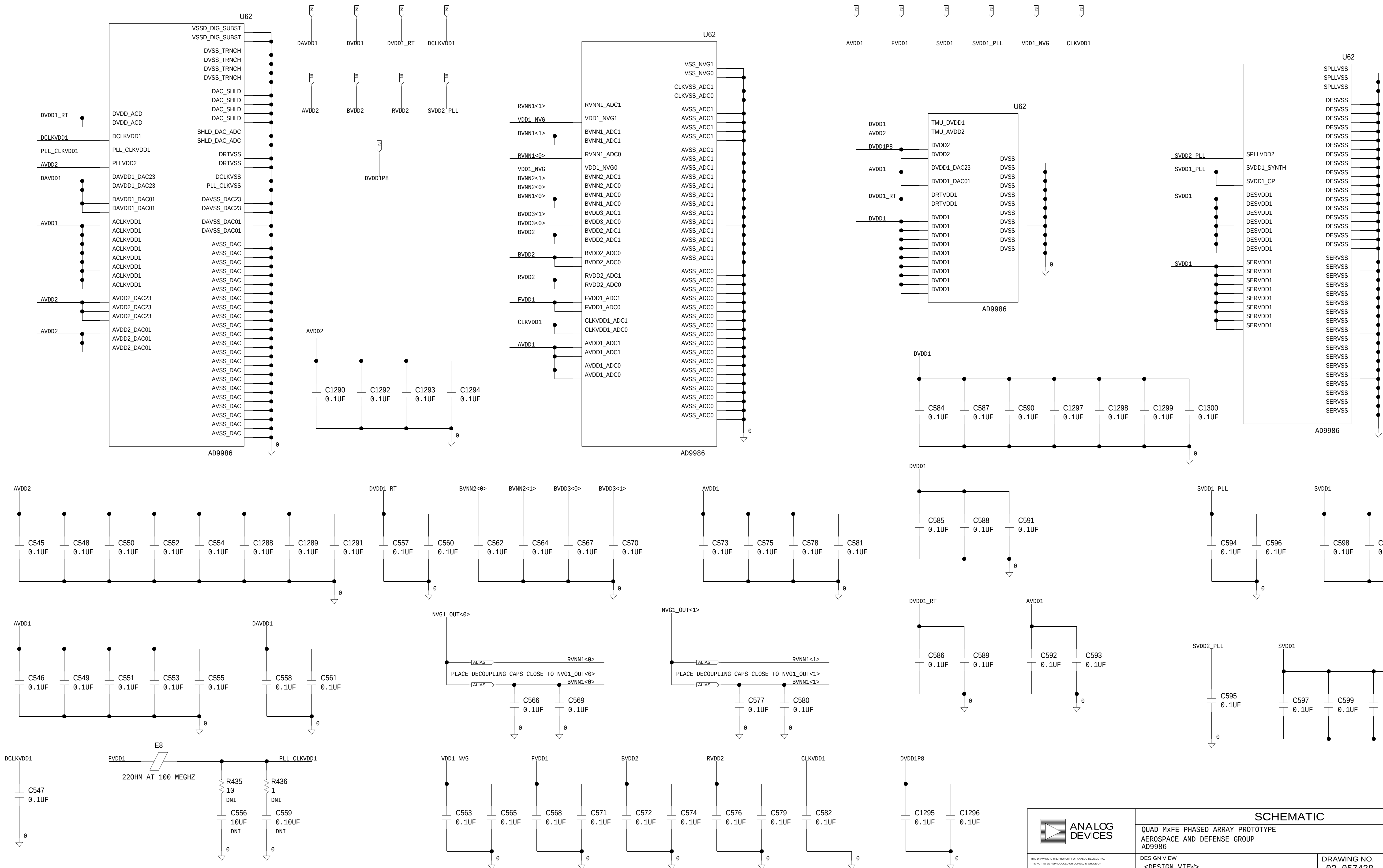
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



 ANALOG DEVICES	SCHEMATIC			
	QUAD MxFe PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9986			
THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSES PERTAINING TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT DESIGNER(S) MAY BE IMPROVED BY PATENTS OWNED OR CONTROLLED BY ANALOG DEVICES.	DESIGN VIEW <DESIGN_VIEW>		DRAWING NO. 02-057438	REV A
PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 7 OF 79	

MXFE SUPPLIES

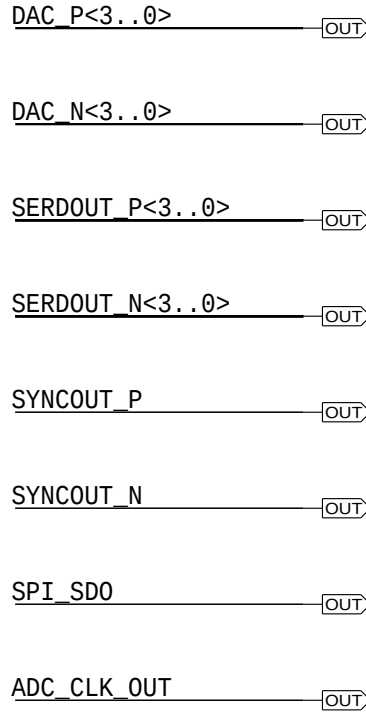
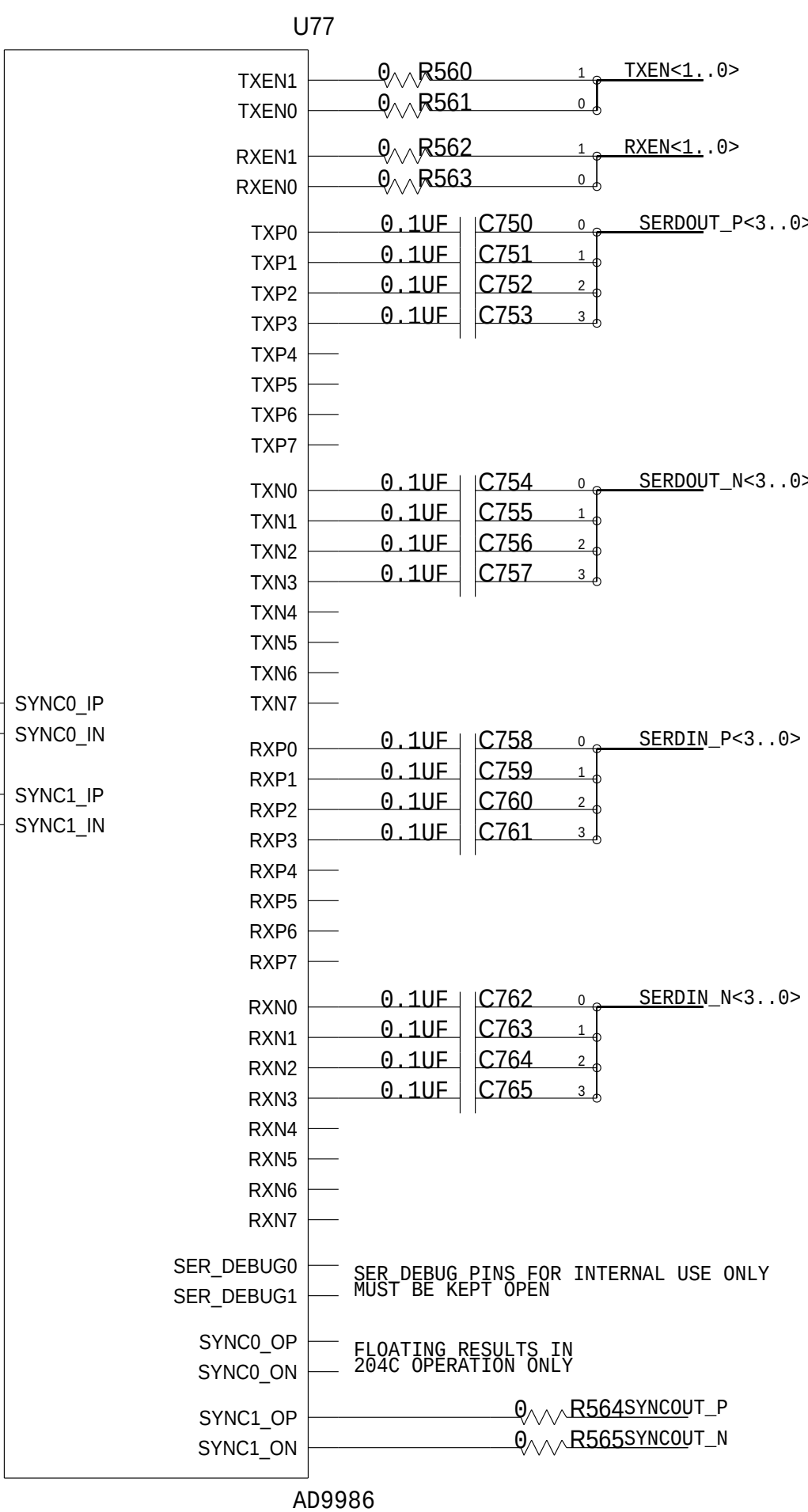
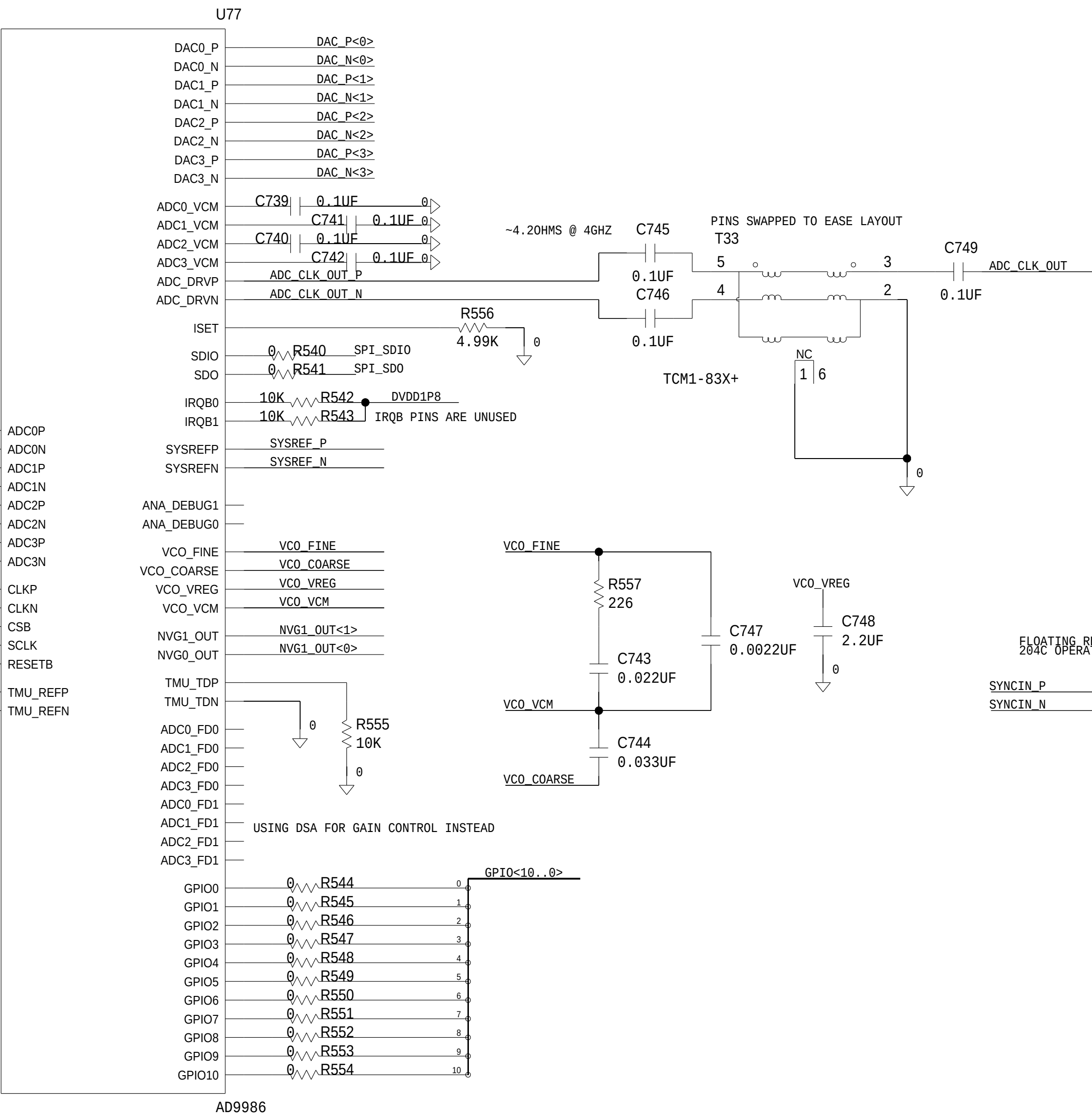
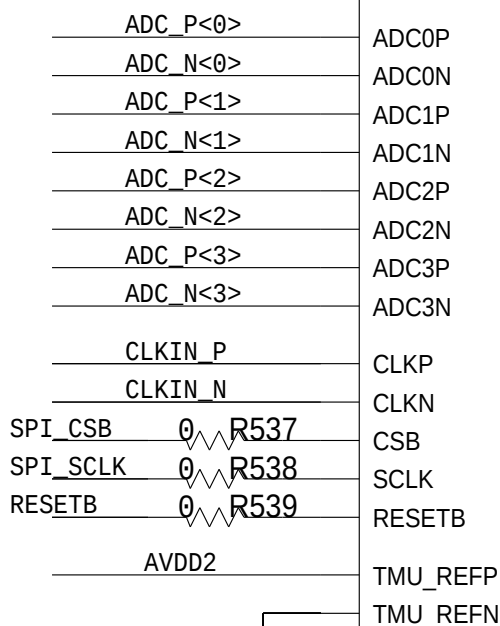
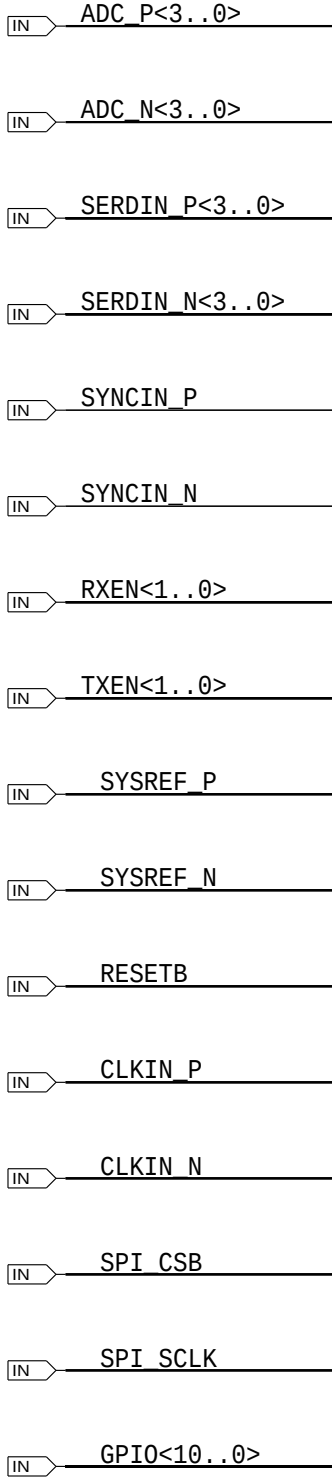
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



 ANALOG DEVICES	SCHEMATIC			
	QUAD MxFe PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9986			
THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES, INC. IF IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, A PENALTY OF CIVIL OR CRIMINAL PENALTIES TO THE VIOLATORS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREIN MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG ANALOG DEVICES.	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02-057438	REV A	
PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 8	OF 79

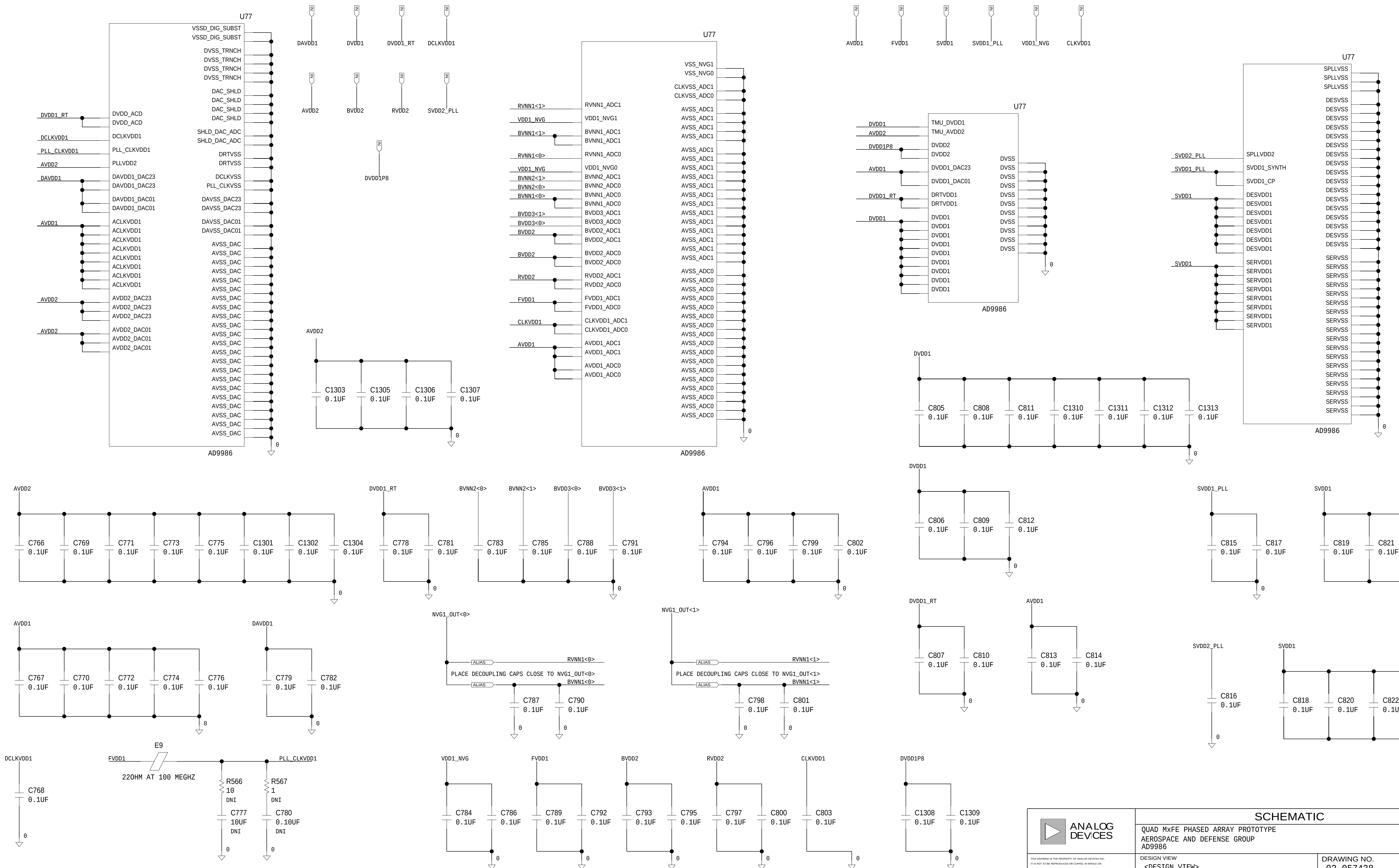
MXFE INPUT / OUTPUT

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



MXFE SUPPLIES

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

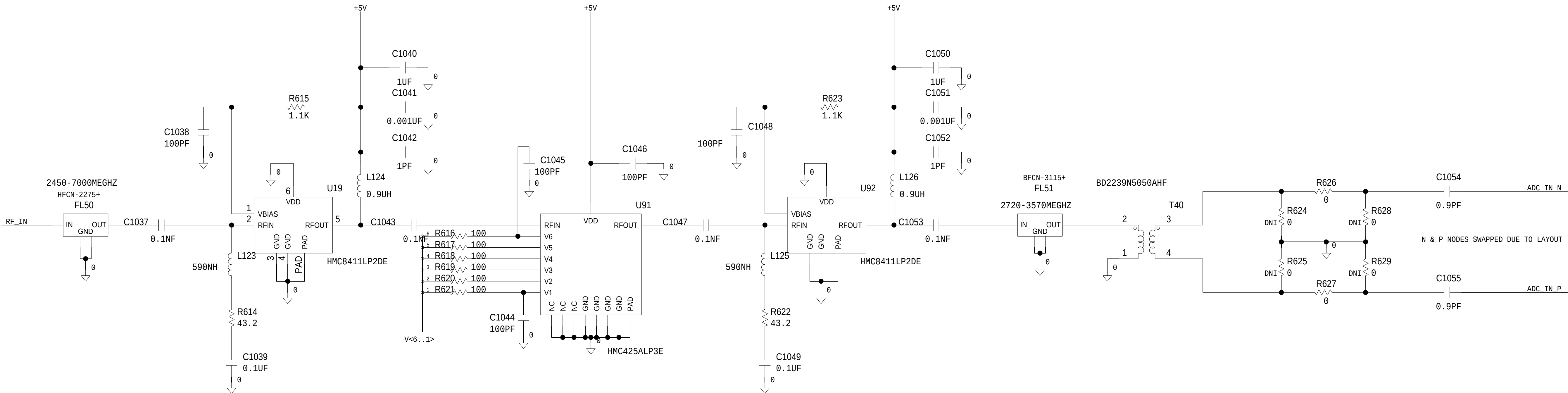
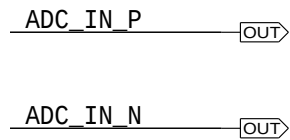
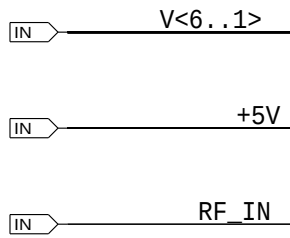


ADC FRONT END

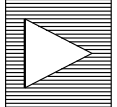
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANTICIPATED FE PERFORMANCE @ MINIMUM DSA ATTEN

S21 [1.3GHZ] = -67.4DB	S11 [2.7GHZ] = -15.3DB
S21 [2.7GHZ] = 20.7DB	S11 [3.2GHZ] = -15.5DB
S21 [3.2GHZ] = 21.5DB	S11 [3.7GHZ] = -19.0DB
S21 [3.7GHZ] = 20.5DB	
S21 [4.3GHZ] = -10.1DB	
S21 [5.3GHZ] = -31.4DB	



N & P NODES SWAPPED DUE TO LAYOUT



ANALOG
DEVICES

SCHEMATIC

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9986

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
M. JONES / C. FRICK

DRAWING NO.
02-057438

SIZE
D

SCALE
1:1

SHEET 11 OF 79

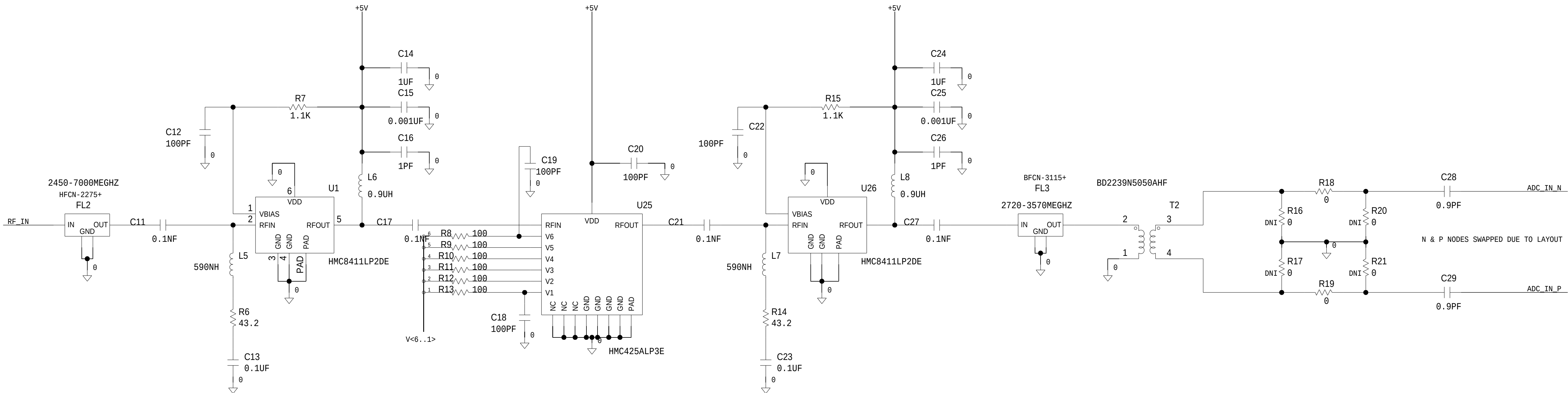
REV
A

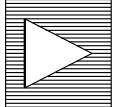
ADC FRONT END

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANTICIPATED FE PERFORMANCE @ MINIMUM DSA ATTEN

S21 [1.3GHZ] = -67.4DB	S11 [2.7GHZ] = -15.3DB
S21 [2.7GHZ] = 20.7DB	S11 [3.2GHZ] = -15.5DB
S21 [3.2GHZ] = 21.5DB	S11 [3.7GHZ] = -19.0DB
S21 [3.7GHZ] = 20.5DB	
S21 [4.3GHZ] = -10.1DB	
S21 [5.3GHZ] = -31.4DB	



 ANALOG DEVICES	SCHEMATIC			
	QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9986			
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02-057438		REV A
	PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 12 OF 79

ADC FRONT END

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

V<6...1>

+5V

RF_IN

ADC_IN_P

ADC_IN_N

ANTICIPATED FE PERFORMANCE @ MINIMUM DSA ATTEN

S21 [1.3GHZ] = -67.4DB

S21 [2.7GHZ] = 20.7DB

S21 [3.2GHZ] = 21.5DB

S21 [3.7GHZ] = 20.5DB

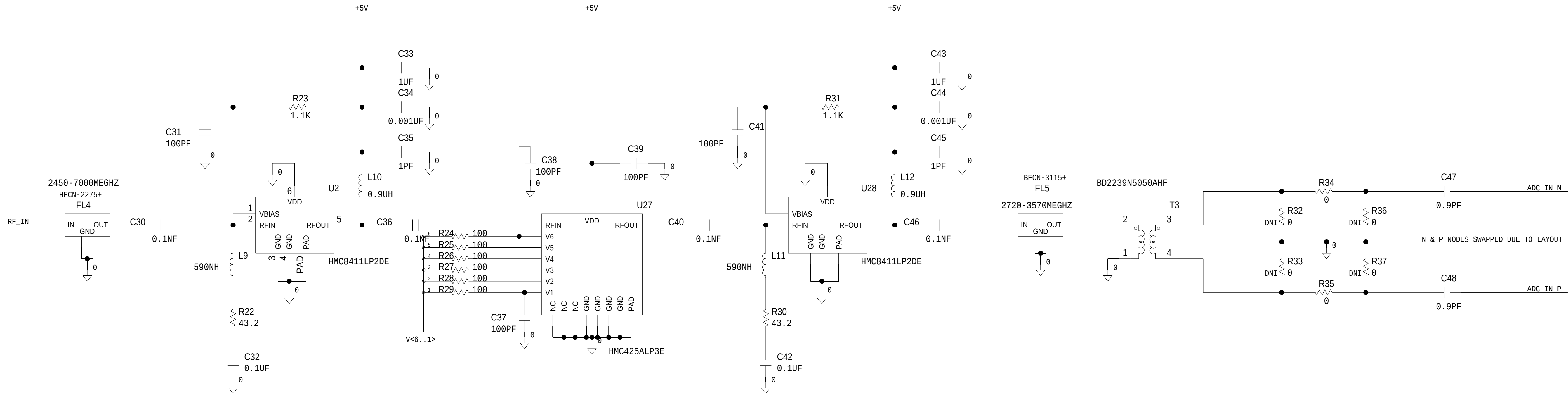
S21 [4.3GHZ] = -10.1DB

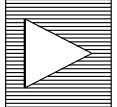
S21 [5.3GHZ] = -31.4DB

S11 [2.7GHZ] = -15.3DB

S11 [3.2GHZ] = -15.5DB

S11 [3.7GHZ] = -19.0DB





ANALOG
DEVICES

SCHEMATIC

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9986

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
M. JONES / C. FRICK

DRAWING NO.
02-057438

SIZE
D

SCALE
1:1

SHEET 13 OF 79

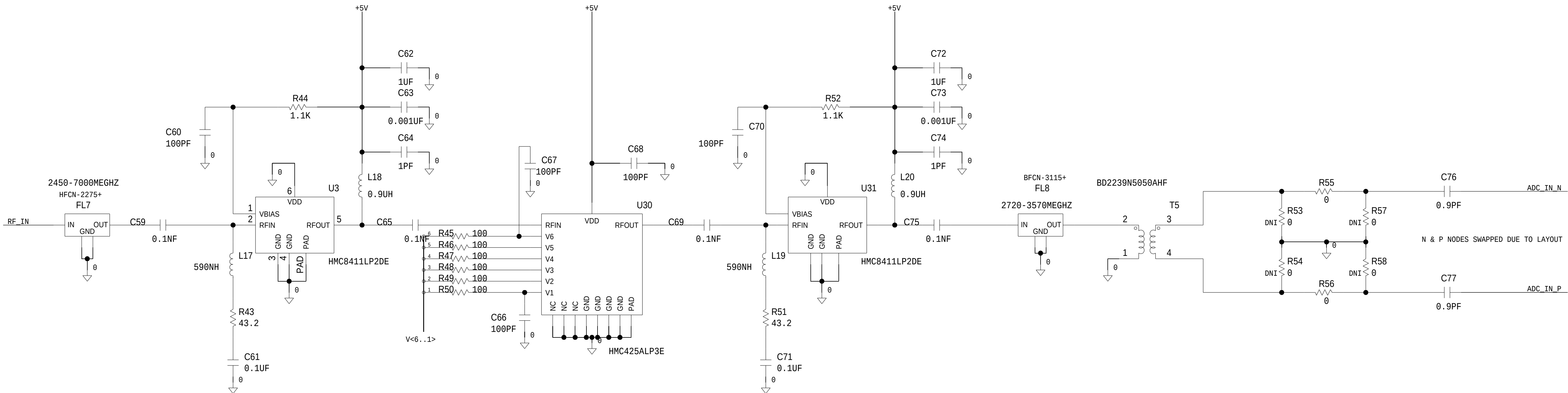
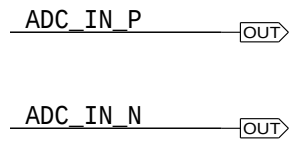
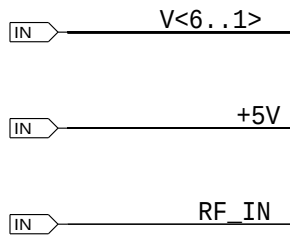
REV
A

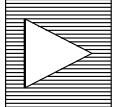
ADC FRONT END

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANTICIPATED FE PERFORMANCE @ MINIMUM DSA ATTEN

S21 [1.3GHZ] = -67.4DB	S11 [2.7GHZ] = -15.3DB
S21 [2.7GHZ] = 20.7DB	S11 [3.2GHZ] = -15.5DB
S21 [3.2GHZ] = 21.5DB	S11 [3.7GHZ] = -19.0DB
S21 [3.7GHZ] = 20.5DB	
S21 [4.3GHZ] = -10.1DB	
S21 [5.3GHZ] = -31.4DB	



 ANALOG DEVICES THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.	SCHEMATIC			
	QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9986			
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02-057438		REV A
	PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 14 OF 79

ADC FRONT END

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

V<6...1>

+5V

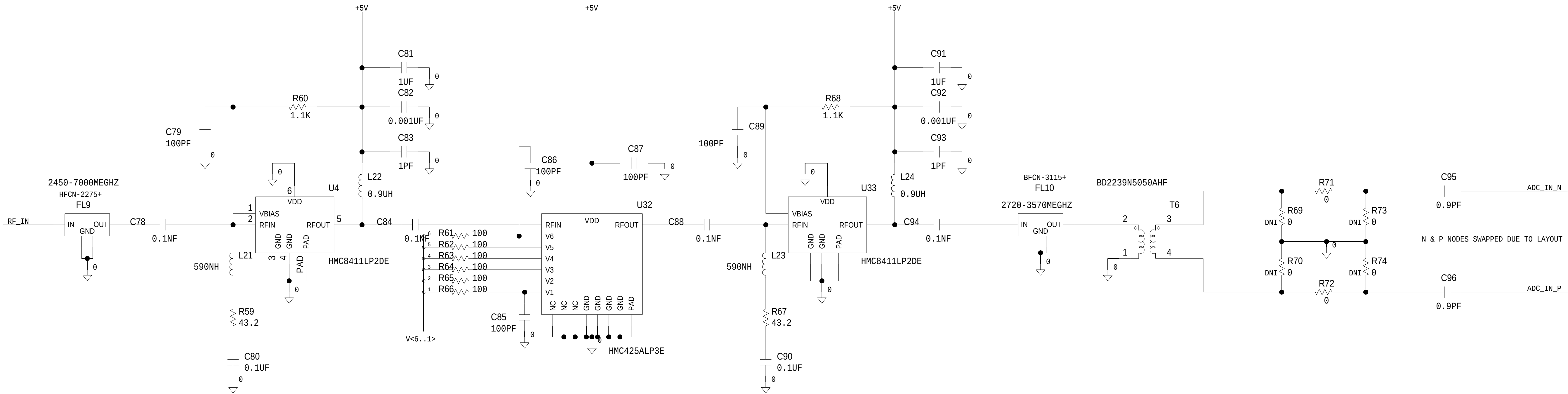
RF_IN

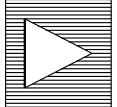
ADC_IN_P

ADC_IN_N

ANTICIPATED FE PERFORMANCE @ MINIMUM DSA ATTEN

S21 [1.3GHZ] = -67.4DB	S11 [2.7GHZ] = -15.3DB
S21 [2.7GHZ] = 20.7DB	S11 [3.2GHZ] = -15.5DB
S21 [3.2GHZ] = 21.5DB	S11 [3.7GHZ] = -19.0DB
S21 [3.7GHZ] = 20.5DB	
S21 [4.3GHZ] = -10.1DB	
S21 [5.3GHZ] = -31.4DB	





ANALOG
DEVICES

SCHEMATIC

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9986

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
M. JONES / C. FRICK

DRAWING NO.
02-057438

SIZE
D

SCALE
1:1

SHEET 15 OF 79

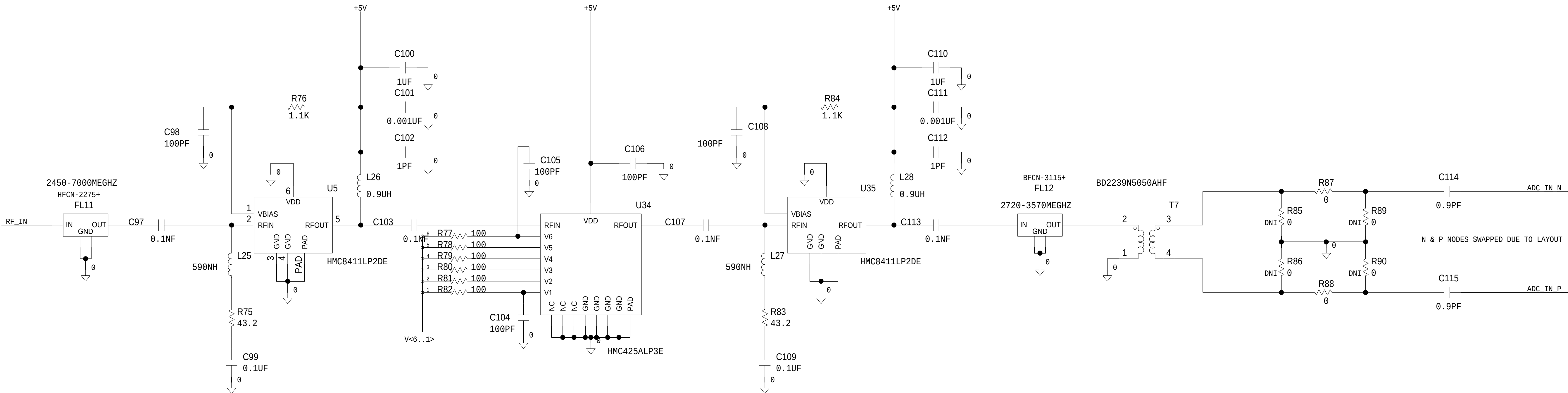
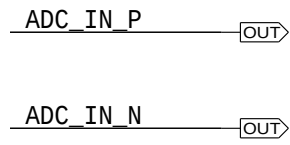
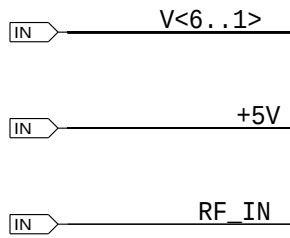
REV
A

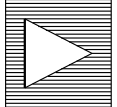
ADC FRONT END

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANTICIPATED FE PERFORMANCE @ MINIMUM DSA ATTEN

S21 [1.3GHZ] = -67.4DB	S11 [2.7GHZ] = -15.3DB
S21 [2.7GHZ] = 20.7DB	S11 [3.2GHZ] = -15.5DB
S21 [3.2GHZ] = 21.5DB	S11 [3.7GHZ] = -19.0DB
S21 [3.7GHZ] = 20.5DB	
S21 [4.3GHZ] = -10.1DB	
S21 [5.3GHZ] = -31.4DB	



**ANALOG
DEVICES**

SCHEMATIC

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9986

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
M. JONES / C. FRICK

DRAWING NO.
02-057438

SIZE
D

REV
A

SCALE
1:1

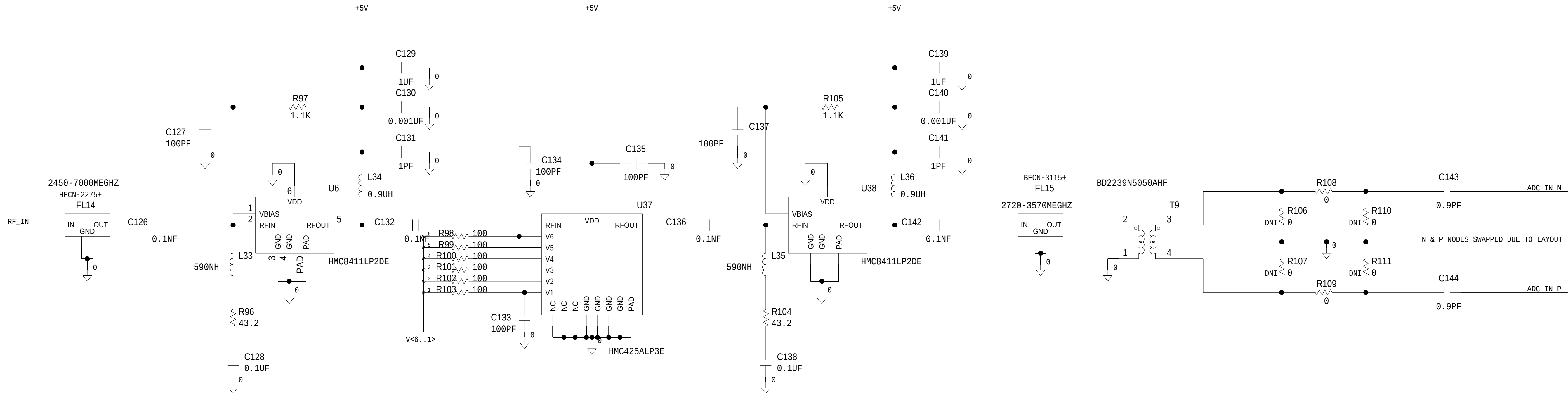
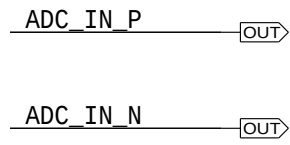
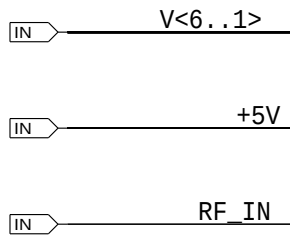
SHEET 16 OF 79

ADC FRONT END

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANTICIPATED FE PERFORMANCE @ MINIMUM DSA ATTEN

S21 [1.3GHZ] = -67.4DB	S11 [2.7GHZ] = -15.3DB
S21 [2.7GHZ] = 20.7DB	S11 [3.2GHZ] = -15.5DB
S21 [3.2GHZ] = 21.5DB	S11 [3.7GHZ] = -19.0DB
S21 [3.7GHZ] = 20.5DB	
S21 [4.3GHZ] = -10.1DB	
S21 [5.3GHZ] = -31.4DB	



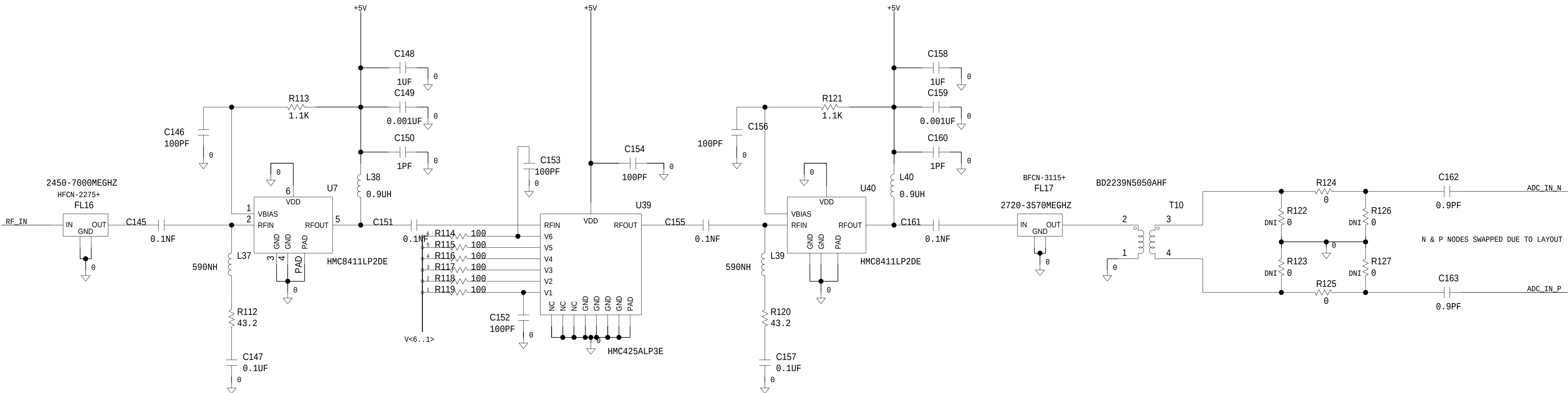
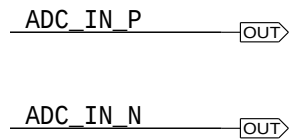
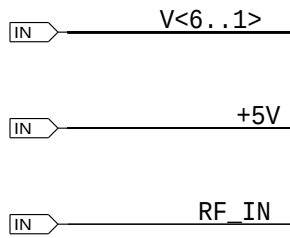
	SCHEMATIC			
	QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9986			
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02-057438		REV A
	PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 17 OF 79

ADC FRONT END

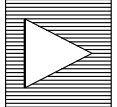
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANTICIPATED FE PERFORMANCE @ MINIMUM DSA ATTEN

S21 [1.3GHZ] = -67.4DB	S11 [2.7GHZ] = -15.3DB
S21 [2.7GHZ] = 20.7DB	S11 [3.2GHZ] = -15.5DB
S21 [3.2GHZ] = 21.5DB	S21 [3.7GHZ] = -19.0DB
S21 [3.7GHZ] = 20.5DB	
S21 [4.3GHZ] = -10.1DB	
S21 [5.3GHZ] = -31.4DB	



N & P NODES SWAPPED DUE TO LAYOUT



ANALOG
DEVICES

SCHEMATIC

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9986

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
M. JONES / C. FRICK

DRAWING NO.
02-057438

SIZE
D

SCALE
1:1

SHEET 18 OF 79

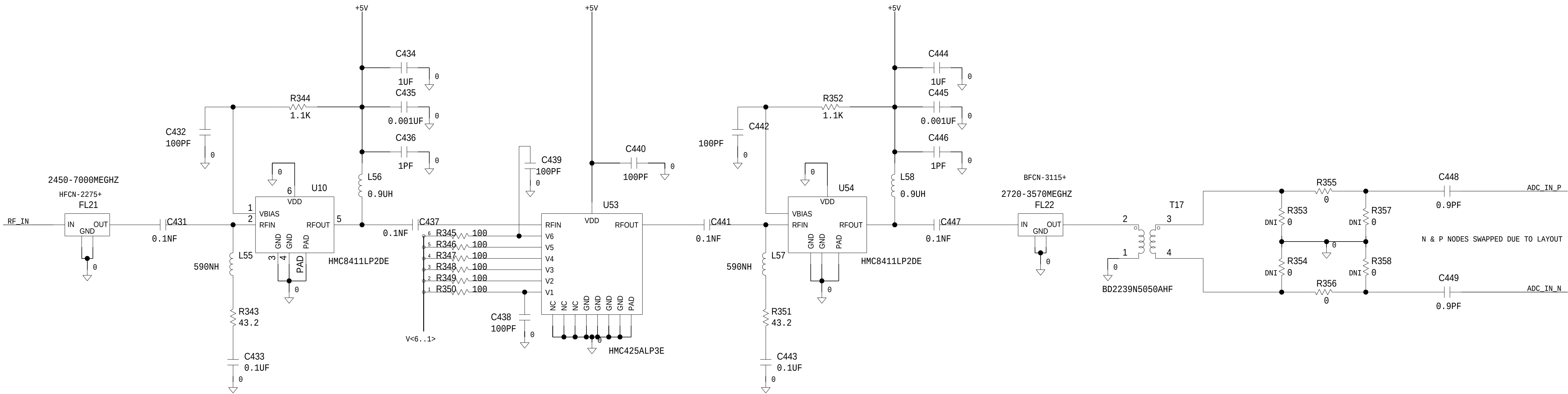
REV
A

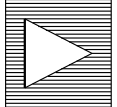
ADC FRONT END-WEST

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANTICIPATED FE PERFORMANCE @ MINIMUM DSA ATTEN

S21 [1.3GHZ] = -67.4DB	S11 [2.7GHZ] = -15.3DB
S21 [2.7GHZ] = 20.7DB	S11 [3.2GHZ] = -15.5DB
S21 [3.2GHZ] = 21.5DB	S11 [3.7GHZ] = -19.0DB
S21 [3.7GHZ] = 20.5DB	
S21 [4.3GHZ] = -10.1DB	
S21 [5.3GHZ] = -31.4DB	



**ANALOG
DEVICES**

SCHEMATIC

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9986

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
M. JONES / C. FRICK

DRAWING NO.
02-057438

SIZE
D

REV
A

SCALE
1:1

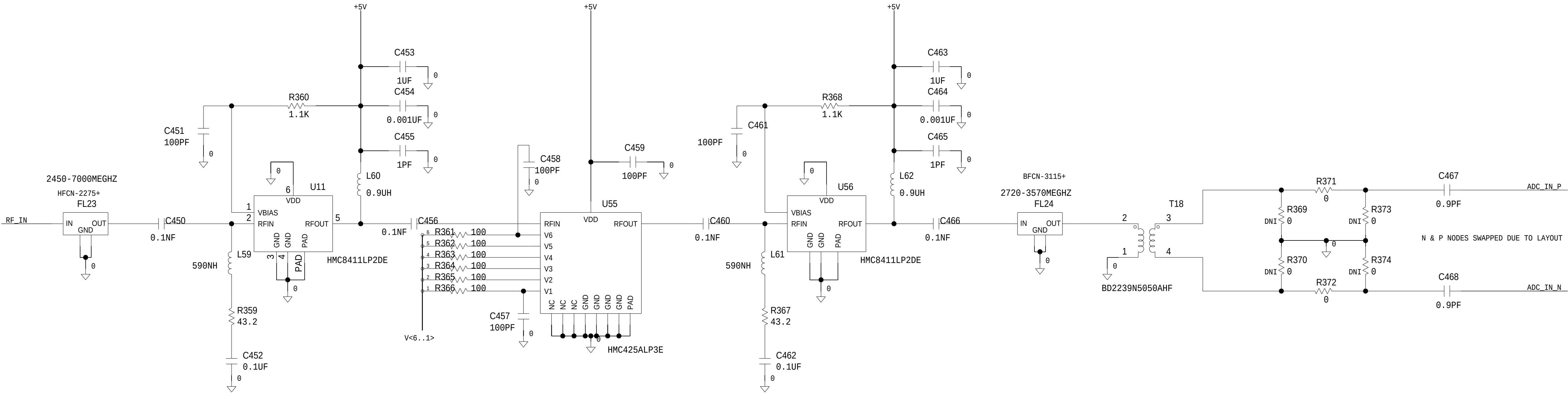
SHEET 19 OF 79

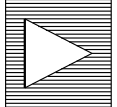
ADC FRONT END-WEST

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANTICIPATED FE PERFORMANCE @ MINIMUM DSA ATTEN

S21 [1.3GHZ] = -67.4DB	S11 [2.7GHZ] = -15.3DB
S21 [2.7GHZ] = 20.7DB	S11 [3.2GHZ] = -15.5DB
S21 [3.2GHZ] = 21.5DB	S11 [3.7GHZ] = -19.0DB
S21 [3.7GHZ] = 20.5DB	
S21 [4.3GHZ] = -10.1DB	
S21 [5.3GHZ] = -31.4DB	



**ANALOG
DEVICES**

SCHEMATIC

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9986

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
M. JONES / C. FRICK

DRAWING NO.
02-057438

SIZE
D

REV
A

SCALE
1:1

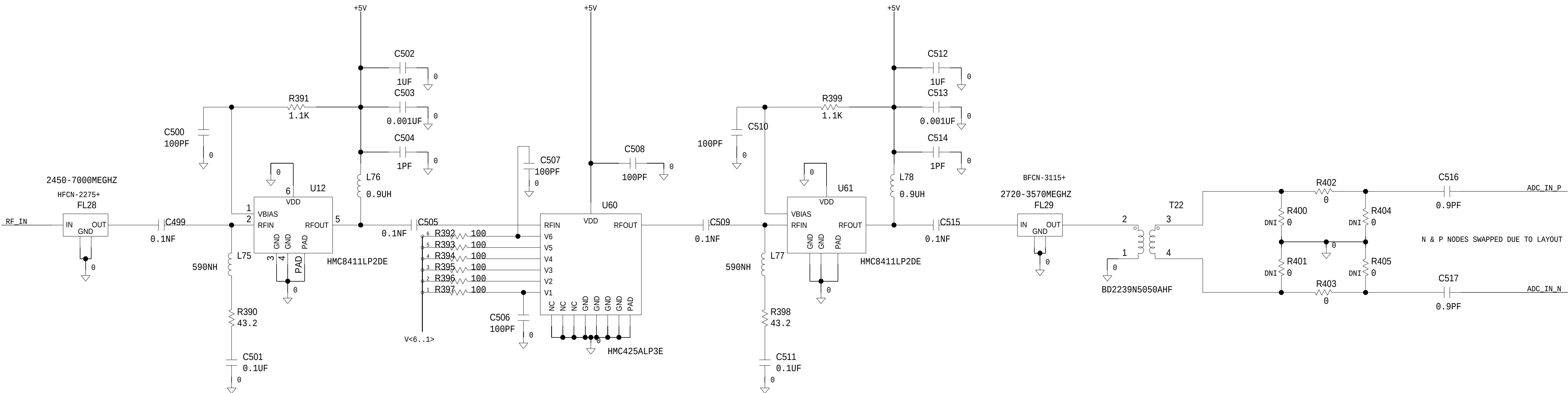
SHEET 20 OF 79

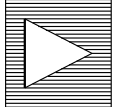
ADC FRONT END-WEST

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANTICIPATED FE PERFORMANCE @ MINIMUM DSA ATTEN

S21 [1.3GHZ] = -67.4DB	S11 [2.7GHZ] = -15.3DB
S21 [2.7GHZ] = 20.7DB	S11 [3.2GHZ] = -15.5DB
S21 [3.2GHZ] = 21.5DB	S11 [3.7GHZ] = -19.0DB
S21 [3.7GHZ] = 20.5DB	
S21 [4.3GHZ] = -10.1DB	
S21 [5.3GHZ] = -31.4DB	



**ANALOG
DEVICES**

SCHEMATIC

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9986

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
M. JONES / C. FRICK

DRAWING NO.
02-057438

SIZE
D

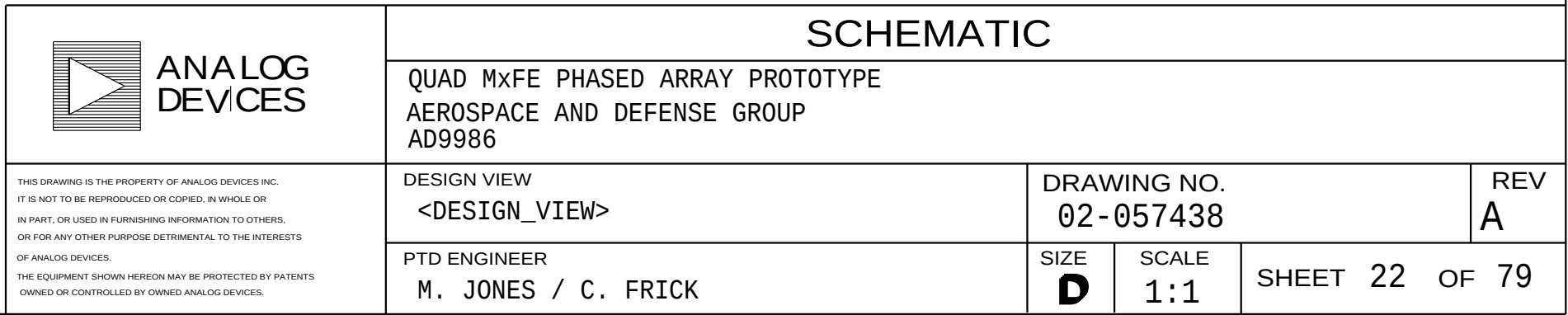
REV
A

SCALE
1:1

SHEET 21 OF 79

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

S21	[1.3GHZ]	=	-67.4DB		
S21	[2.7GHZ]	=	20.7DB	S11	[2.7GHZ] = -15.3DB
S21	[3.2GHZ]	=	21.5DB	S11	[3.2GHZ] = -15.5DB
S21	[3.7GHZ]	=	20.5DB	S11	[3.7GHZ] = -19.0DB
S21	[4.3GHZ]	=	-10.1DB		
S21	[5.3GHZ]	=	-31.4DB		

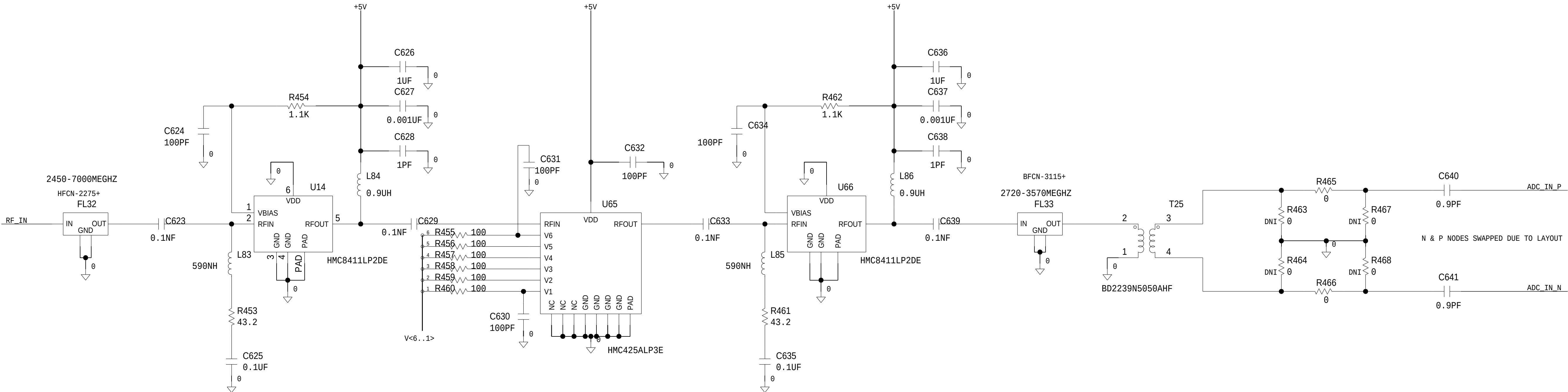


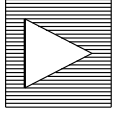
ADC FRONT END-WEST

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANTICIPATED FE PERFORMANCE @ MINIMUM DSA ATTEN

S21 [1.3GHZ] = -67.4DB	S11 [2.7GHZ] = -15.3DB
S21 [2.7GHZ] = 20.7DB	S11 [3.2GHZ] = -15.5DB
S21 [3.2GHZ] = 21.5DB	S11 [3.7GHZ] = -19.0DB
S21 [3.7GHZ] = 20.5DB	
S21 [4.3GHZ] = -10.1DB	
S21 [5.3GHZ] = -31.4DB	



**ANALOG
DEVICES**

SCHEMATIC

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9986

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
M. JONES / C. FRICK

DRAWING NO.
02-057438

SIZE
D

REV
A

SCALE
1:1

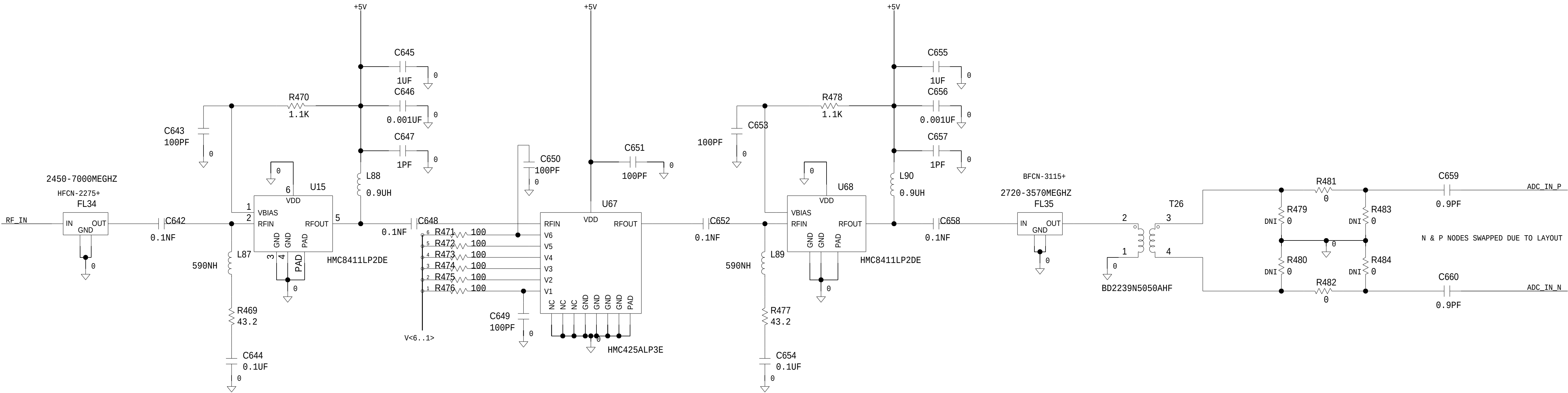
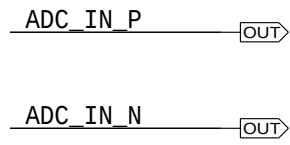
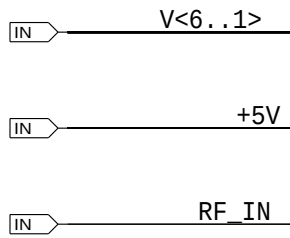
SHEET 23 OF 79

ADC FRONT END-WEST

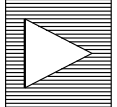
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANTICIPATED FE PERFORMANCE @ MINIMUM DSA ATTEN

S21 [1.3GHZ] = -67.4DB	S11 [2.7GHZ] = -15.3DB
S21 [2.7GHZ] = 20.7DB	S11 [3.2GHZ] = -15.5DB
S21 [3.2GHZ] = 21.5DB	S11 [3.7GHZ] = -19.0DB
S21 [3.7GHZ] = 20.5DB	
S21 [4.3GHZ] = -10.1DB	
S21 [5.3GHZ] = -31.4DB	



N & P NODES SWAPPED DUE TO LAYOUT



ANALOG
DEVICES

SCHEMATIC

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9986

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
M. JONES / C. FRICK

DRAWING NO.
02-057438

SIZE
D

SCALE
1:1

SHEET 24 OF 79

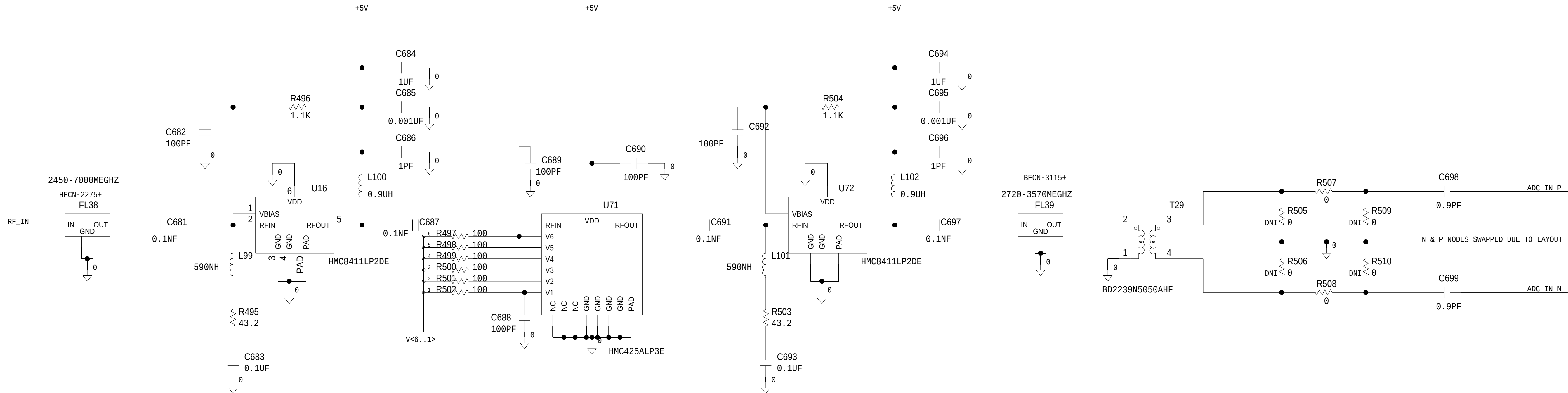
REV
A

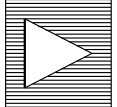
ADC FRONT END-WEST

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANTICIPATED FE PERFORMANCE @ MINIMUM DSA ATTEN

S21 [1.3GHZ] = -67.4DB	S11 [2.7GHZ] = -15.3DB
S21 [2.7GHZ] = 20.7DB	S11 [3.2GHZ] = -15.5DB
S21 [3.2GHZ] = 21.5DB	S11 [3.7GHZ] = -19.0DB
S21 [3.7GHZ] = 20.5DB	
S21 [4.3GHZ] = -10.1DB	
S21 [5.3GHZ] = -31.4DB	



**ANALOG
DEVICES**

SCHEMATIC

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9986

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
M. JONES / C. FRICK

DRAWING NO.
02-057438

SIZE
D

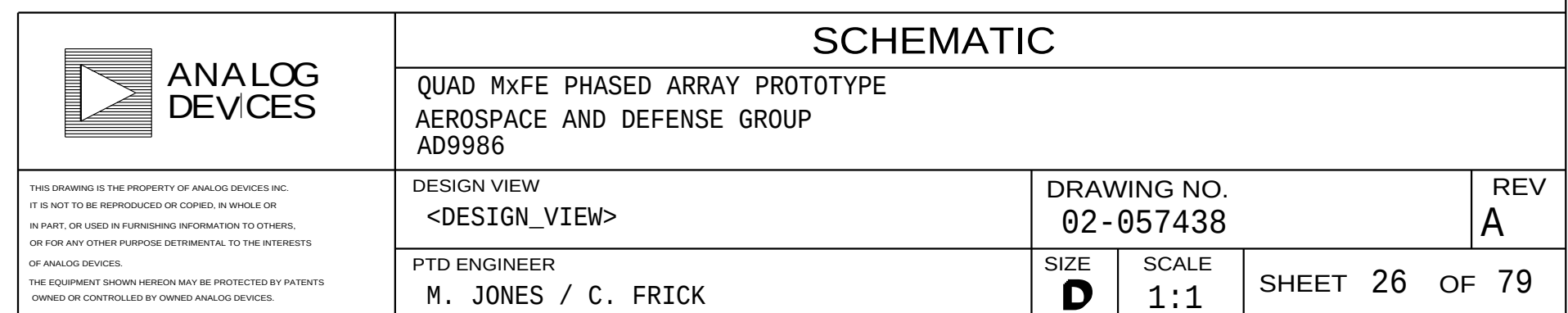
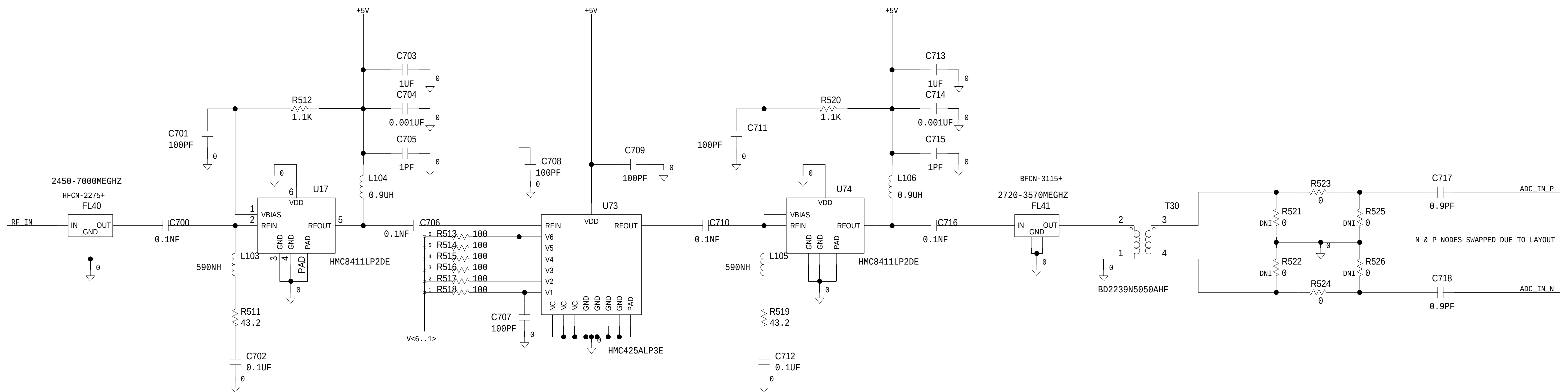
REV
A

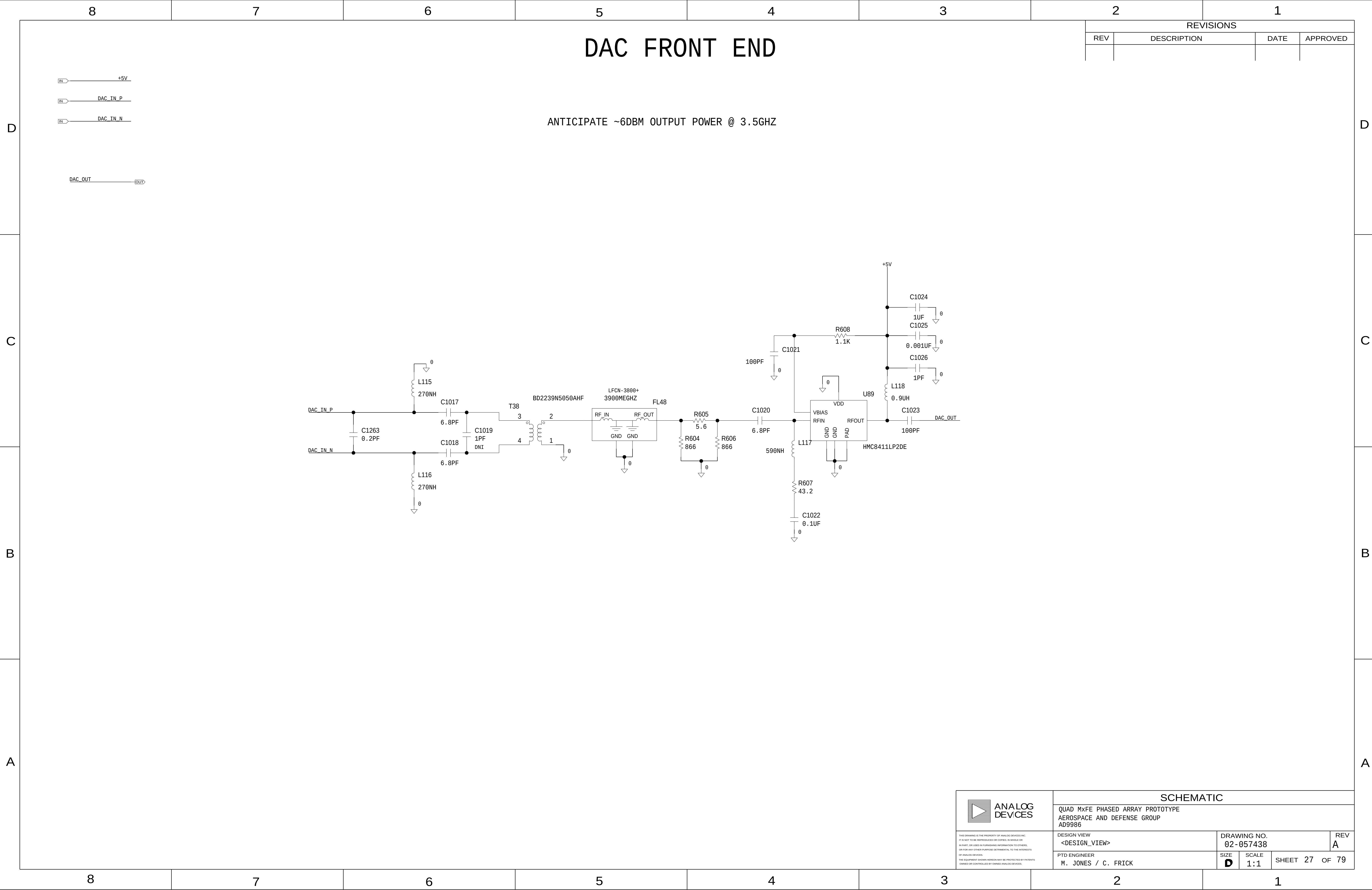
SCALE
1:1

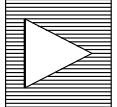
SHEET 25 OF 79

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

S21	[1.3GHz]	=	-67.4dB		
S21	[2.7GHz]	=	20.7dB	S11	[2.7GHz] = -15.3dB
S21	[3.2GHz]	=	21.5dB	S11	[3.2GHz] = -15.5dB
S21	[3.7GHz]	=	20.5dB	S11	[3.7GHz] = -19.0dB
S21	[4.3GHz]	=	-10.1dB		
S21	[5.3GHz]	=	-31.4dB		

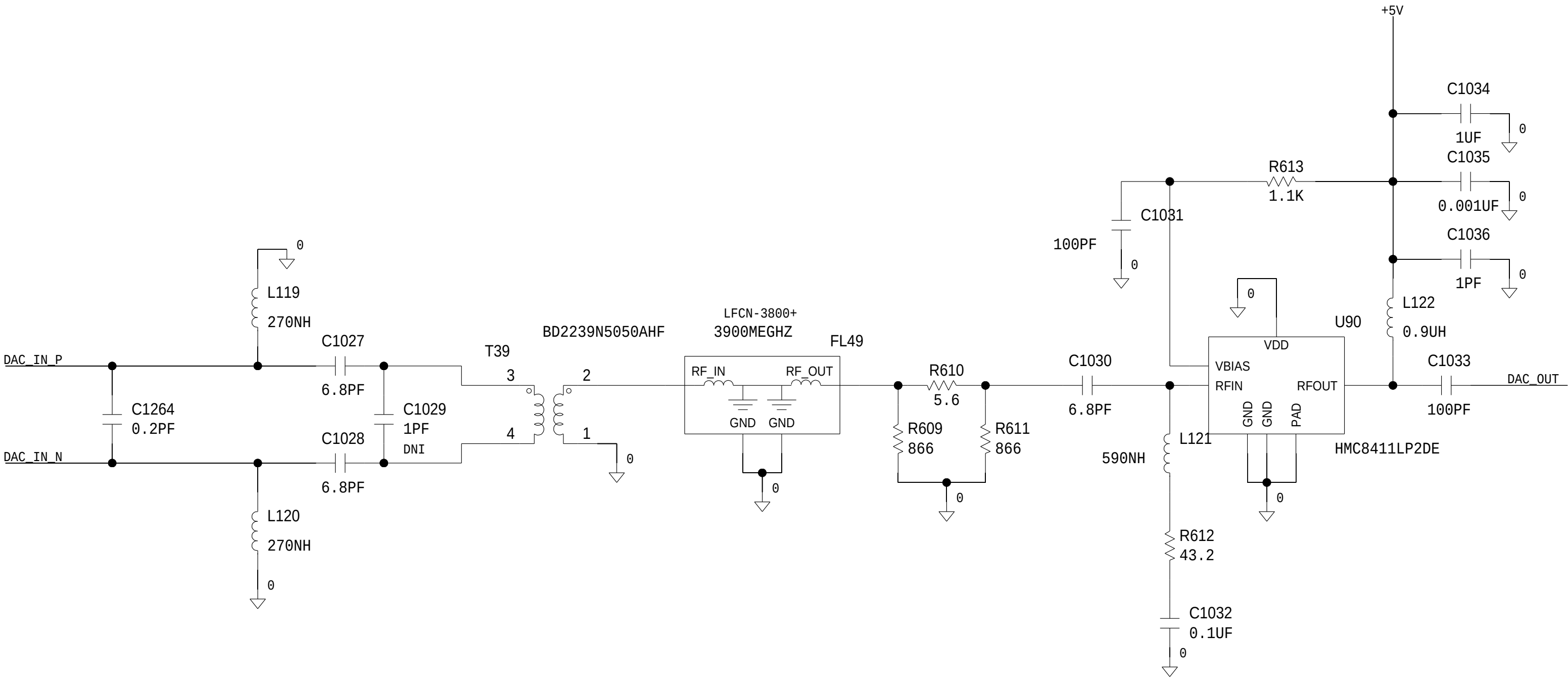




 ANALOG DEVICES THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.	SCHEMATIC			
	QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9986			
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02-057438		REV A
	PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 27 OF 79

DAC FRONT END

ANTICIPATE ~6DBM OUTPUT POWER @ 3.5GHZ

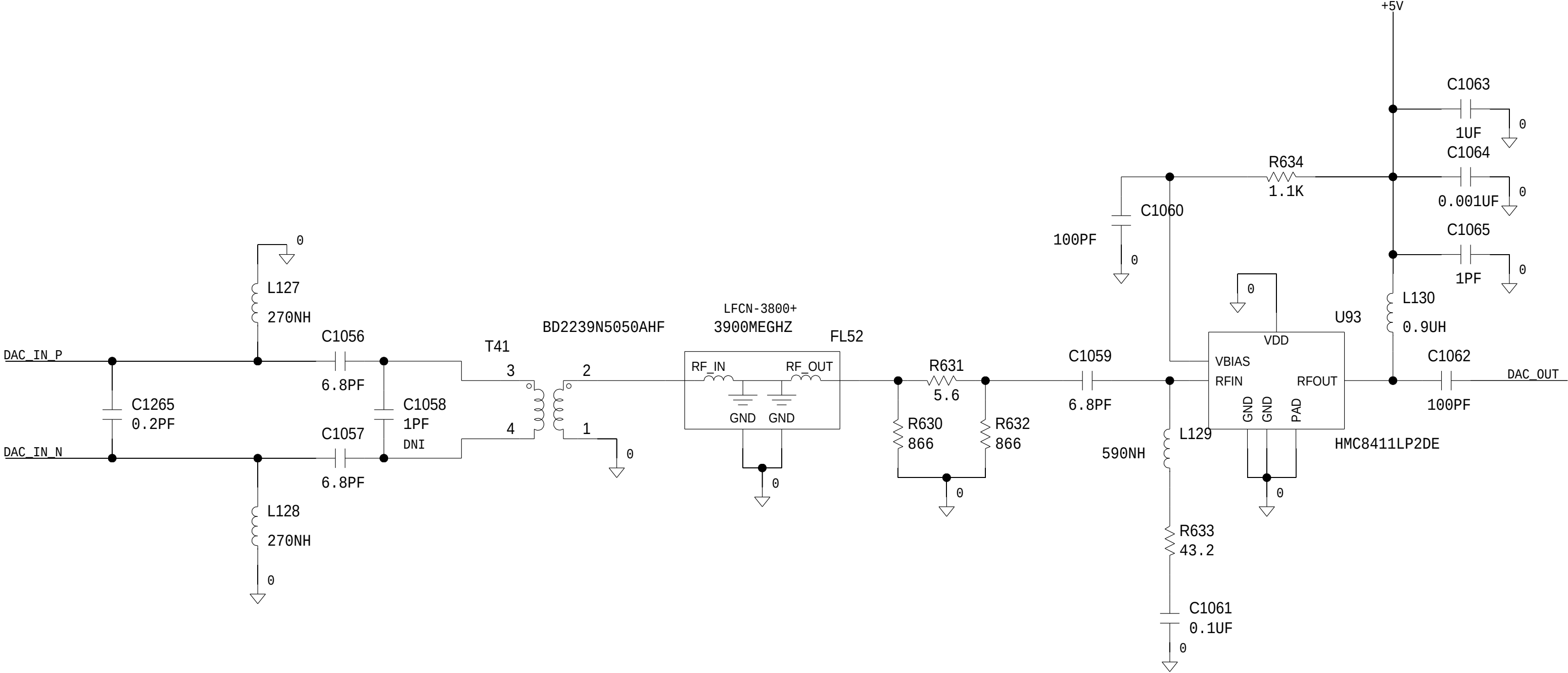


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

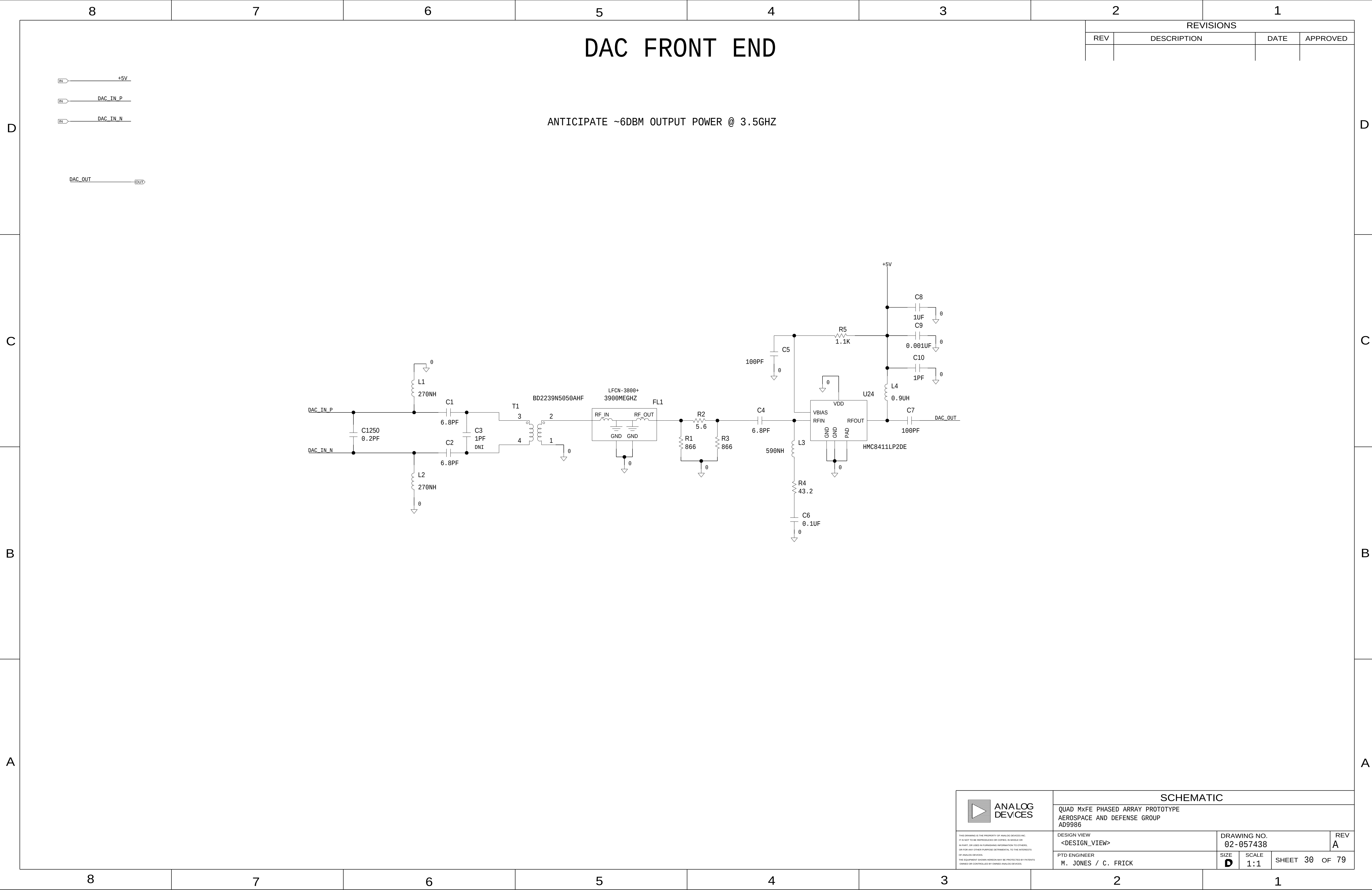
 ANALOG DEVICES	SCHEMATIC			
	QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9986			
THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSES PERTAINING TO THE INTERESTS OF ANALOG DEVICES. ALL EQUIPMENT AND/OR DRAWINGS MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY OWNED ANALOG DEVICES	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02-057438	REV A	
PDT ENGINEER M. JONES / C. FRICK	CONTROL BY D	SCALE 1:1	SHEET 28 OF 79	

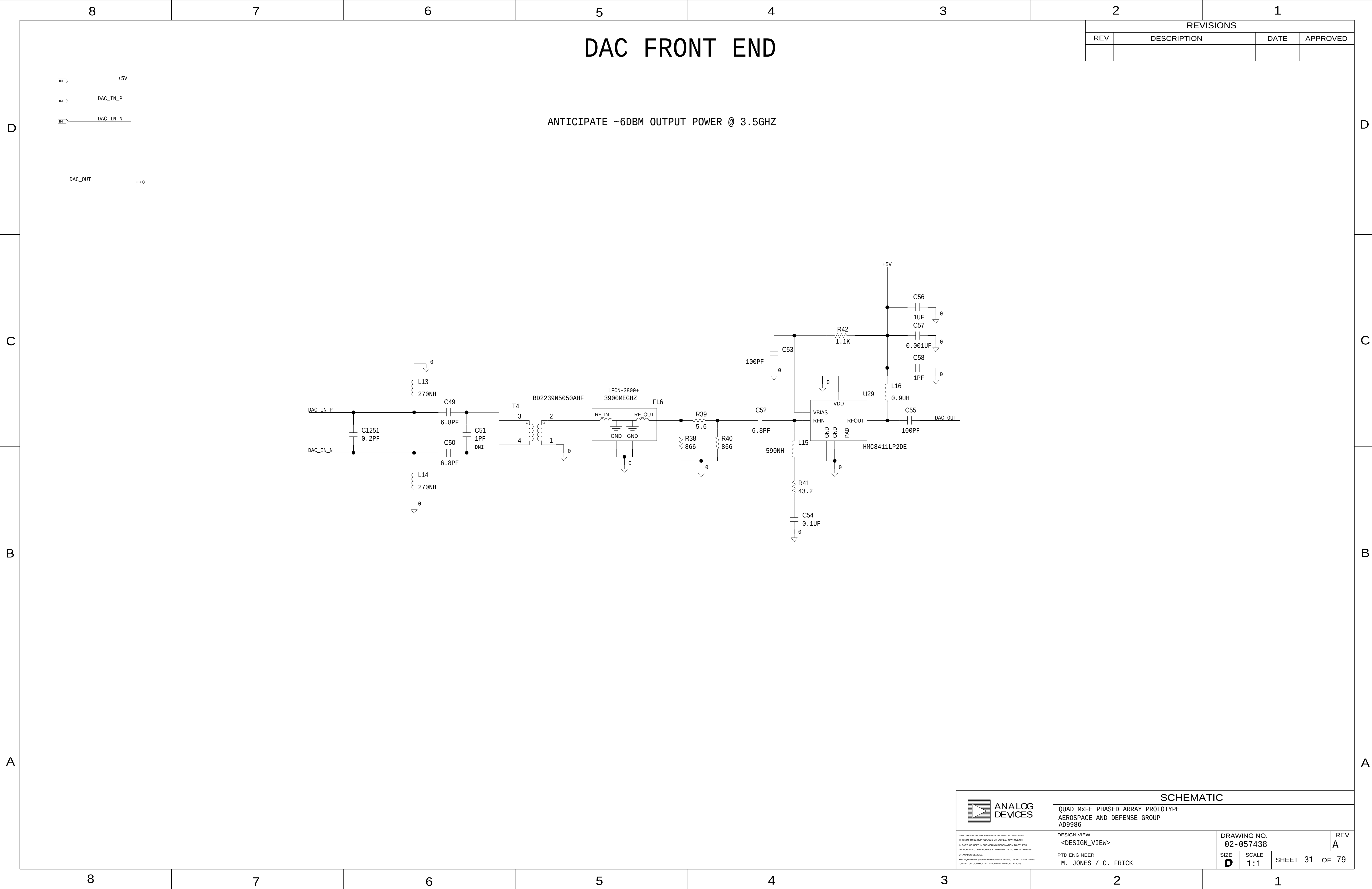
DAC FRONT END

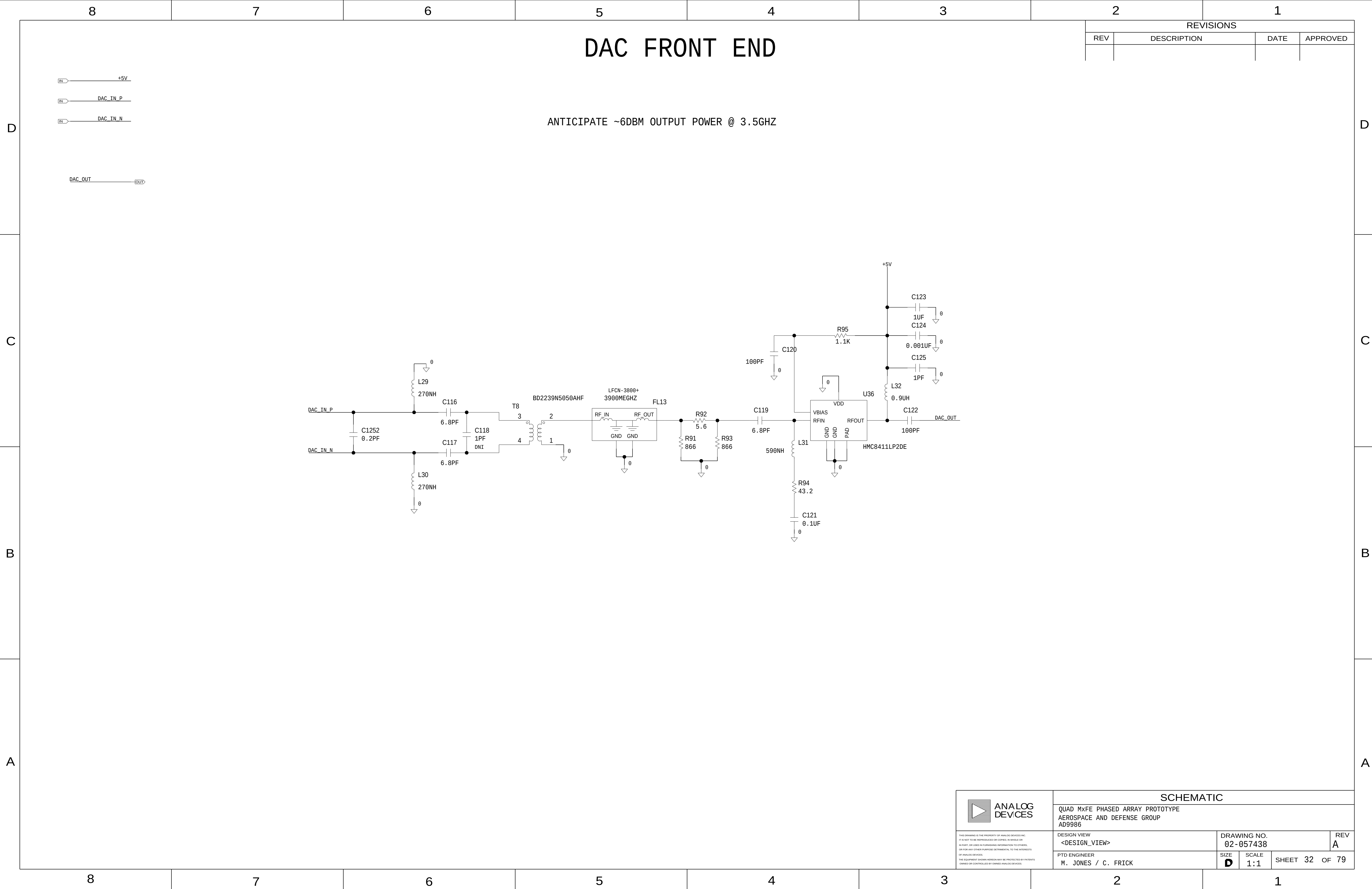
ANTICIPATE ~6DBM OUTPUT POWER @ 3.5GHZ

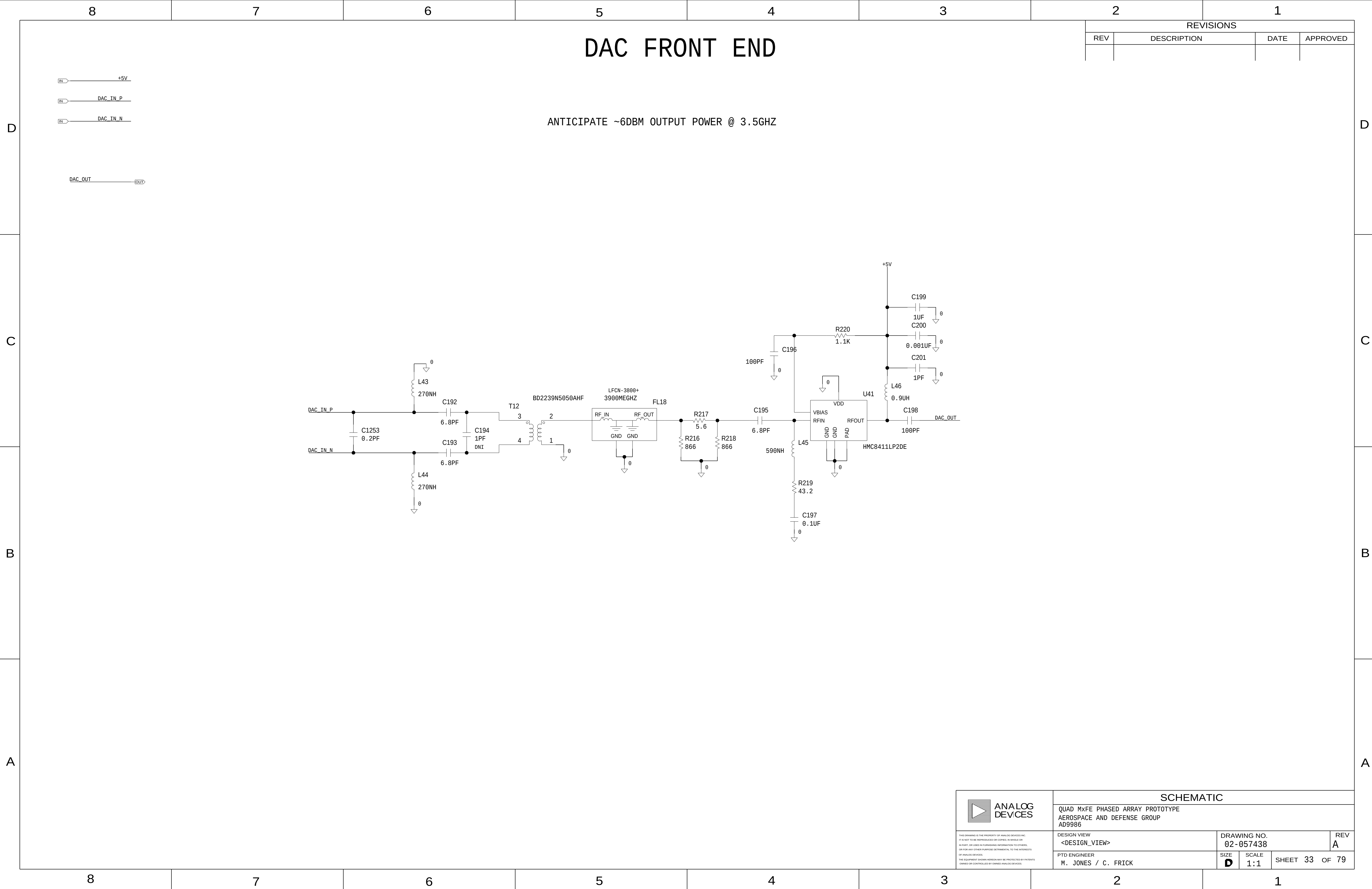


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



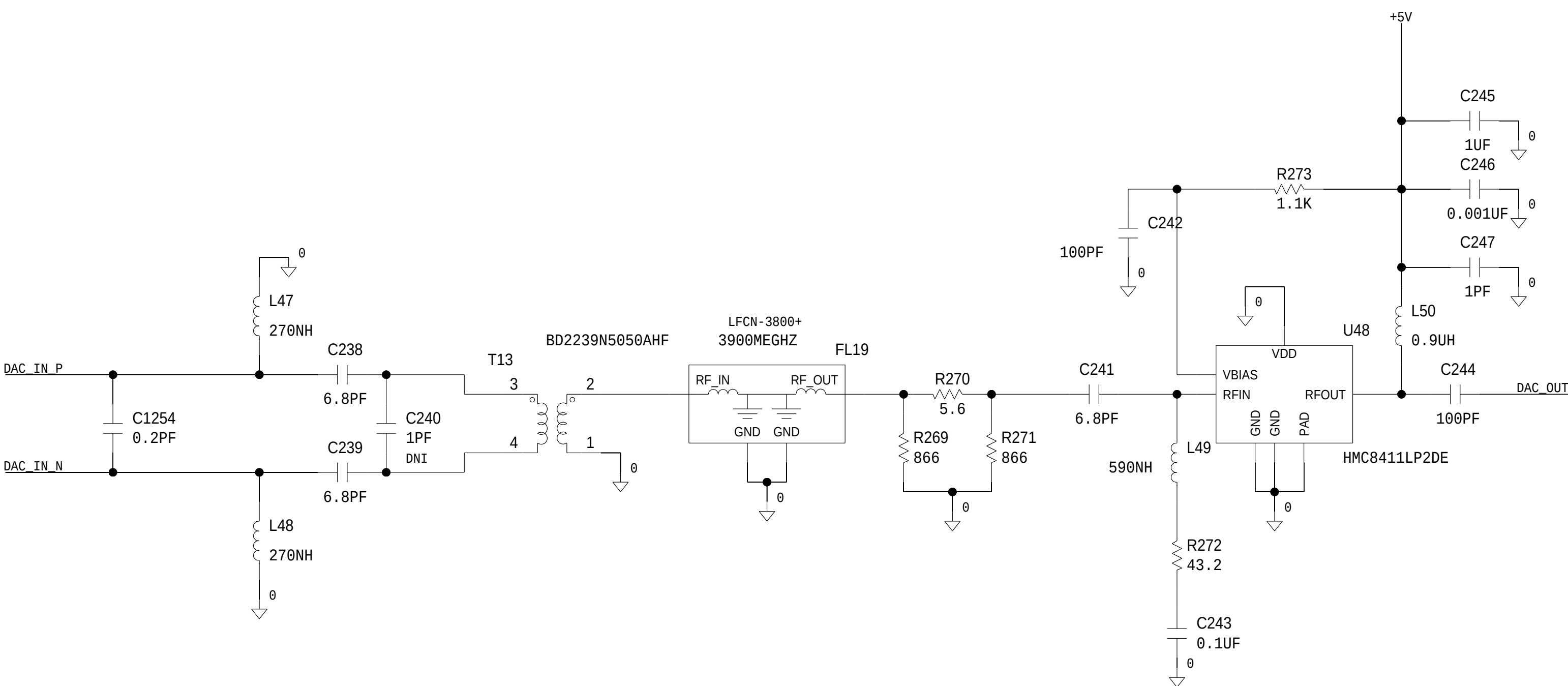




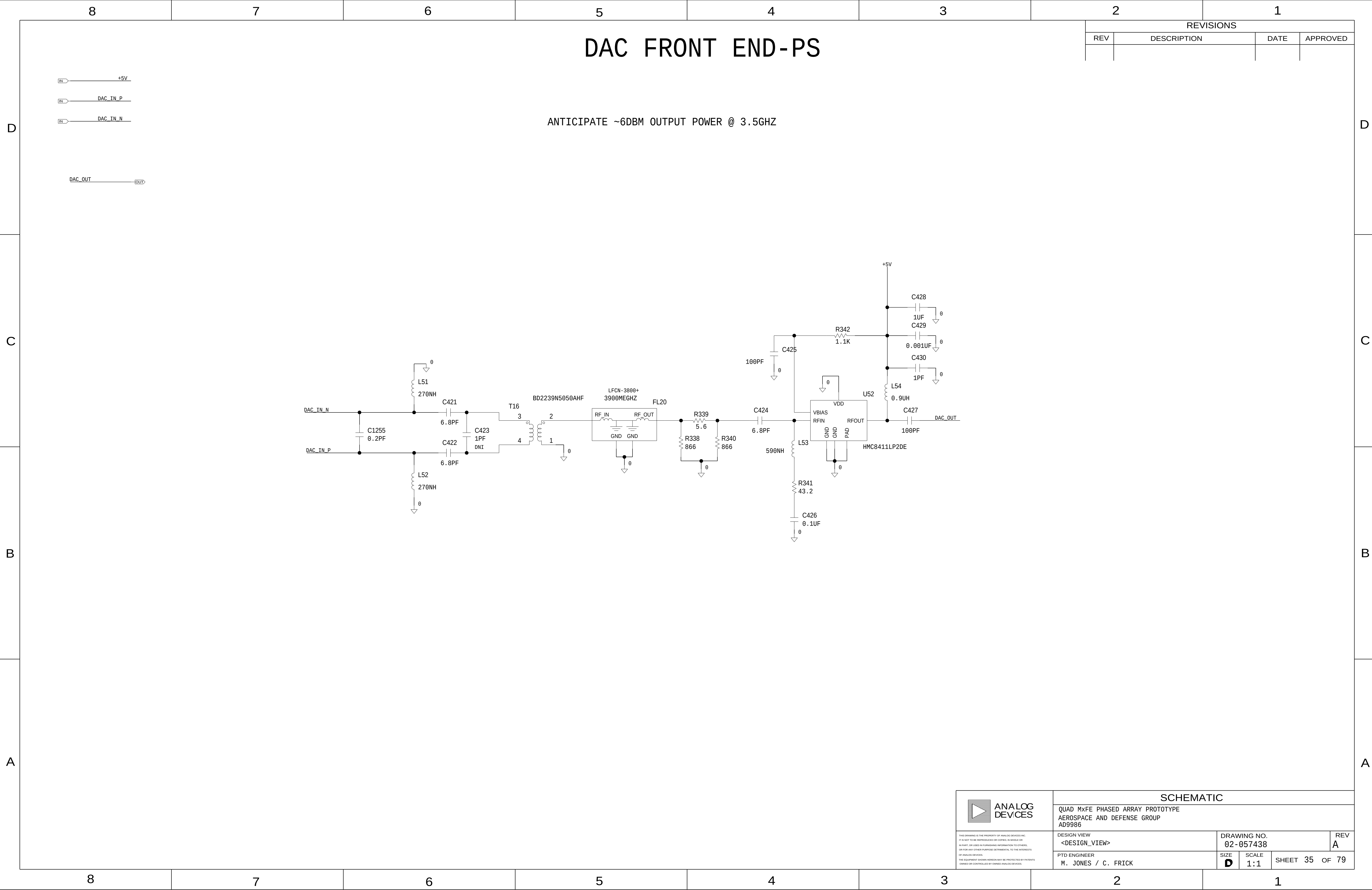


DAC FRONT END

ANTICIPATE ~6DBM OUTPUT POWER @ 3.5GH.

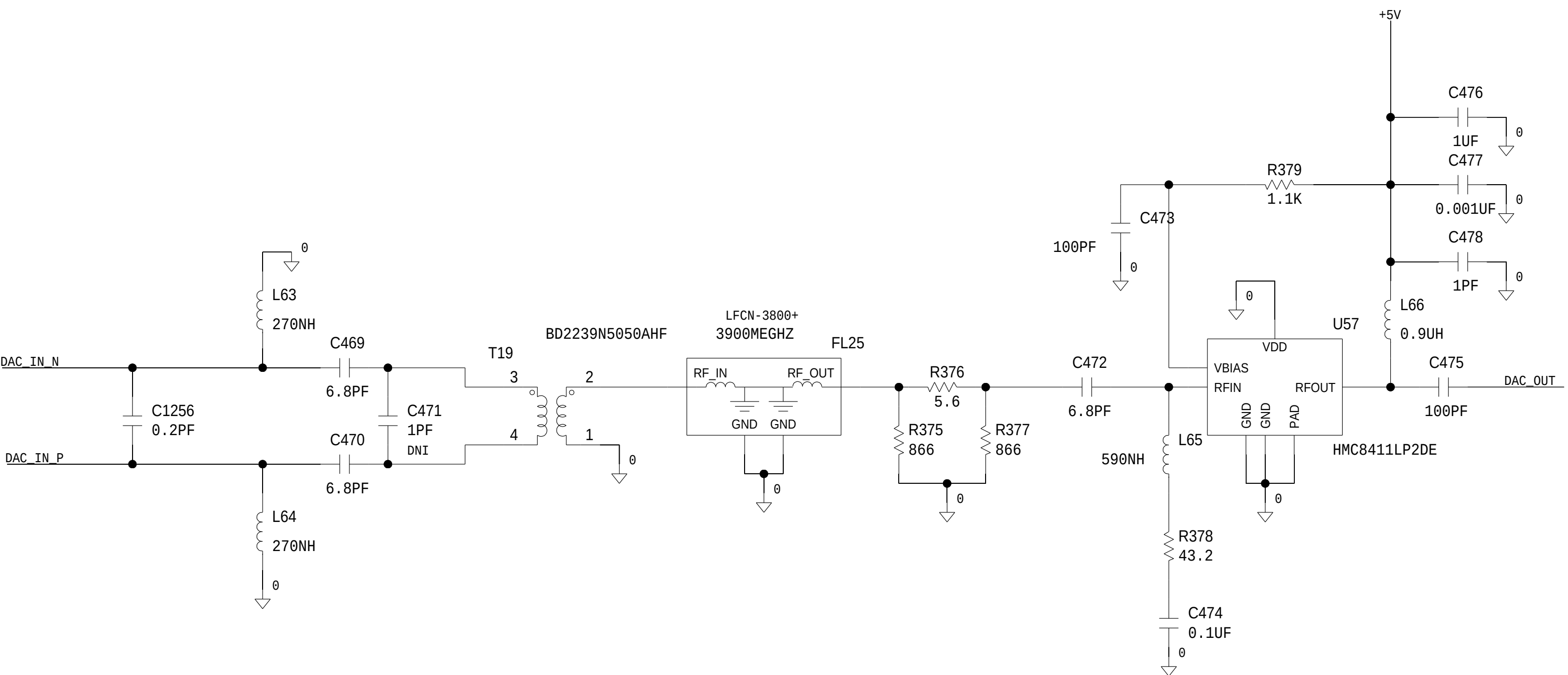


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



DAC FRONT END-PS

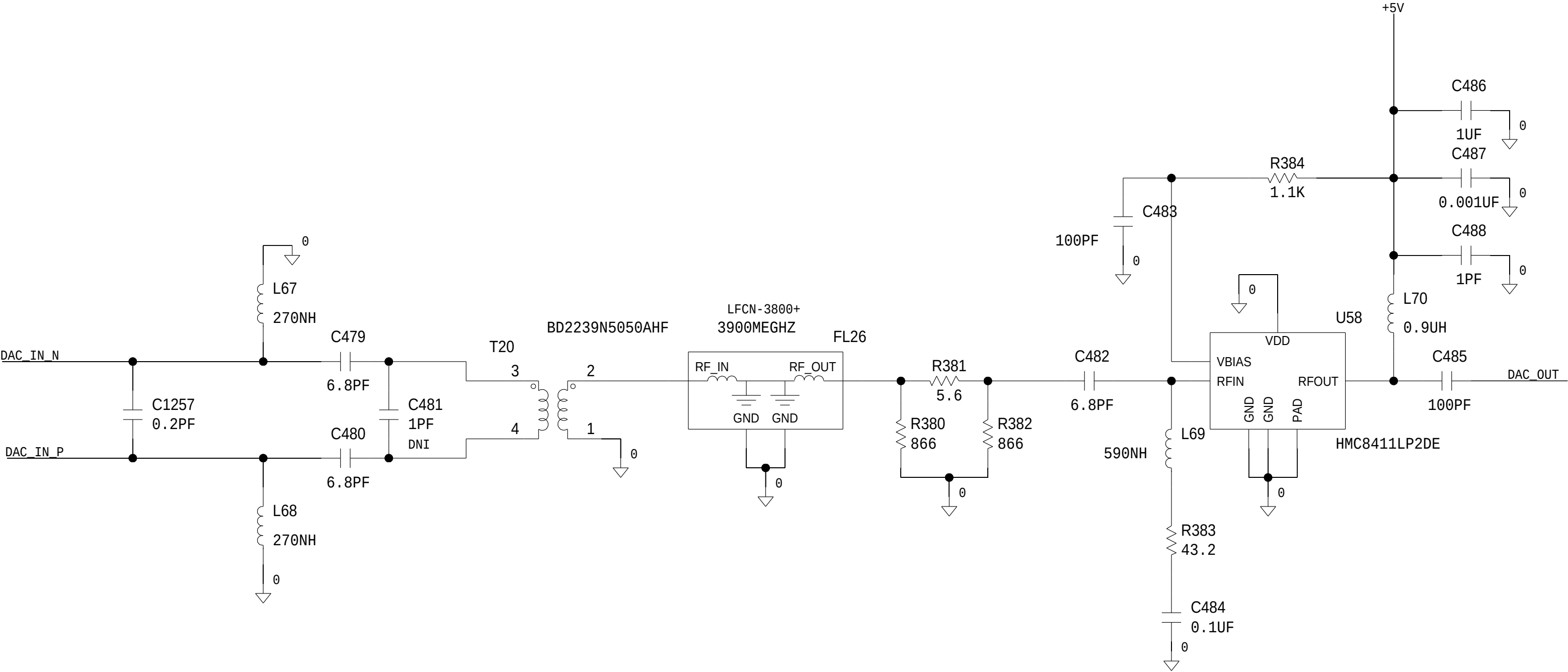
ANTICIPATE ~6DBM OUTPUT POWER @ 3.5GH.



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

DAC FRONT END-PS

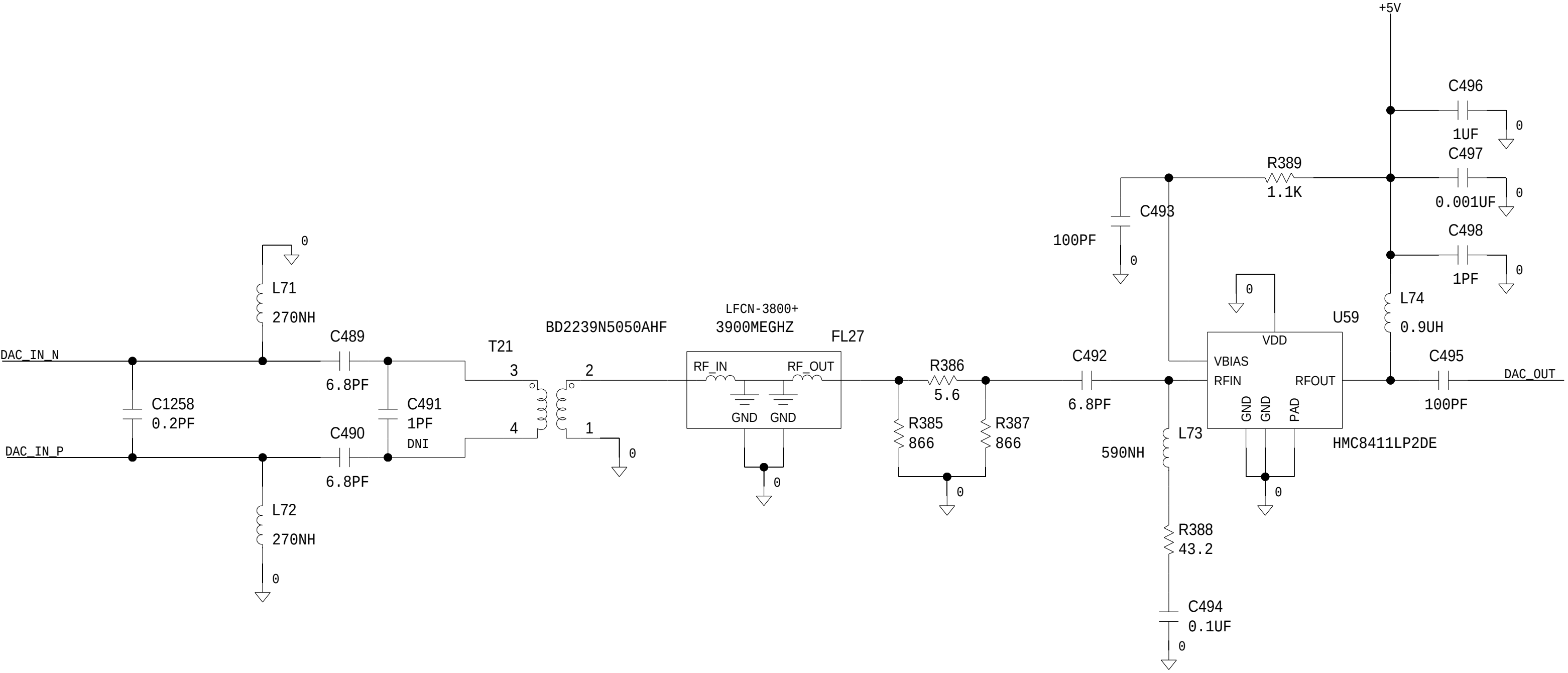
ANTICIPATE ~6DBM OUTPUT POWER @ 3.5GHZ



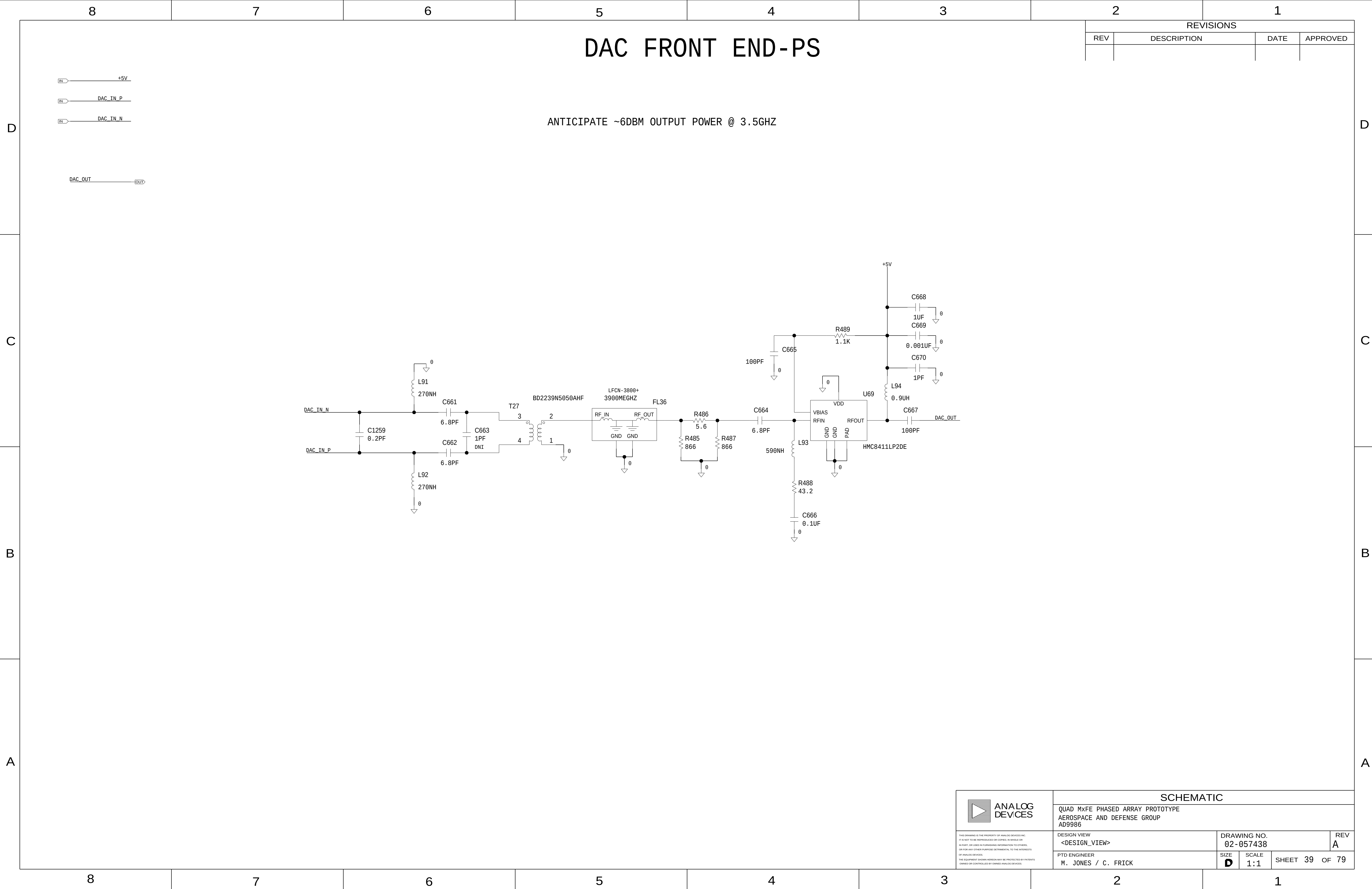
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

DAC FRONT END-PS

ANTICIPATE ~6DBM OUTPUT POWER @ 3.5GH.



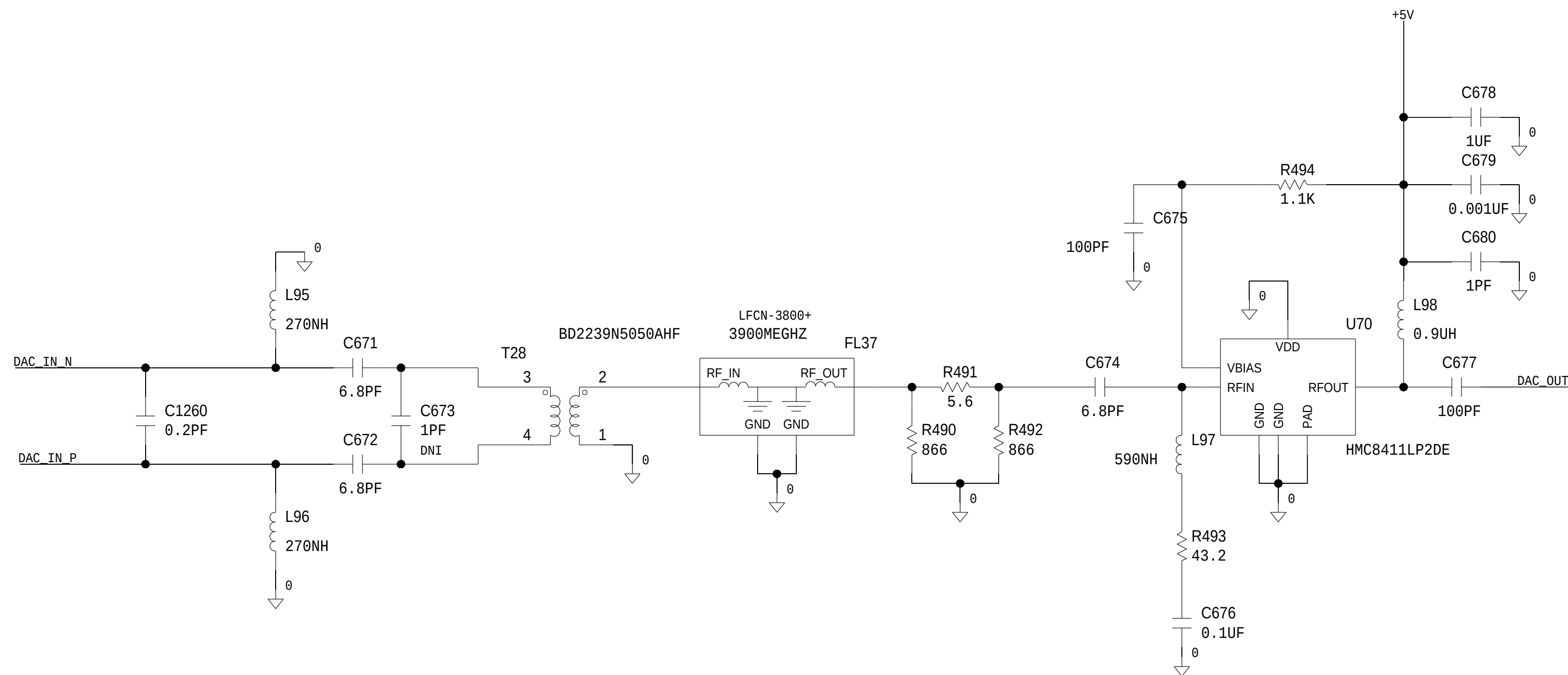
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

The block diagram shows the DAC0808 with the following pins:

- IN
- IN
- IN
- IN
- DAC_IN_P
- DAC_IN_N
- DAC_OUT
- OUT



THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES, INC.
IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR
IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS,
OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS
OF ANALOG DEVICES.
THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENT,
OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9986

DESIGN VIEW
<DESIGN_VIEW>

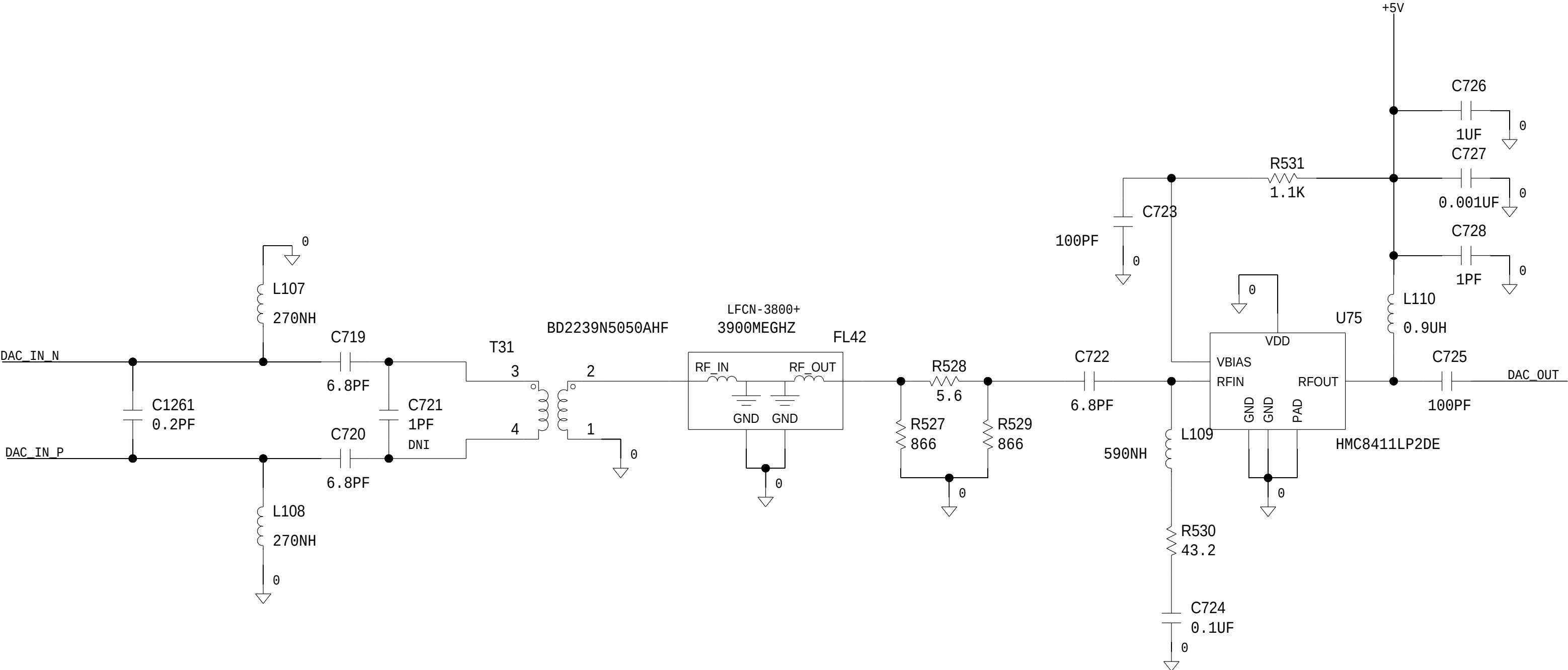
PTD ENGINEER
M. JONES / C. FRICK

DRAWING NO.
02-057438

SIZE D	SCALE 1:1	SHEET 40 OF 79
------------------	--------------	----------------

DAC FRONT END-PS

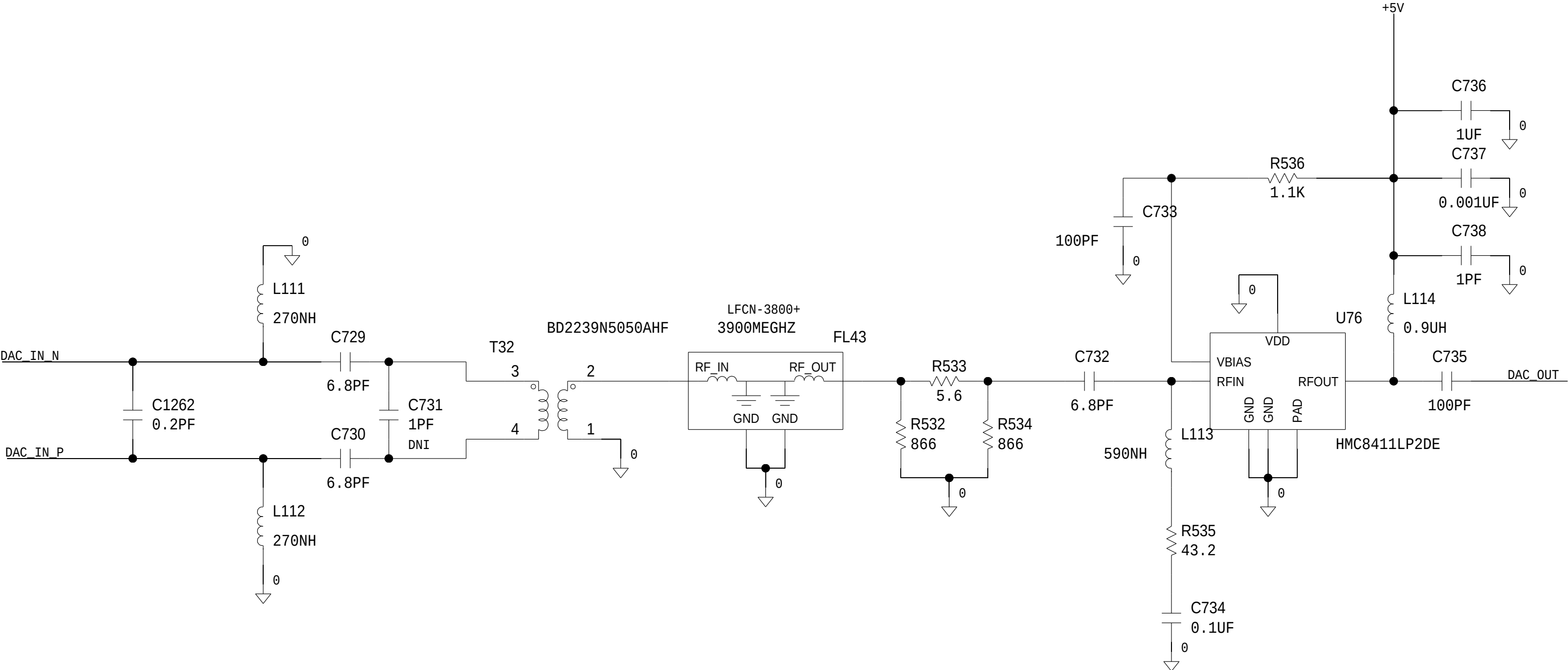
ANTICIPATE ~6DBM OUTPUT POWER @ 3.5GHZ



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

DAC FRONT END-PS

ANTICIPATE ~6DBM OUTPUT POWER @ 3.5GHZ

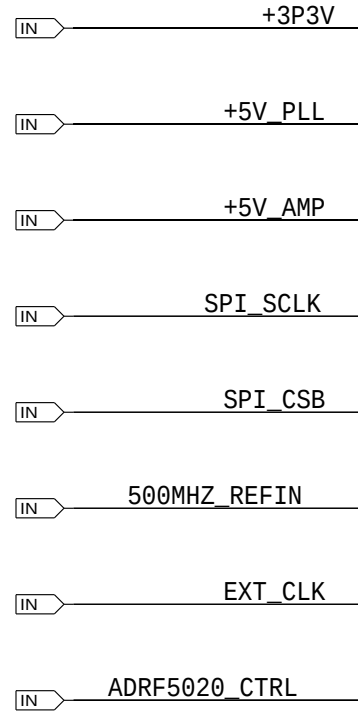


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

CLOCK GENERATION

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

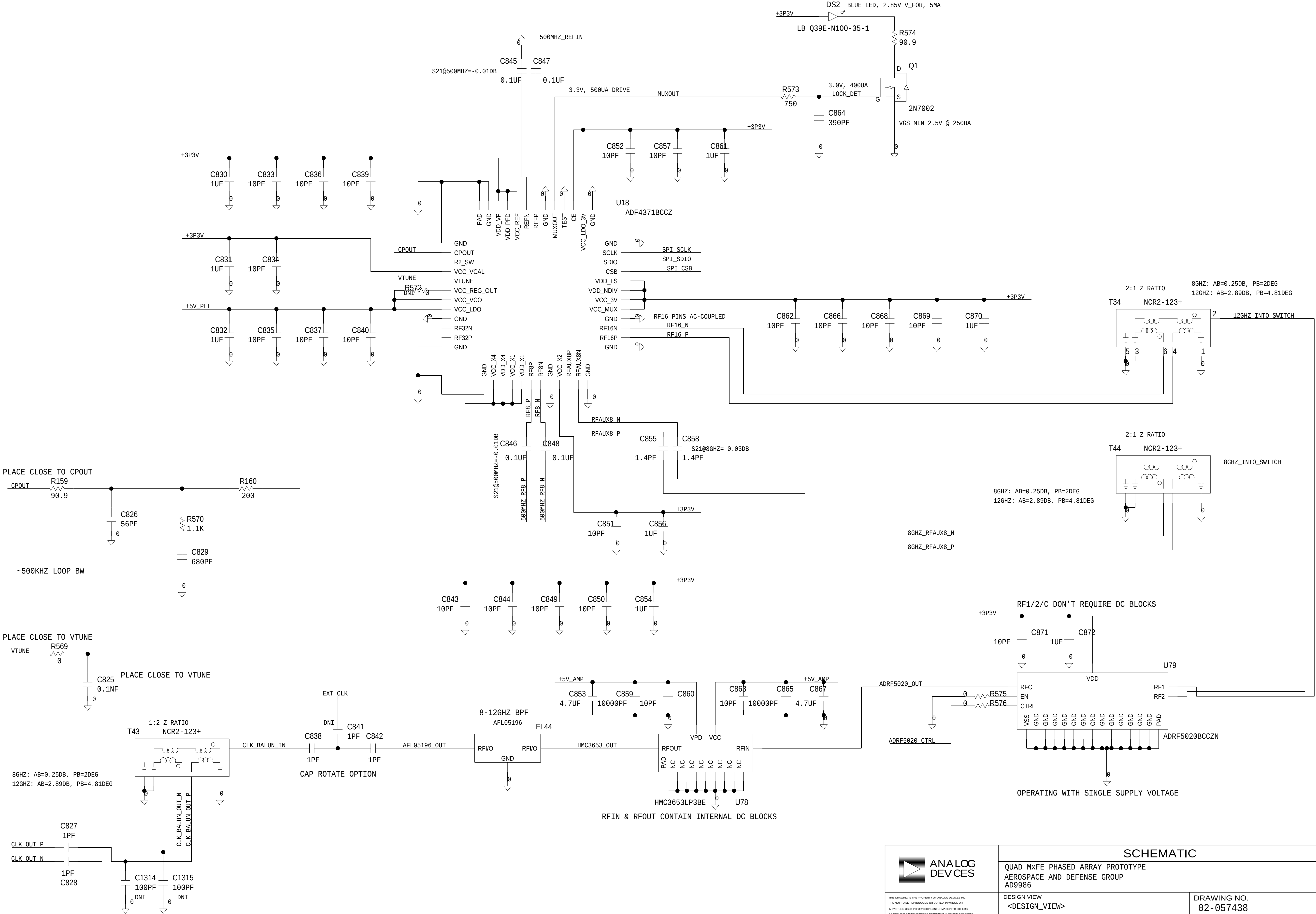
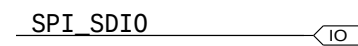
INPUTS

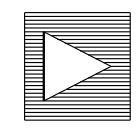


OUTPUTS



I/O





**ANALOG
DEVICES**

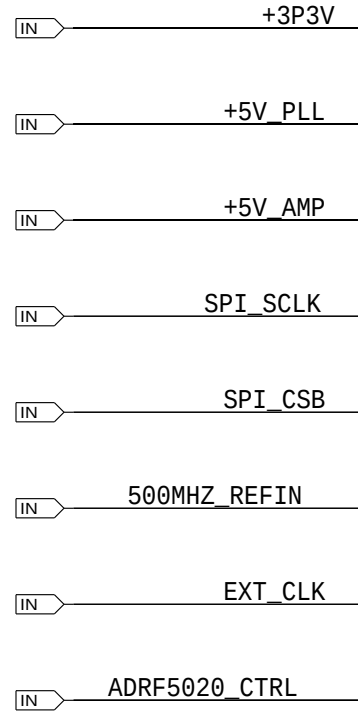
THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC.
IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR
IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS,
OR FOR ANY OTHER PURPOSES DETERMINANTAL TO THE INTERESTS
OF ANALOG DEVICES.
THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS
OWNED OR CONTROLLED BY ANALOG DEVICES.

SCHEMATIC				
QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9986				
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02-057438		REV A	
PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 43 OF 79	

CLOCK GENERATION

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

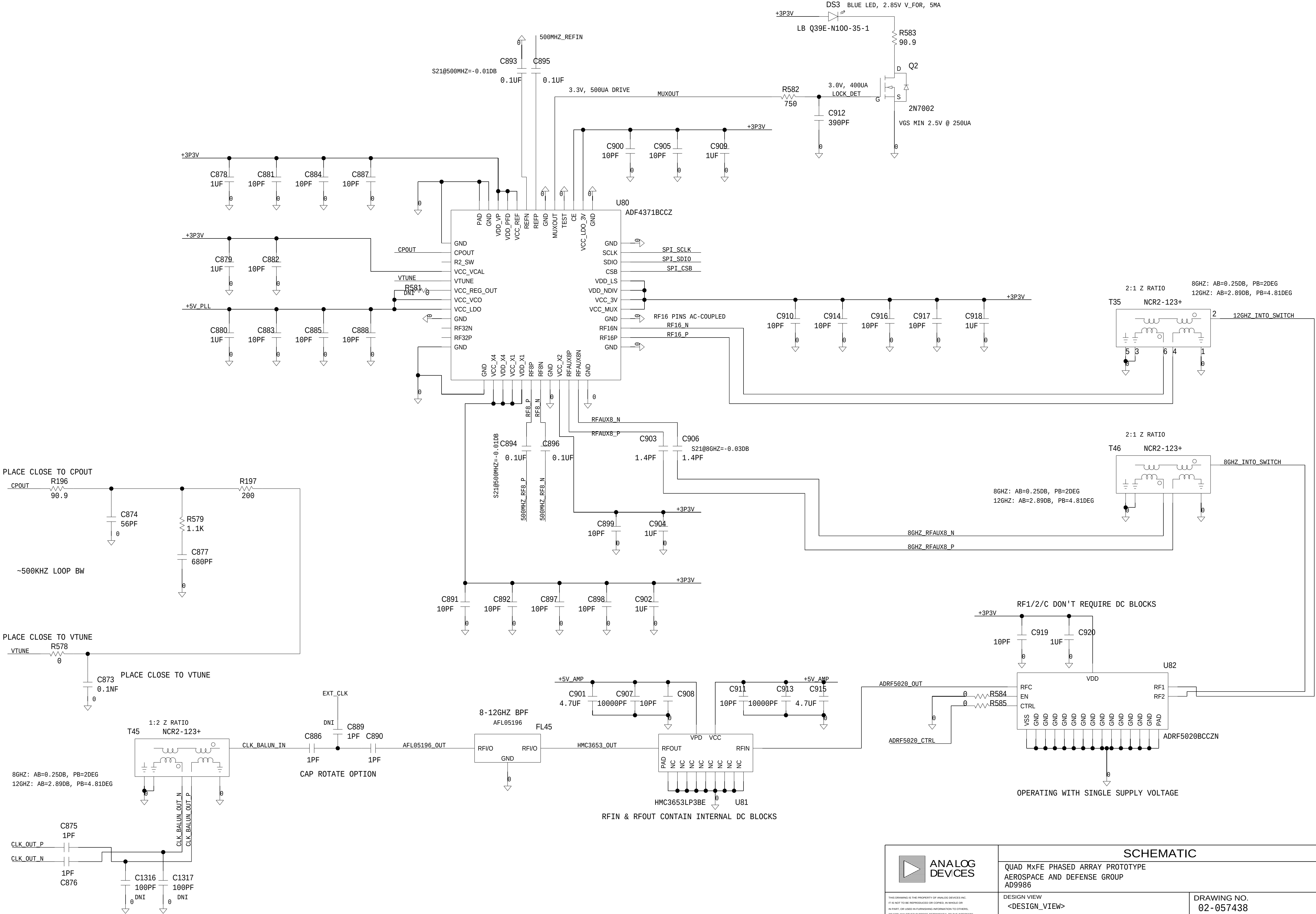
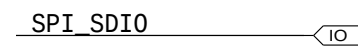
INPUTS



OUTPUTS



I/O

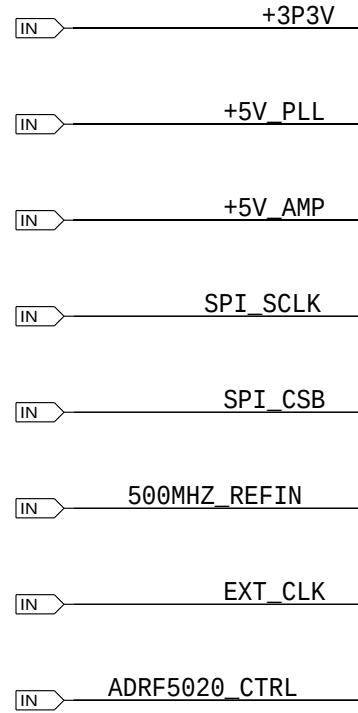


ANALOG DEVICES	SCHEMATIC			
	QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9986			
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02-057438		REV A
	PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 44 OF 79

CLOCK GENERATION

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

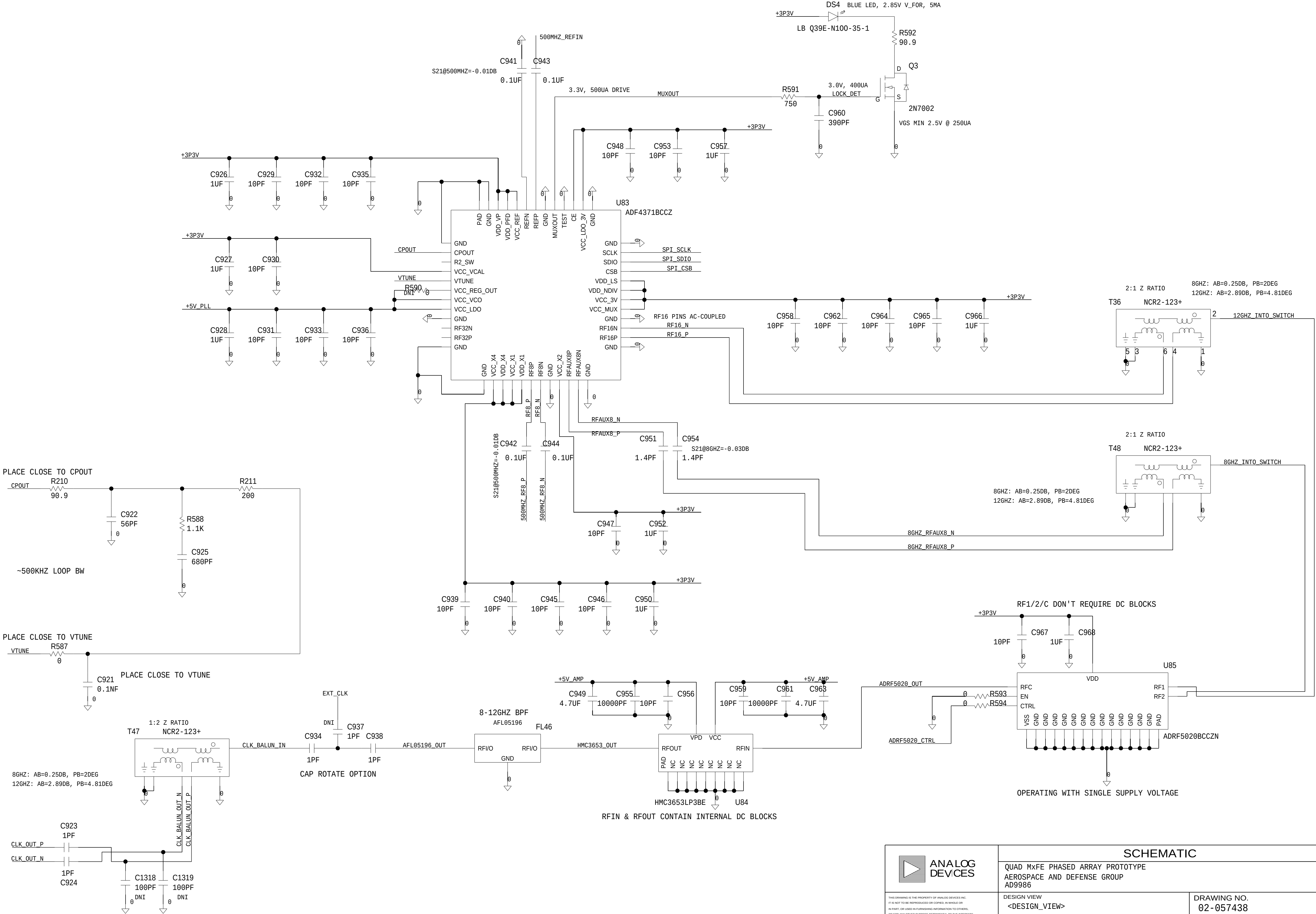
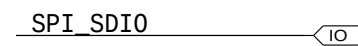
INPUTS



OUTPUTS



I/O



SCHEMATIC

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9986

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
M. JONES / C. FRICK

DRAWING NO.
02-057438

SIZE
D

SCALE
1:1

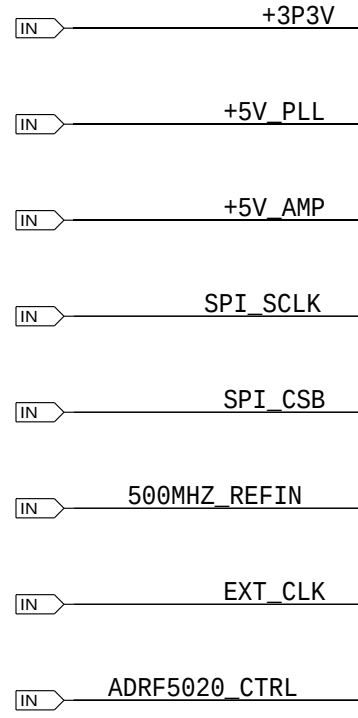
SHEET 45 OF 79

REV
A

CLOCK GENERATION

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

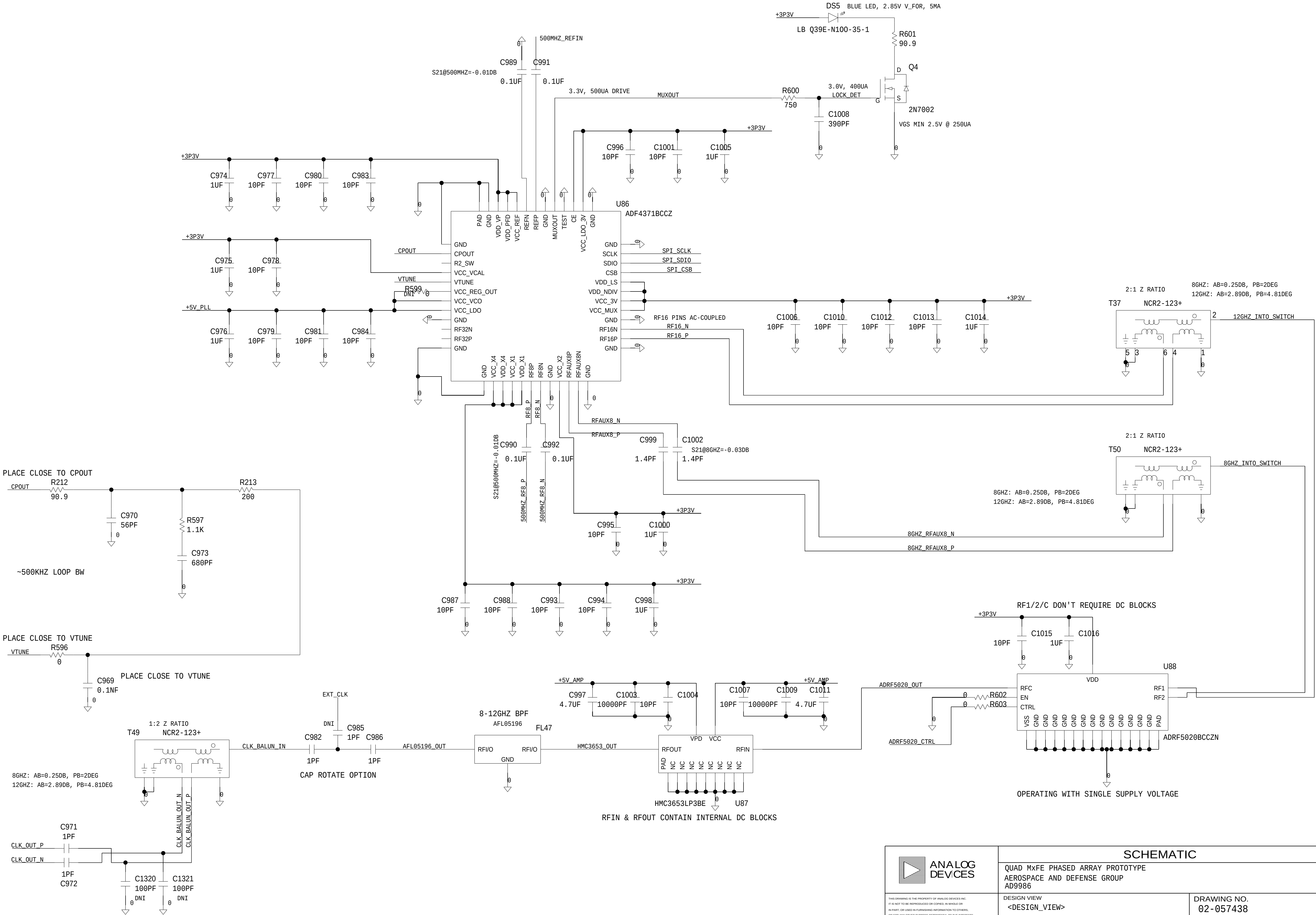
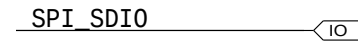
INPUTS



OUTPUTS



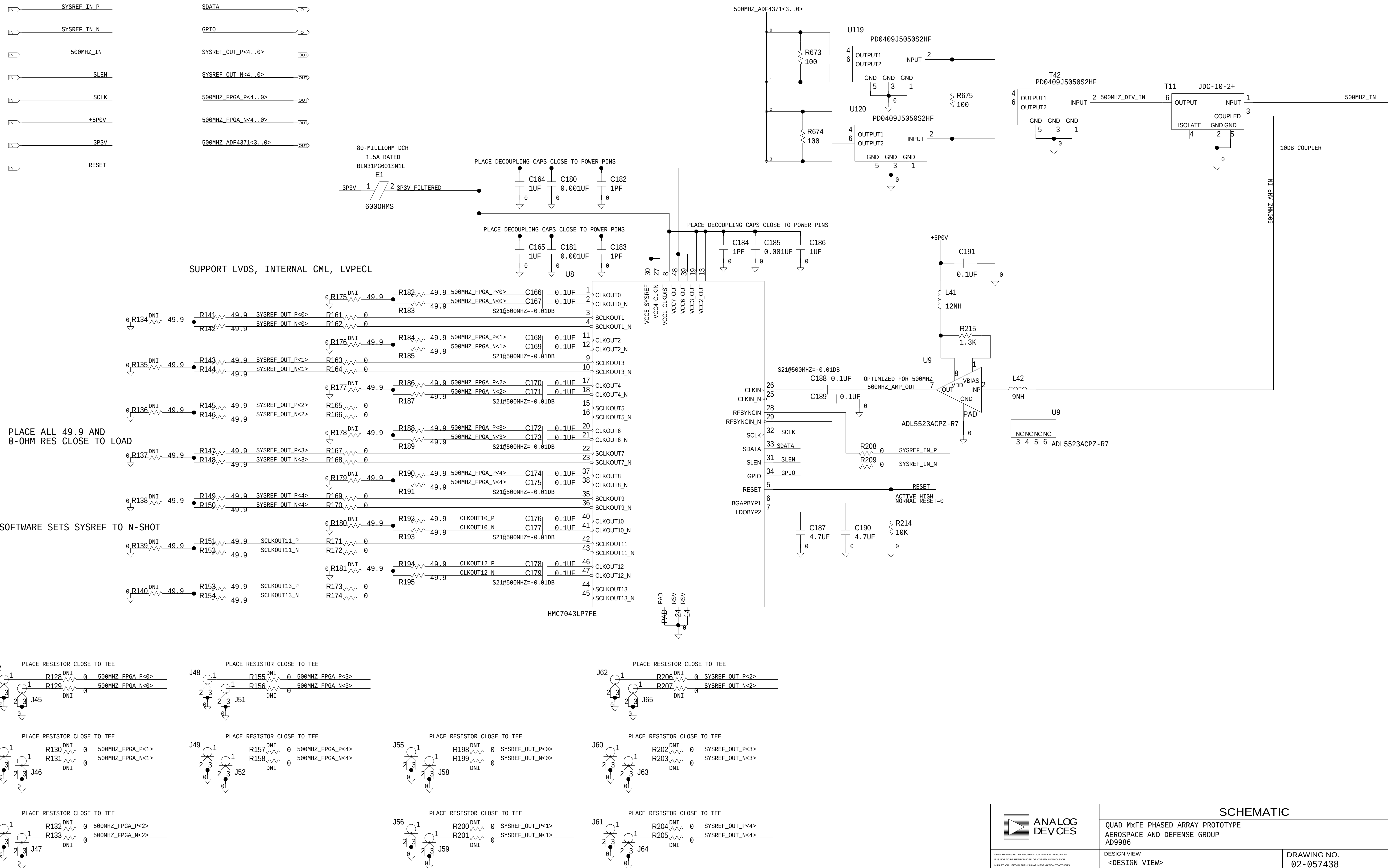
I/O



ANALOG DEVICES	SCHEMATIC			
	QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9986			
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02-057438		REV A
	PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 46 OF 79

CLOCK FRONT END

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANALOG
DEVICES

THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC.
IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR
IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS,
OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS
OF ANALOG DEVICES.
THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENT
OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.

SCHEMATIC

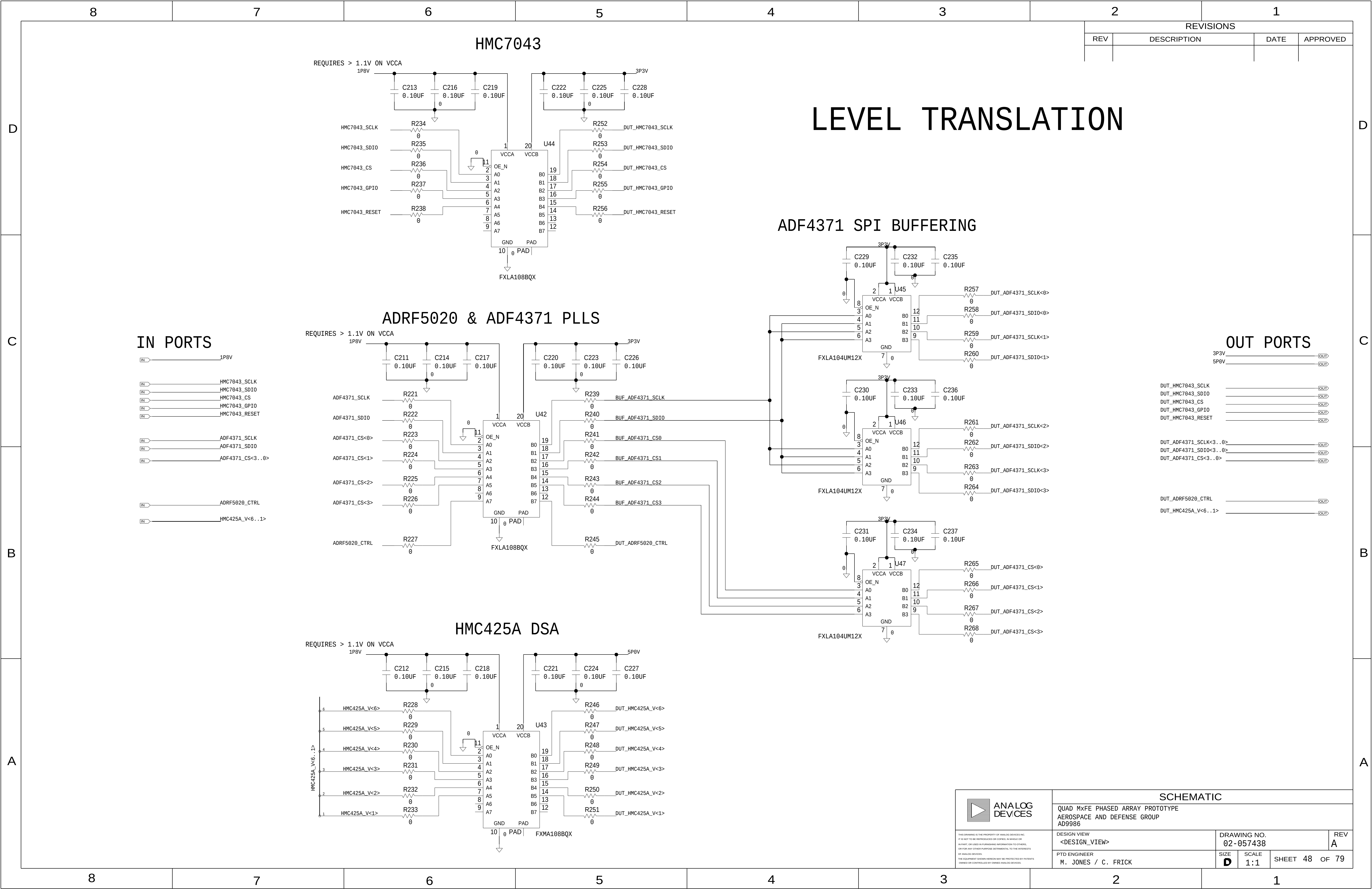
QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9986

DESIGN VIEW	<DESIGN_VIEW>
PTD ENGINEER	M. JONES / C.

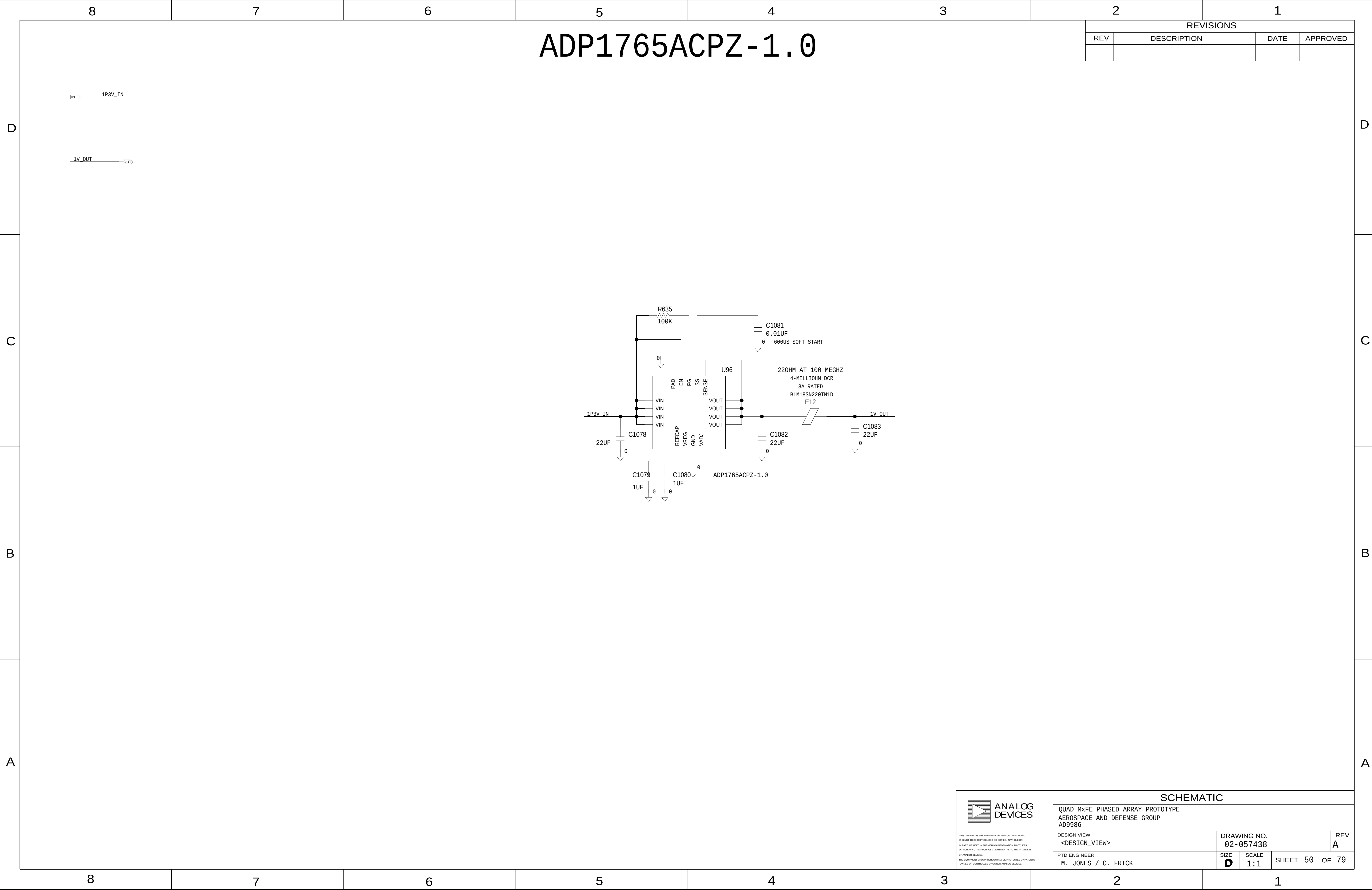
DRAWING NO. 02-057438

SIZE	SCALE	
D	1:1	

REV
A



DA



87654321

ADP1765ACPZ-1.0

REVDESCRIPTIONDATEAPPROVED

1P3V_IN

1V_OUT

QUAD MxFe PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9986

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
M. JONES / C. FRICK

DRAWING NO.
02-057438

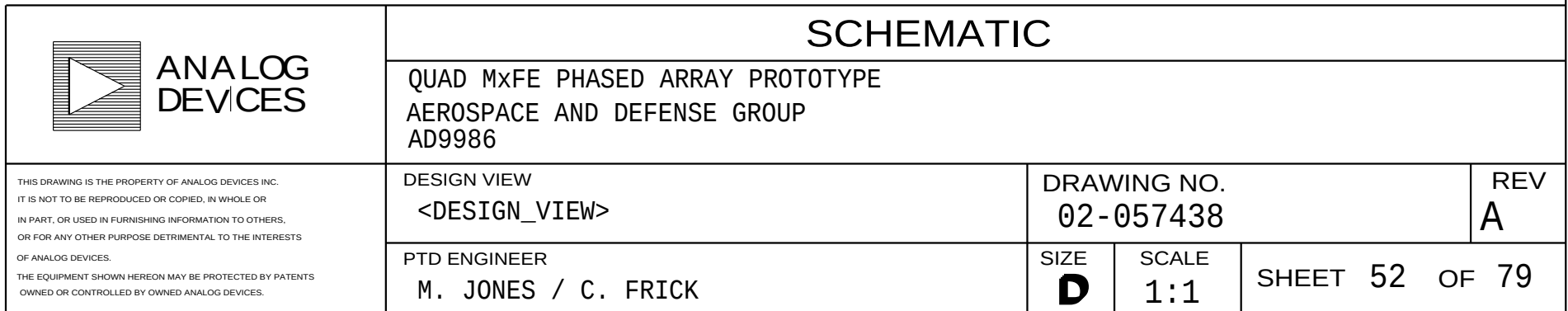
SIZE
D

SCALE
1:1

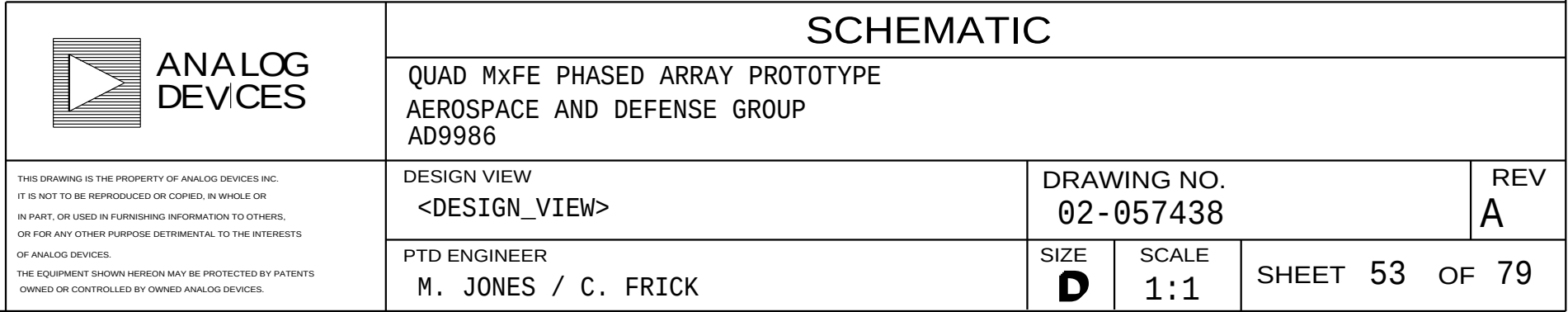
SHEET 51 OF 79

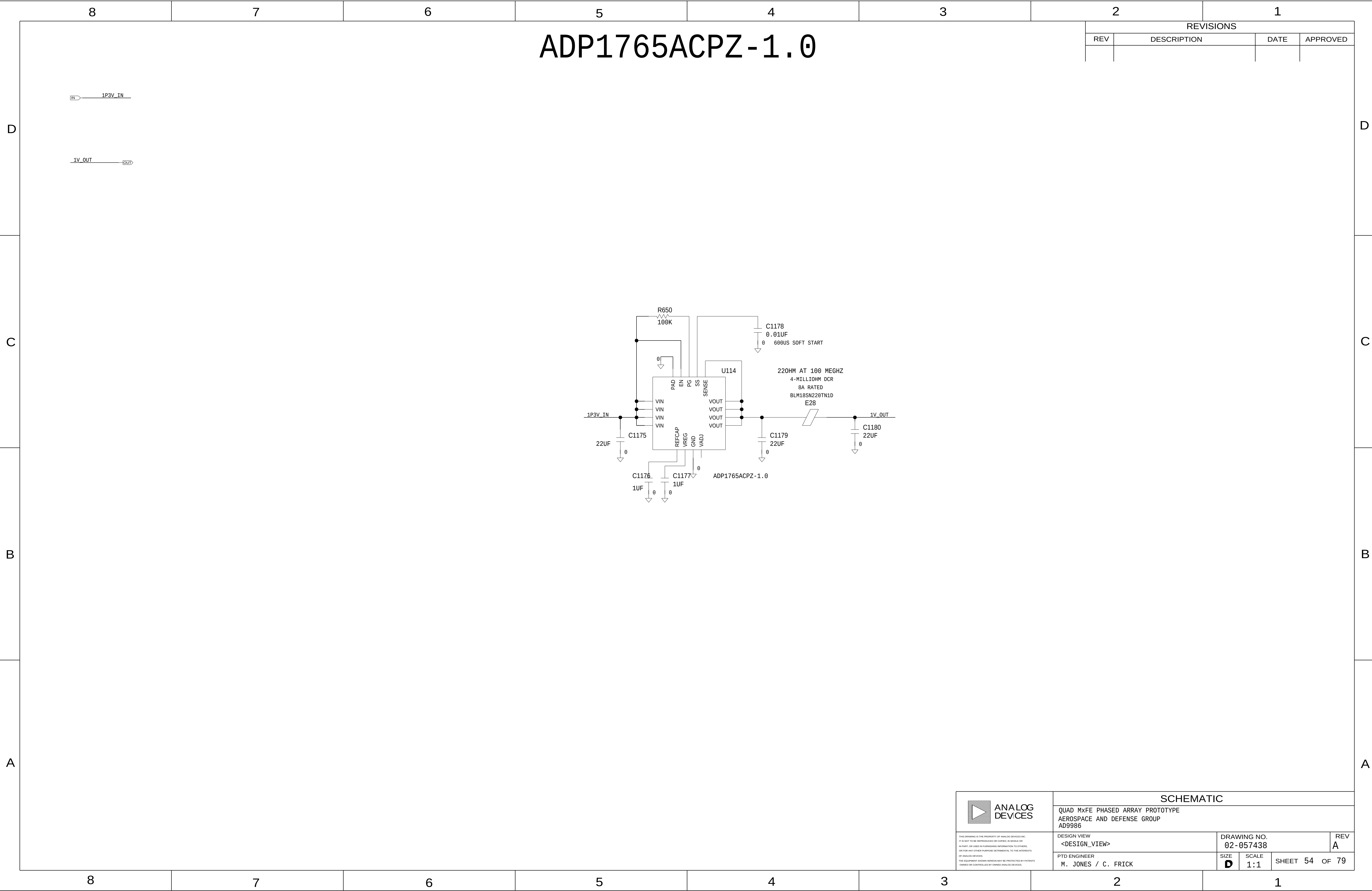
REV
A

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



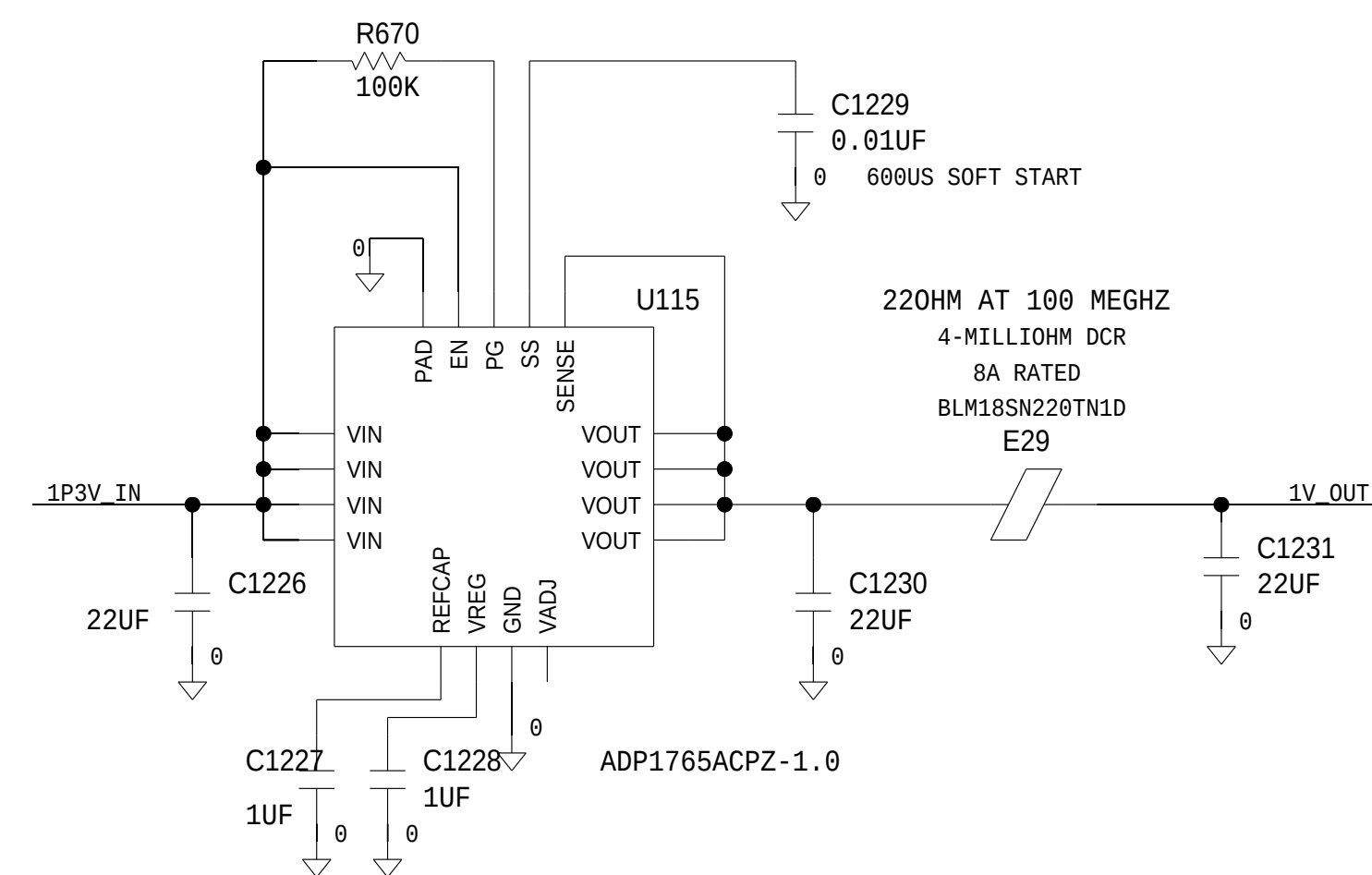
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED





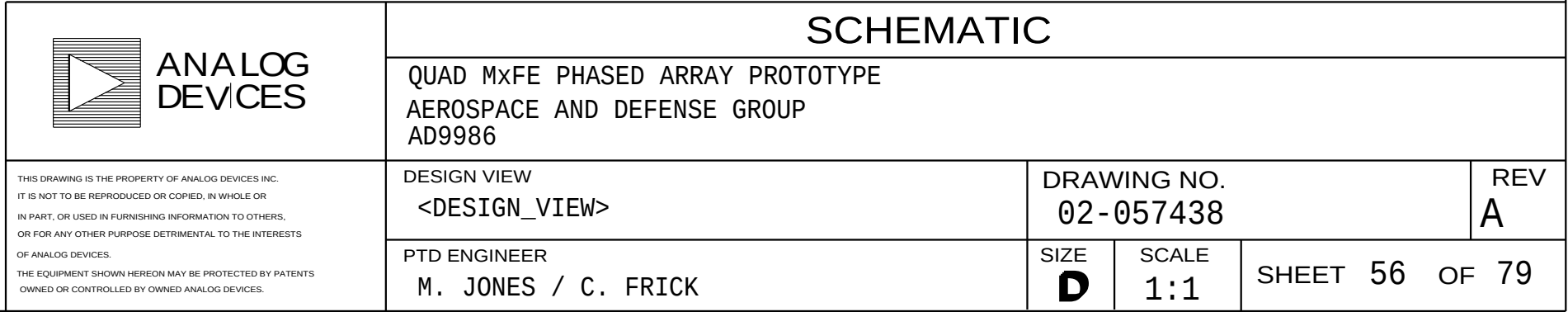
ADP1765ACPZ-1.0

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



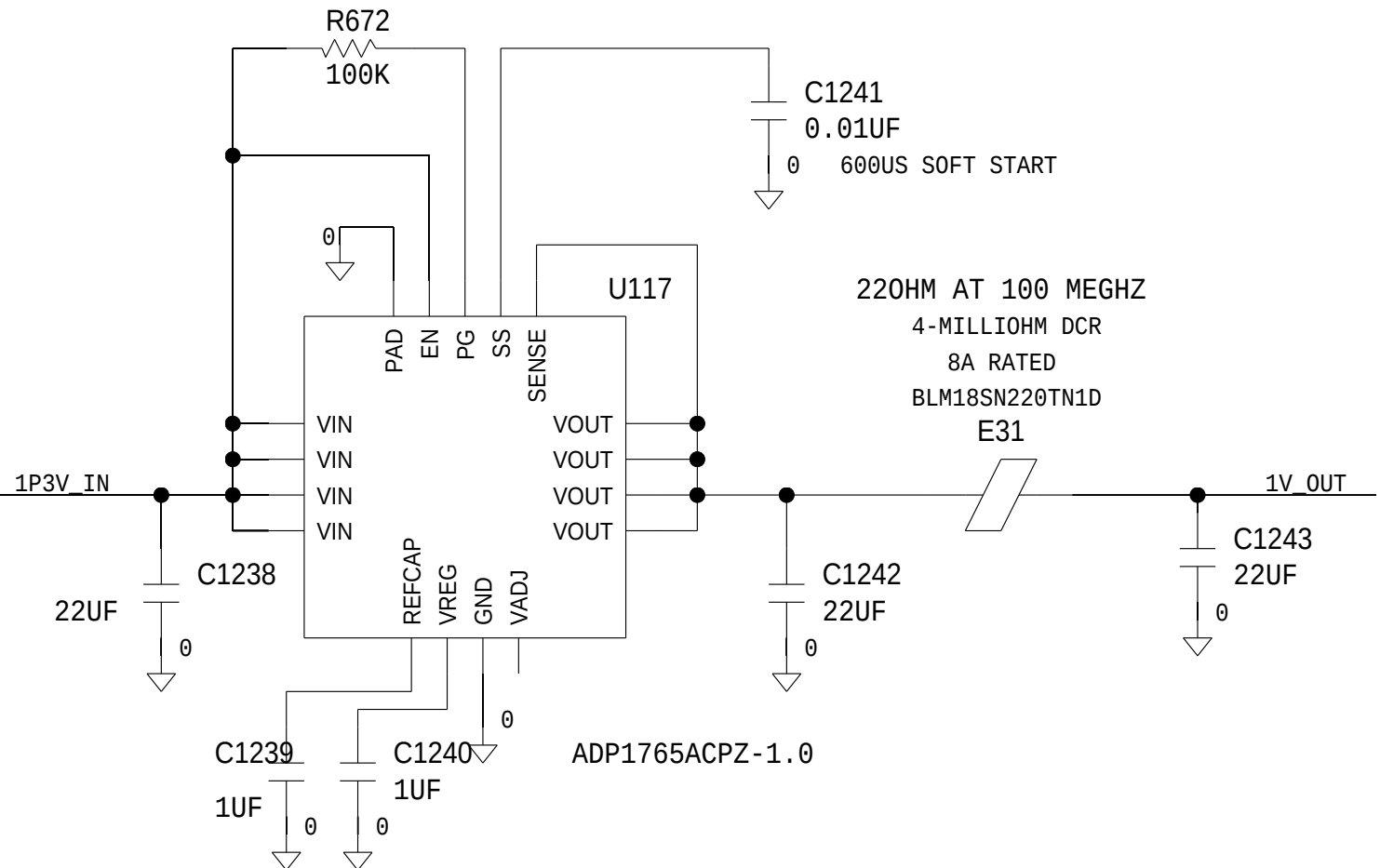
 ANALOG DEVICES	SCHEMATIC				
	QUAD MxFe PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9986				
THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSES DETRIMENTAL, TO THE INTERESTS OF ANALOG DEVICES. ANY EQUIPMENT OR SYSTEMS MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.	DESIGN VIEW <DESIGN_VIEW>		DRAWING NO. 02-057438		REV A
	PTD ENGINEER M. JONES / C. FRICK		SIZE D	SCALE 1:1	SHEET 55 OF 79

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

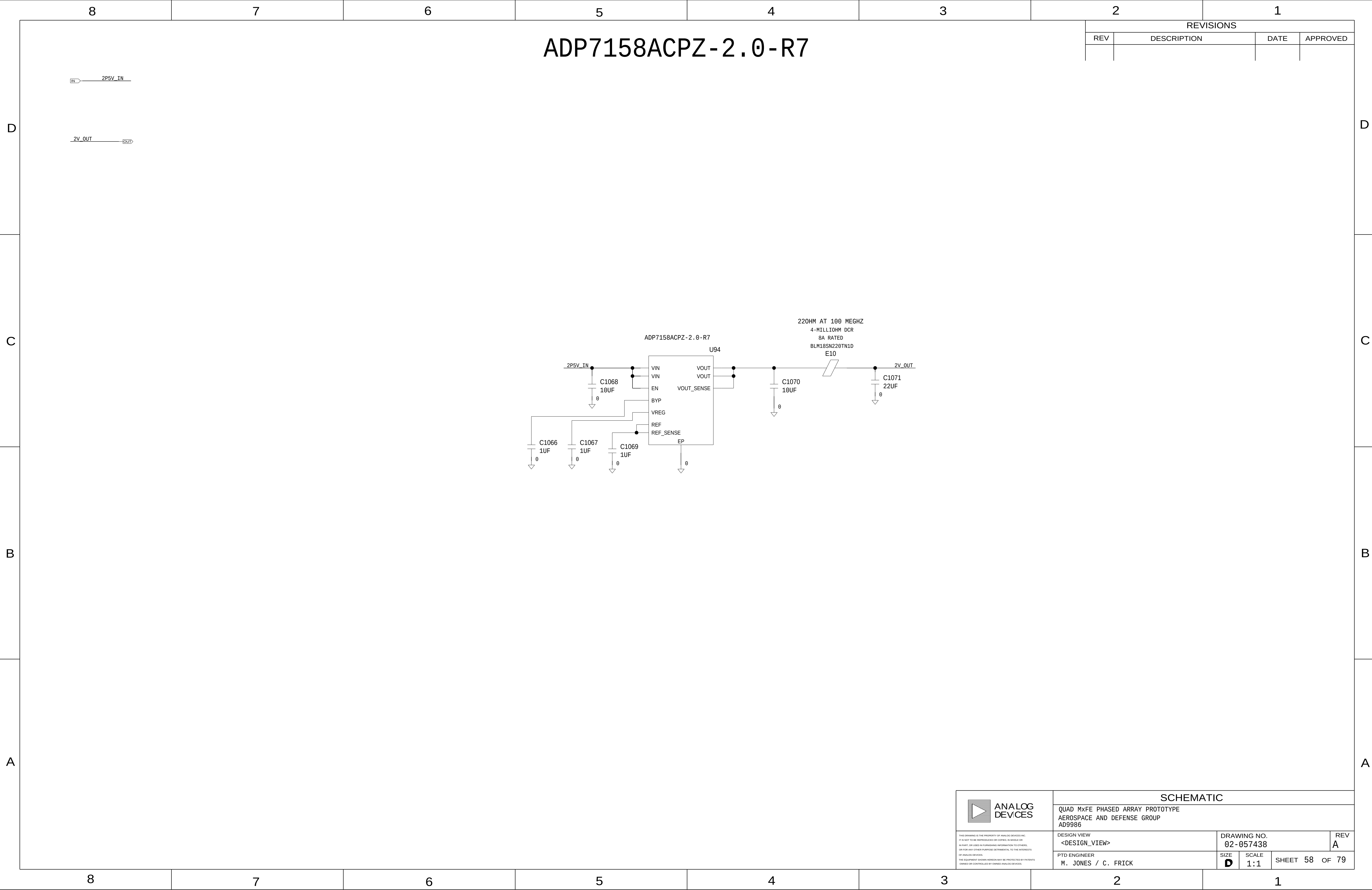


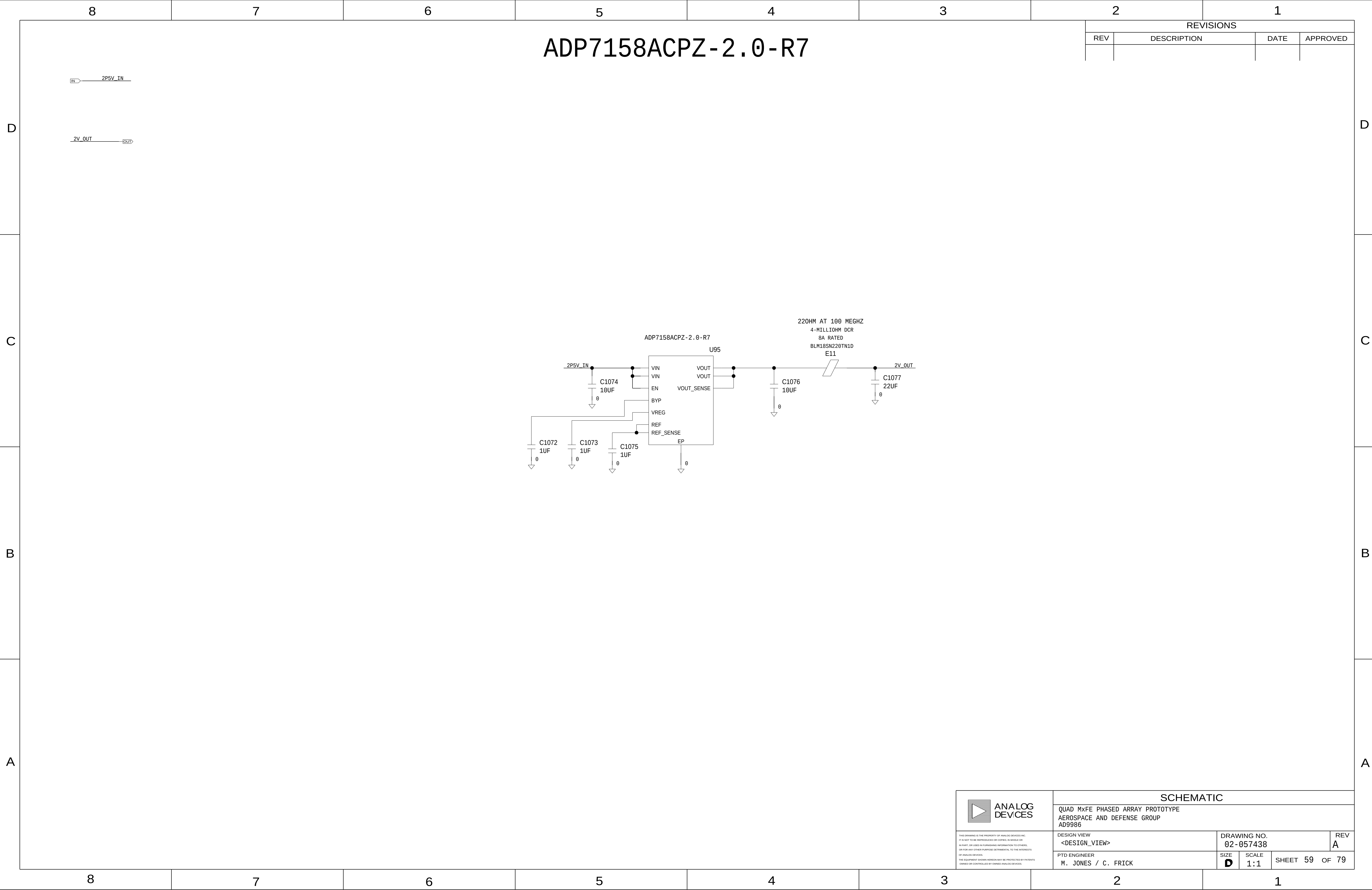
ADP1765ACPZ-1.0

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



	SCHEMATIC			
	QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9986			
THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES, INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE WITHOUT PERMISSION OF THE MANAGERS OF ANALOG DEVICES. THE EQUIPMENT DESIGN INFORMATION MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG DEVICES.	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02-057438	REV A	
	PTD ENGINEER M. JONES / C. FRICK	SCALE 1:1	SHEET 57 OF 79	





87654321

ADP7158ACPZ-2.0-R7

2P5V_IN

2V_OUT

2P5V_IN

2V_OUT

U118

C1246

C1248

C1249

C1244

C1245

C1247

E32

ADP7158ACPZ-2.0-R7

220HM AT 100 MEGHZ

4-MILLIOHM DCR

8A RATED

BLM18SN220TN1D

VIN

VOUT

EN

VOUT_SENSE

BYP

VREG

REF

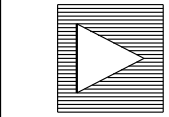
REF_SENSE

EP

87654321

87654321

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

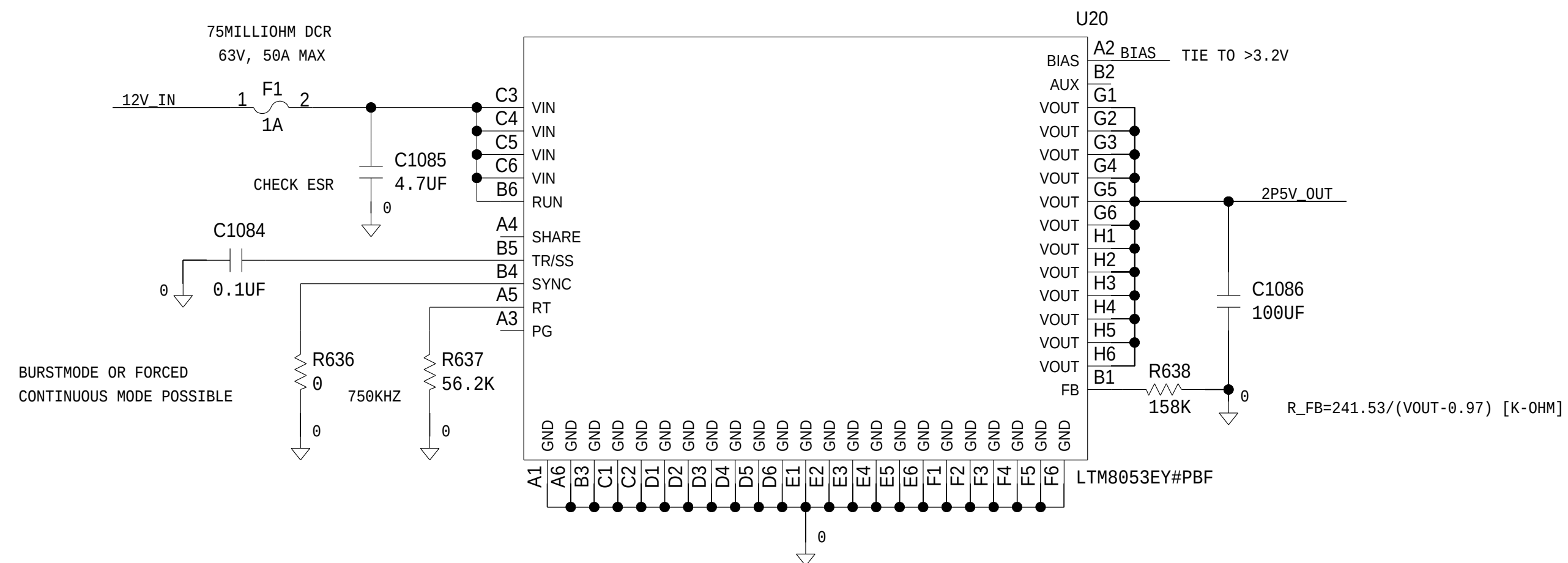


ANALOG
DEVICES

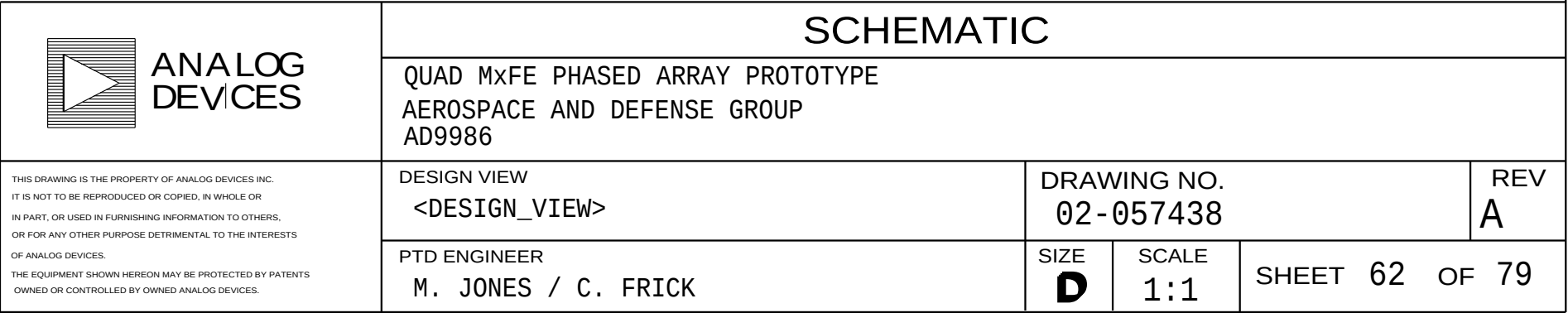
THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC.
IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR
IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS,
OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS
OF ANALOG DEVICES.
THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS
OWNED OR CONTROLLED BY ANALOG DEVICES.

SCHEMATIC			
QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9986			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02-057438	REV A	
PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 60 OF 79

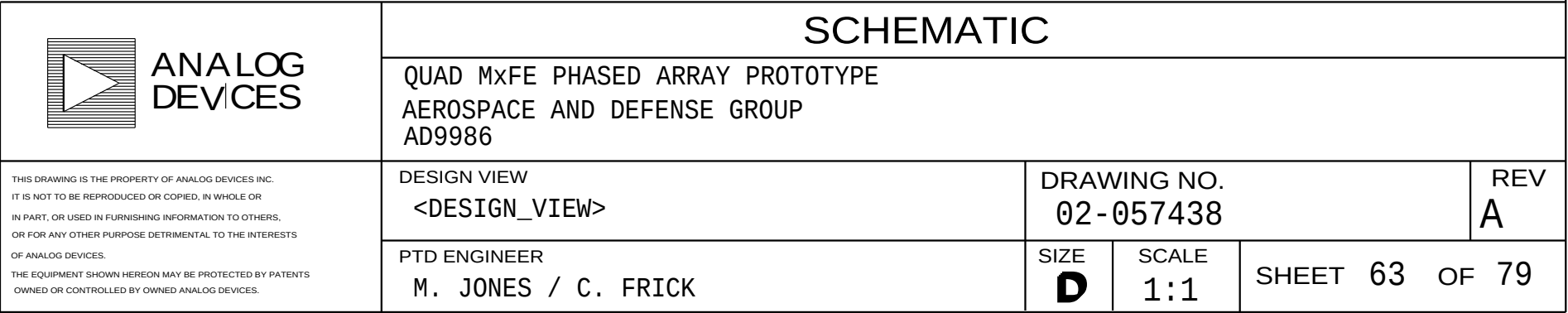
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



87654321

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

ADM7172ACPZ-5.0-R7

6V_IN

5V_OUT

ANALOG
DEVICES

THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC.
IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR
IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS,
OR FOR ANY OTHER PURPOSES DETRIMENTAL TO THE INTERESTS
OF ANALOG DEVICES.
THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS
OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.

SCHEMATIC

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9986

DESIGN VIEW
<DESIGN_VIEW>

DRAWING NO.
02-057438

REV
A

PTD ENGINEER
M. JONES / C. FRICK

SIZE
D

SCALE
1:1

SHEET 64 OF 79

87654321

D

C

B

A

D

C

B

A

87654321

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

ADM7172ACPZ-5.0-R7

6V_IN

5V_OUT

6V_IN

C1094

4.7UF

CHECK ESR

C1095

3000PF

-2.2MS STARTUP

ADM7172ACPZ-5.0

U99

VIN1

VIN2

EN

SS

SENSE

GND

EP

VOUT1

VOUT2

C1096

4.7UF

220HM AT 100 MEGHZ

4-MILLIOHM DCR

8A RATED

BLM18SN220TN1D

E14

C1097

22UF

5V_OUT

87654321

87654321

ANALOG
DEVICES

THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC.
IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR
IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS,
OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS
OF ANALOG DEVICES.
THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS
OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.

SCHEMATIC

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9986

DESIGN VIEW
<DESIGN_VIEW>

DRAWING NO.
02-057438

REV
A

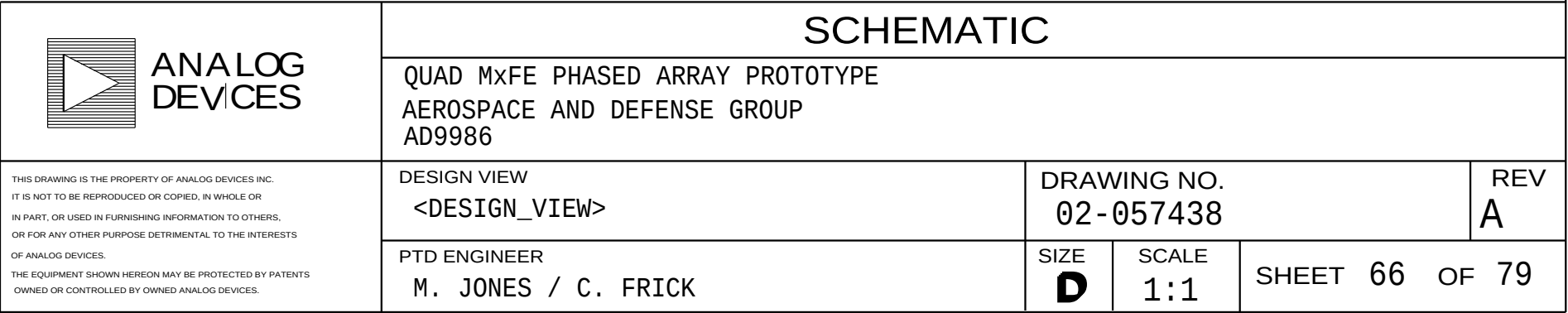
PTD ENGINEER
M. JONES / C. FRICK

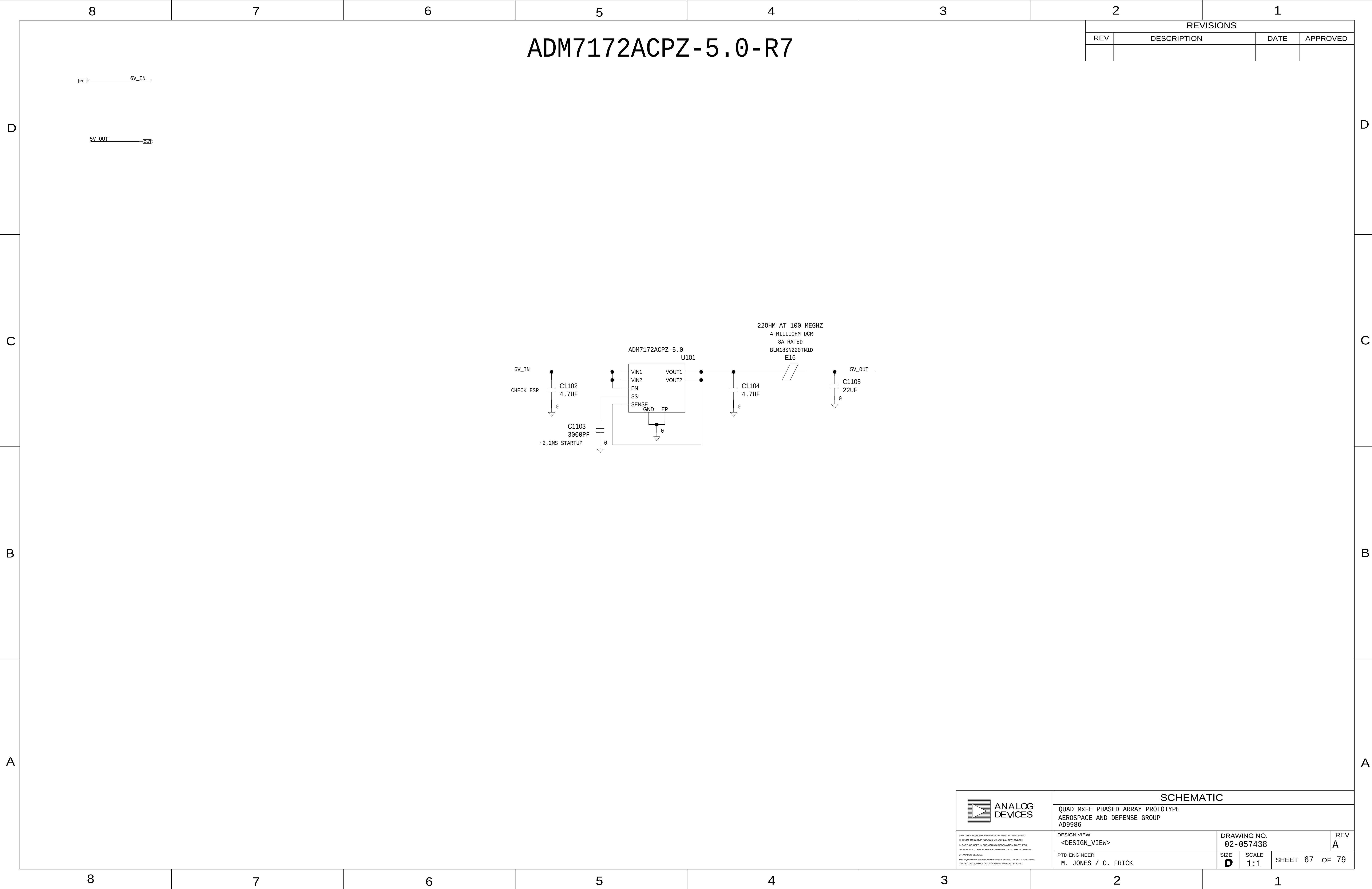
SIZE
D

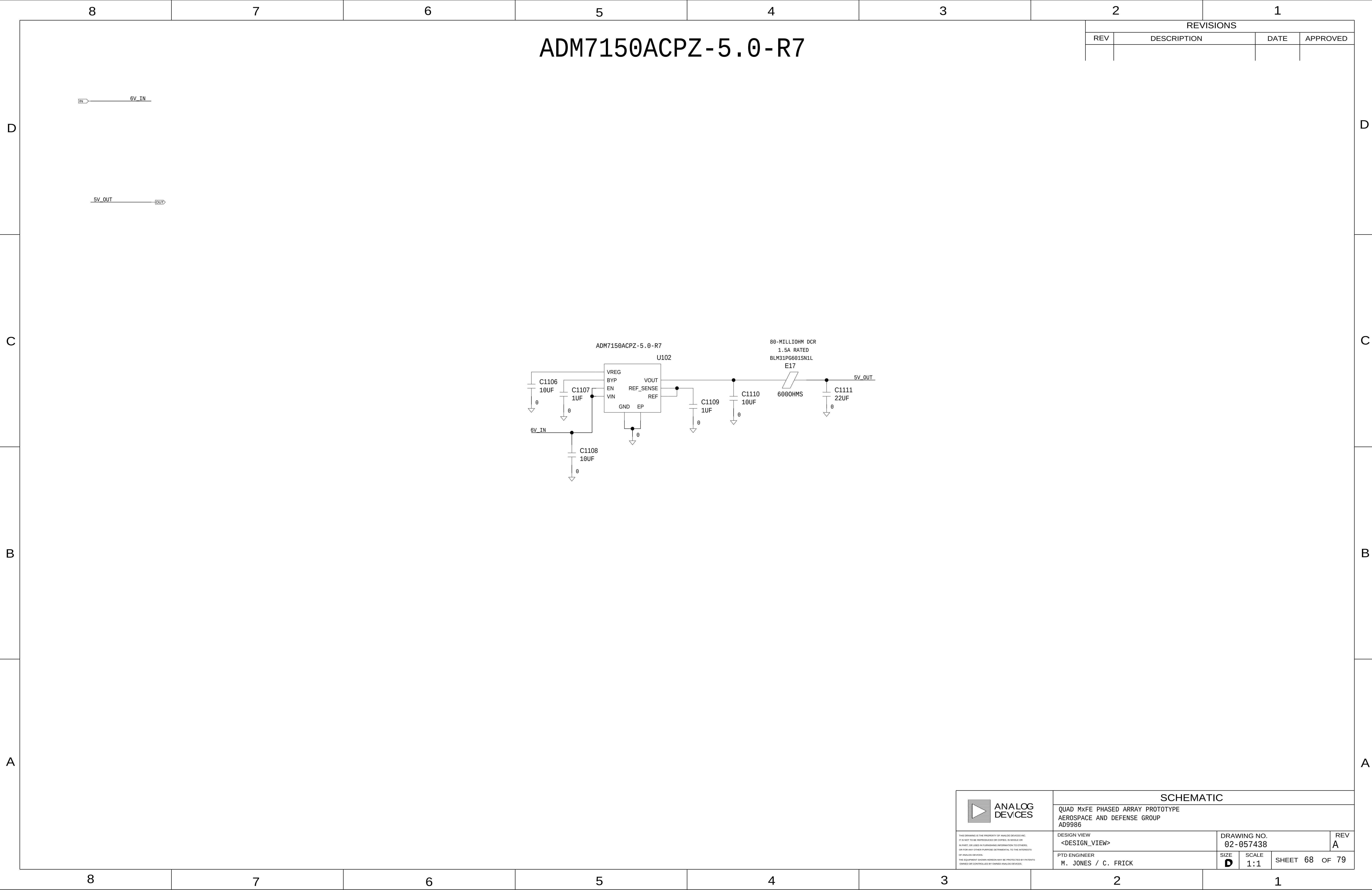
SCALE
1:1

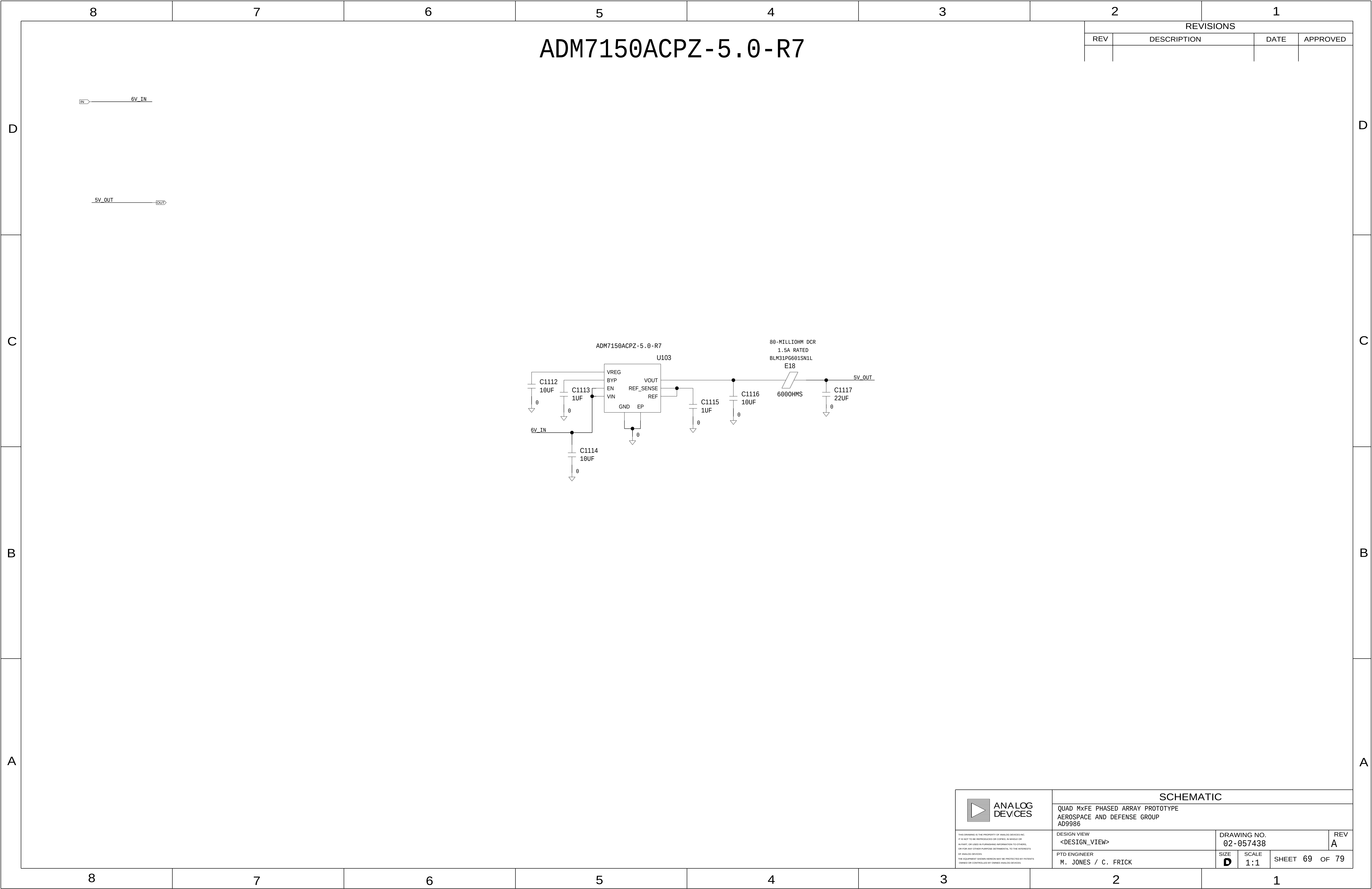
SHEET 65 OF 79

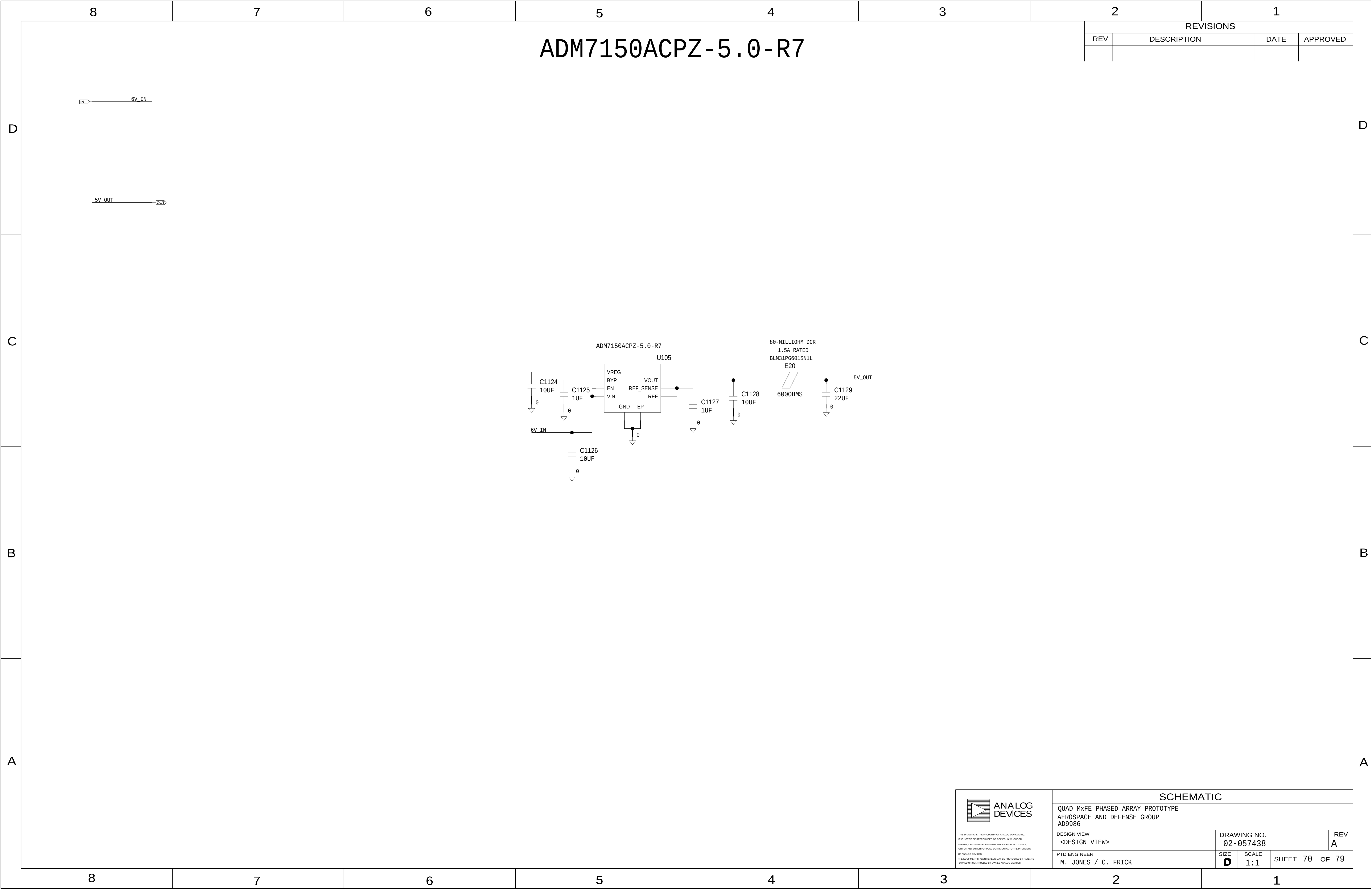
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

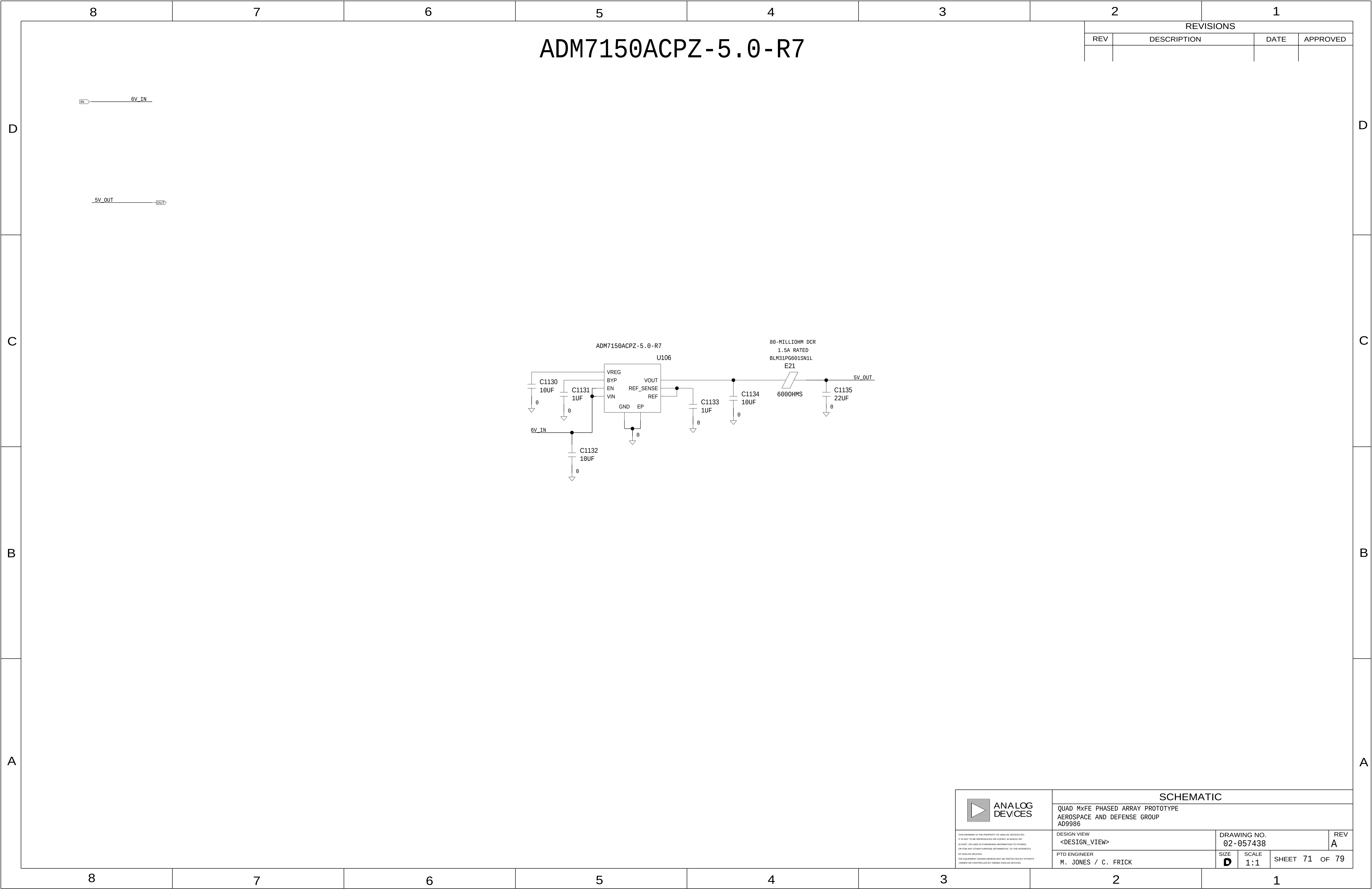


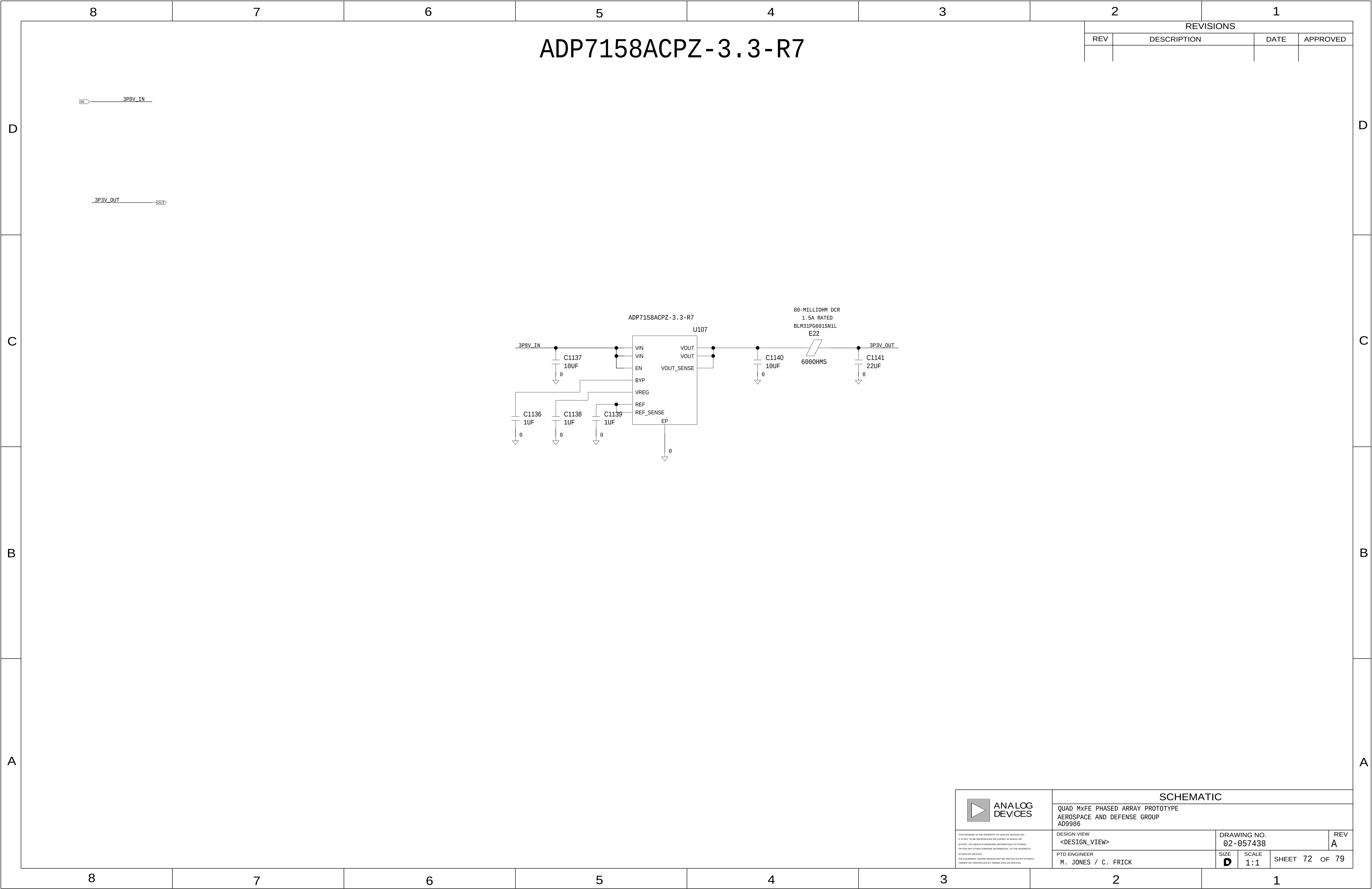




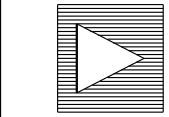








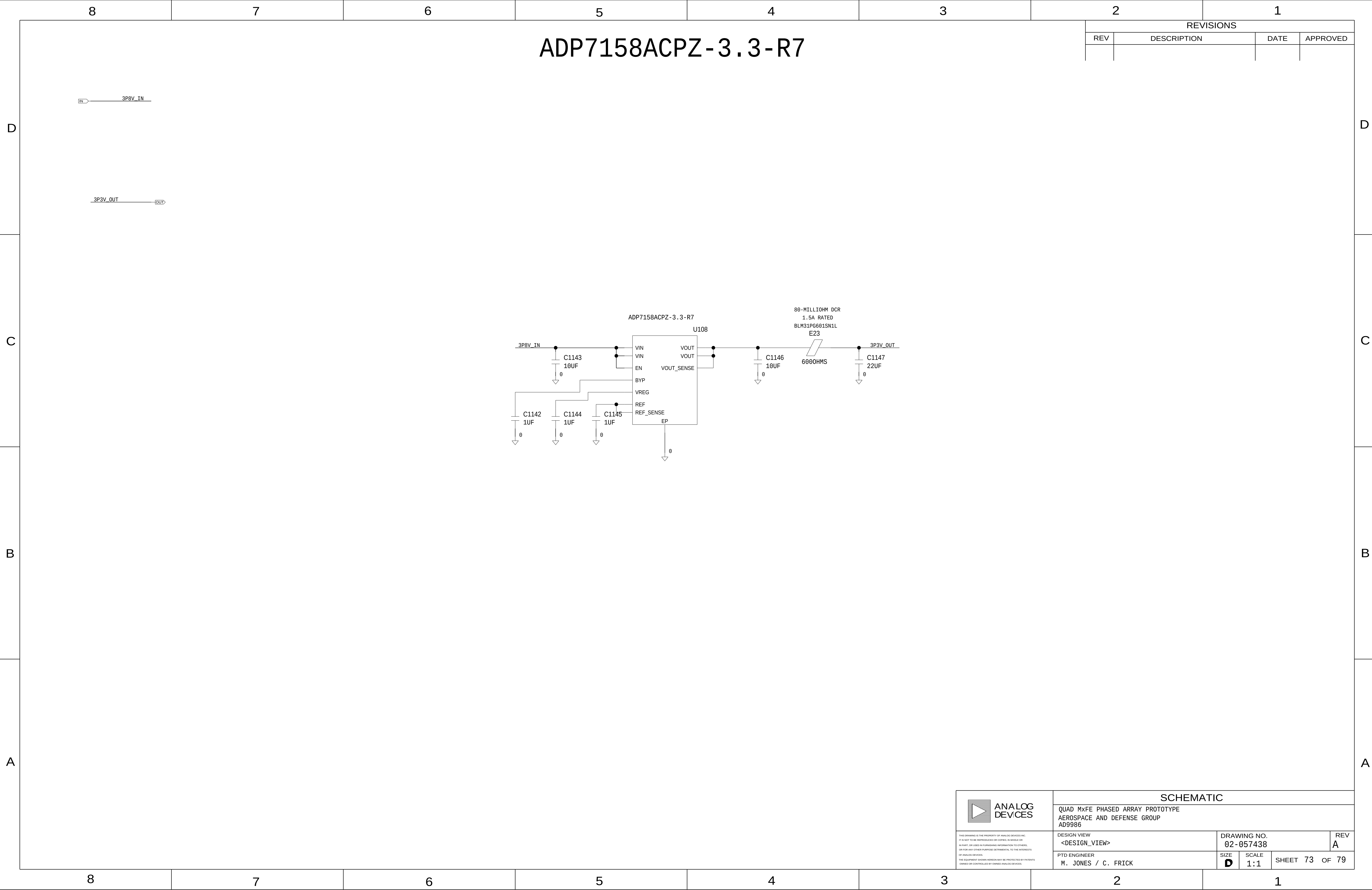
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

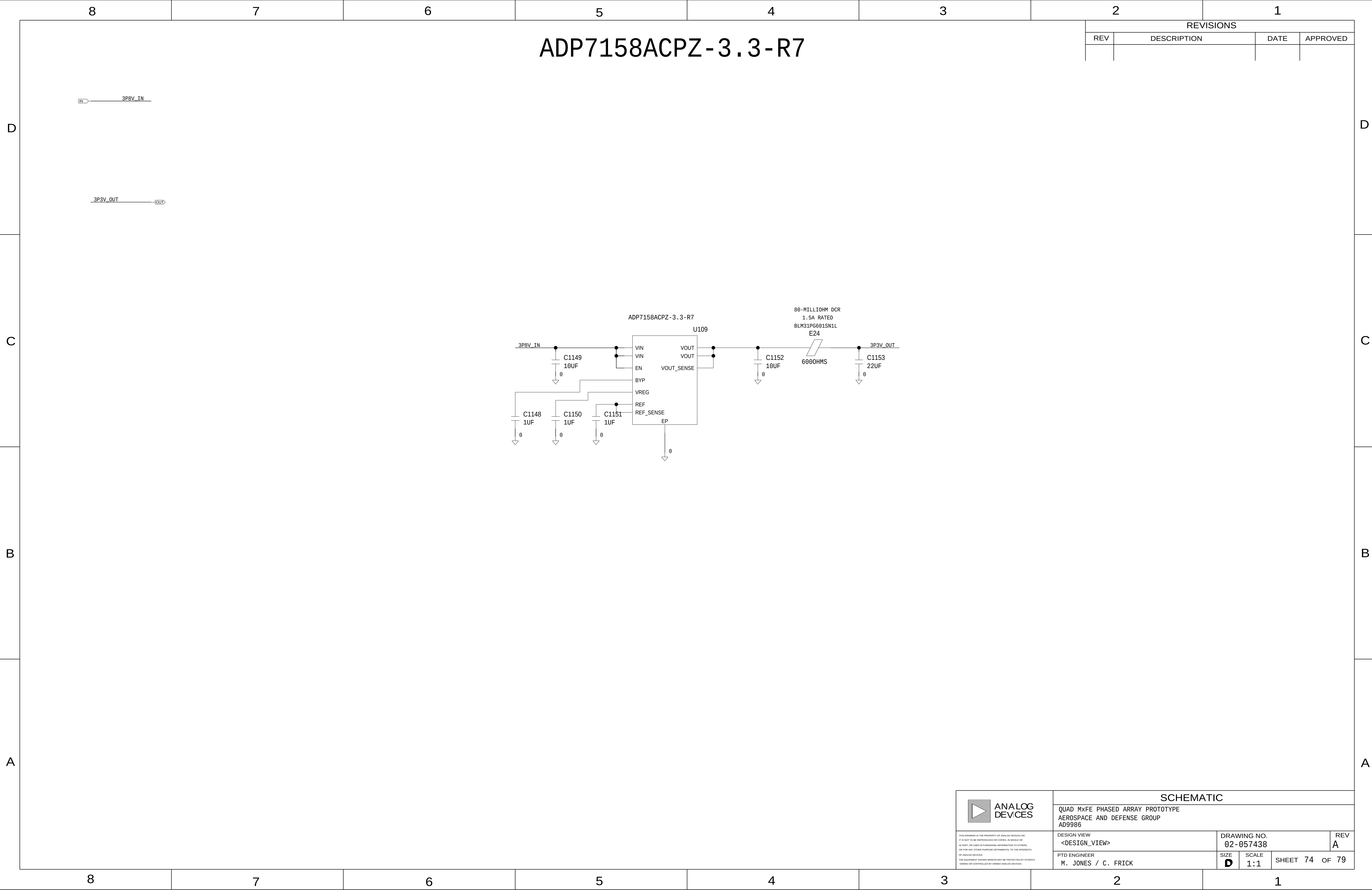


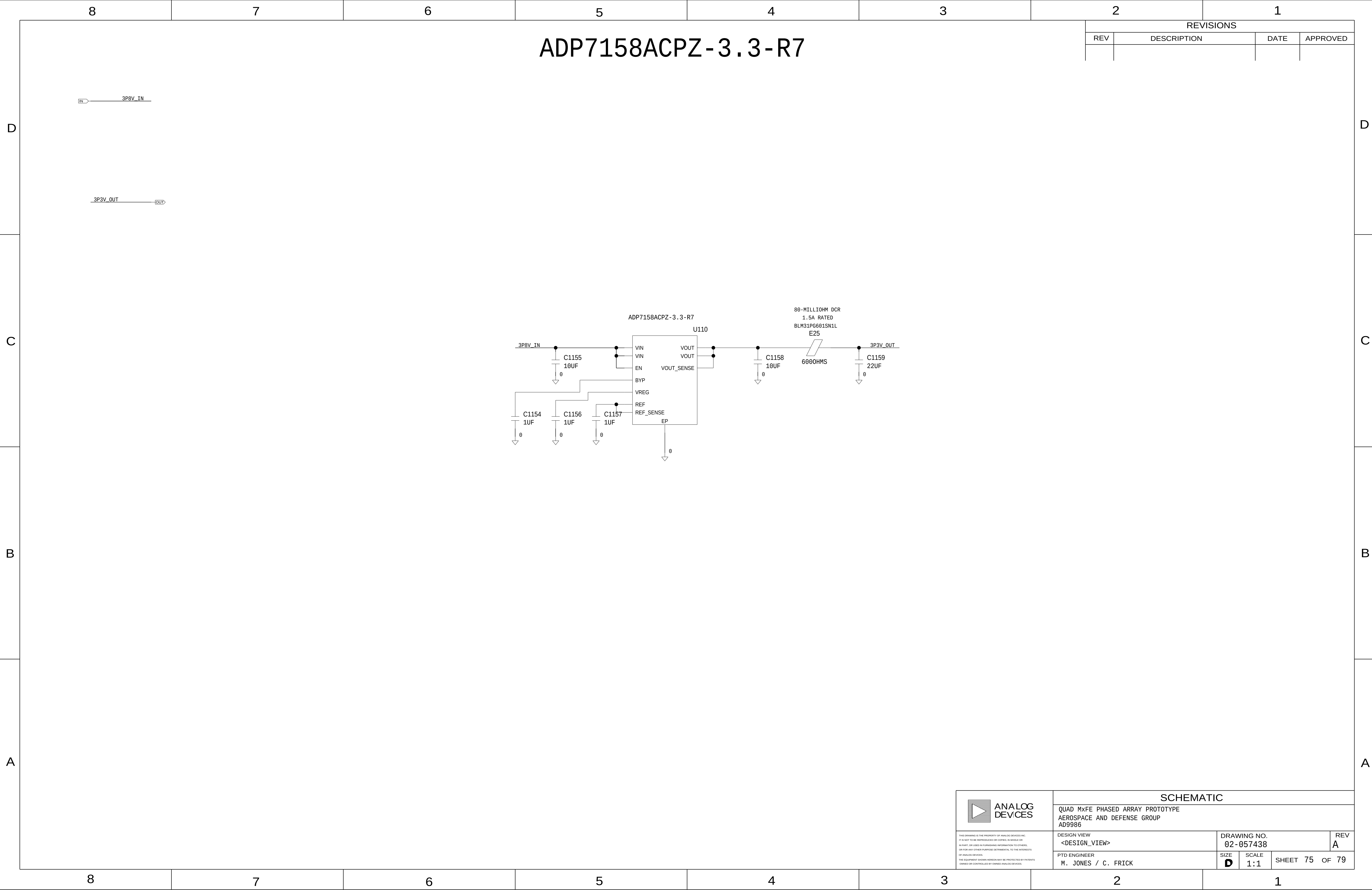
ANALOG
DEVICES

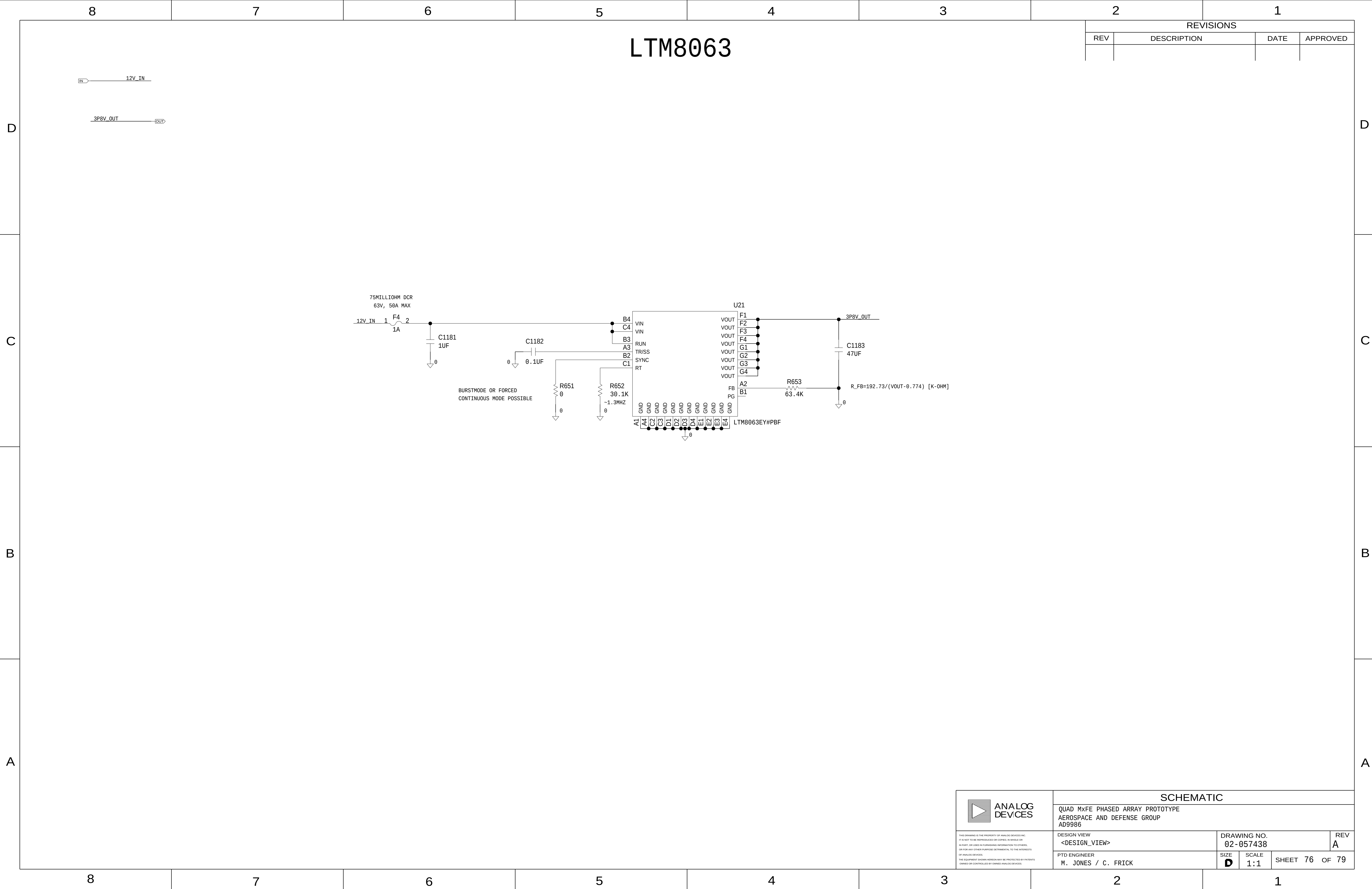
THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC.
IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR
IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS,
OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS
OF ANALOG DEVICES.
THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS
OWNED OR CONTROLLED BY ANALOG DEVICES.

SCHEMATIC				
QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9986				
DESIGN VIEW <DESIGN_VIEW>			DRAWING NO. 02-057438	REV A
PTD ENGINEER M. JONES / C. FRICK			SIZE D	SCALE 1:1
			SHEET 72	OF 79



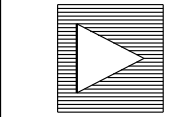
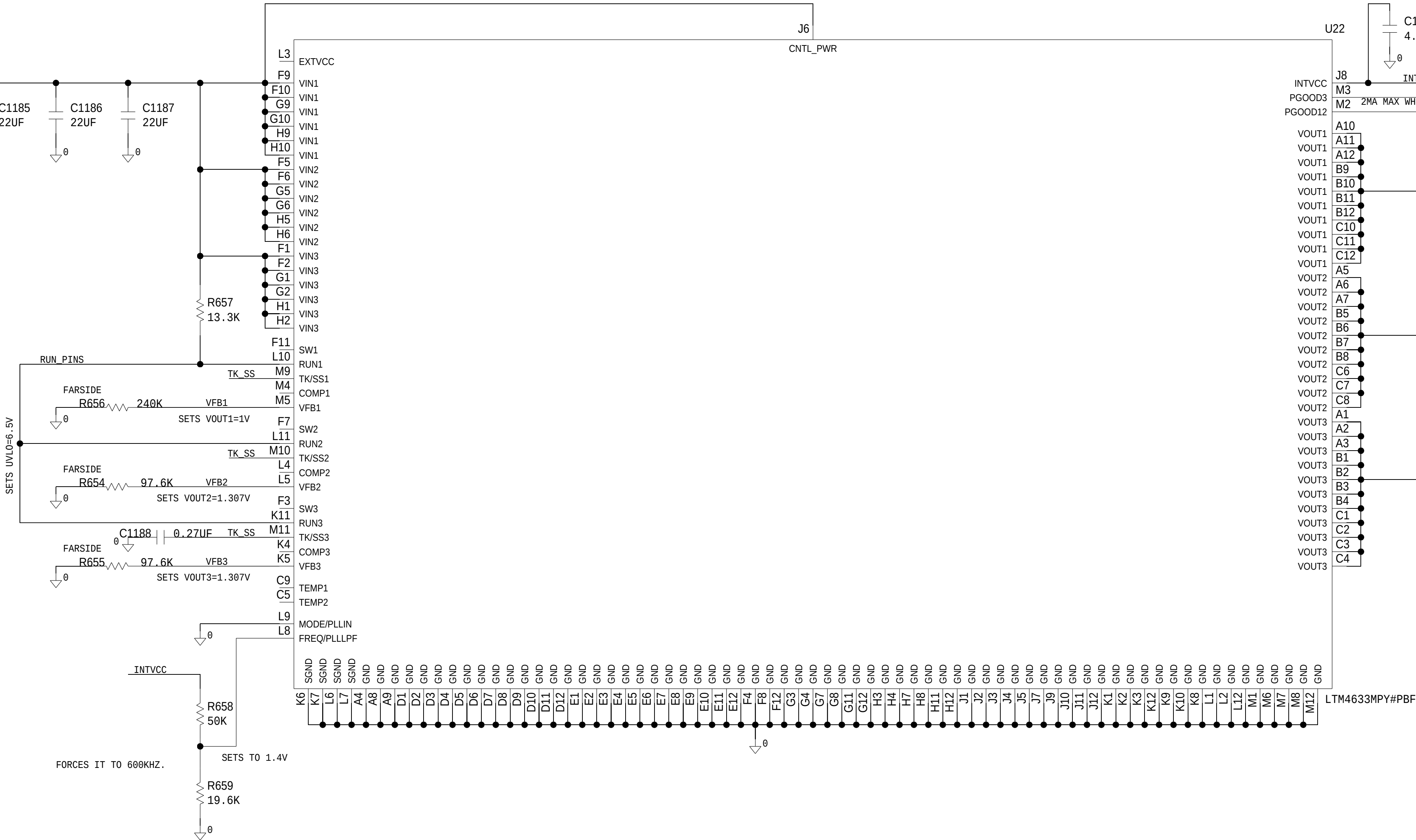
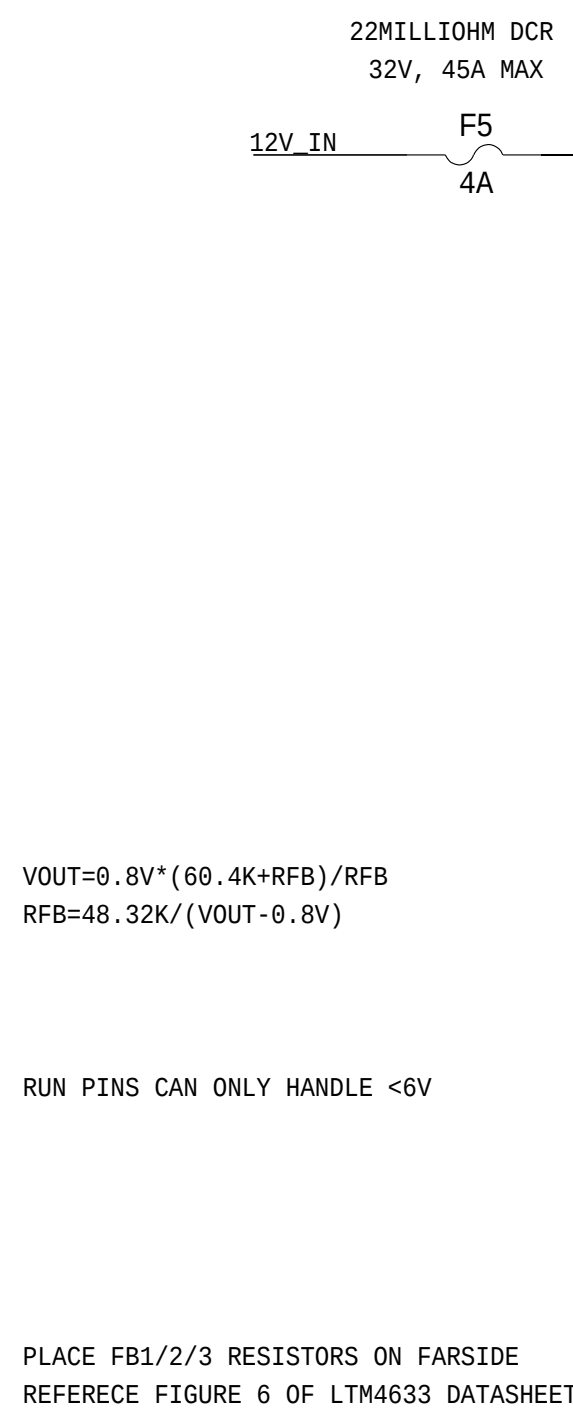
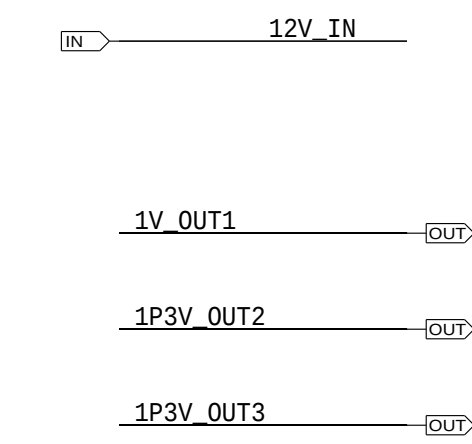






LTM4633

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



ANALOG
DEVICES

THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC.
IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR
IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS,
OR FOR ANY OTHER PURPOSES DETERMINANTAL TO THE INTERESTS
OF ANALOG DEVICES.
THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS
OWNED OR CONTROLLED BY ANALOG DEVICES.

SCHEMATIC

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9986

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
M. JONES / C. FRICK

DRAWING NO.
02-057438

SIZE
D

SCALE
1:1

SHEET 77 OF 79

REV
A

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

