

8		7		6		5		4		3		2		1																																							
D	THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG DEVICES.					JUMPER TABLE <table><tr><th>JP#</th><th>ON</th><th>OFF</th></tr><tr><td>1</td><td></td><td></td></tr><tr><td>2</td><td></td><td></td></tr><tr><td>3</td><td></td><td></td></tr><tr><td>4</td><td></td><td></td></tr><tr><td>5</td><td></td><td></td></tr></table> * SEE ASSEMBLY INSTRUCTIONS					JP#	ON	OFF	1			2			3			4			5			REVISIONS <table><tr><th>REV</th><th>DESCRIPTION</th><th>DATE</th><th>APPROVED</th></tr><tr><td>A</td><td>INITIAL RELEASE</td><td>04APR19</td><td>J. BOWNE</td></tr><tr><td>B</td><td>RECESSED PMCX CONNECTORS, POWER SUPPLY ADDITIONS</td><td>10SEP19</td><td>J. BOWNE</td></tr><tr><td>C</td><td>REROUTED CLK CIRCUITS, ADDED FERRITES TO POWERS</td><td>27AUG20</td><td>J. BOWNE</td></tr><tr><td>D</td><td>DN1'D C288, C387, C586 & C823 TO IMPROVE SPURIOUS</td><td>21JAN21</td><td>M. JONES</td></tr></table>					REV	DESCRIPTION	DATE	APPROVED	A	INITIAL RELEASE	04APR19	J. BOWNE	B	RECESSED PMCX CONNECTORS, POWER SUPPLY ADDITIONS	10SEP19	J. BOWNE	C	REROUTED CLK CIRCUITS, ADDED FERRITES TO POWERS	27AUG20	J. BOWNE	D	DN1'D C288, C387, C586 & C823 TO IMPROVE SPURIOUS	21JAN21	M. JONES
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RELAY CONTROL CHART																																																					
CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR																																																	
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P.O SPEC.		BK/BD SPEC.		SOCKET OEM		OEM PART#		HANDLER																																													

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QUAD MXFE PHASED-ARRAY PLATFORM

8 7 6 5 4 3 2 1

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
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QUAD MXFE PHASED-ARRAY PLATFORM

8 7 6 5 4 3 2 1

REVISIONS

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QUAD MXFE PHASED-ARRAY PLATFORM

8 7 6 5 4 3 2 1

REVISIONS

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QUAD MXFE PHASED-ARRAY PLATFORM

8 7 6 5 4 3 2 1

REVISIONS

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QUAD MXFE PHASED-ARRAY PLATFORM

8 7 6 5 4 3 2 1

REVISIONS

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QUAD MXFE PHASED-ARRAY PLATFORM

8 7 6 5 4 3 2 1

REVISIONS

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QUAD MXFE PHASED-ARRAY PLATFORM

8 7 6 5 4 3 2 1

REVISIONS

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QUAD MXFE PHASED-ARRAY PLATFORM

8 7 6 5 4 3 2 1

REVISIONS

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QUAD MXFE PHASED-ARRAY PLATFORM

8 7 6 5 4 3 2 1

REVISIONS

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QUAD MXFE PHASED-ARRAY PLATFORM

8 7 6 5 4 3 2 1

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
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QUAD MXFE PHASED-ARRAY PLATFORM

8 7 6 5 4 3 2 1

REVISIONS

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QUAD MXFE PHASED-ARRAY PLATFORM

8 7 6 5 4 3 2 1

REVISIONS

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QUAD MXFE PHASED-ARRAY PLATFORM

8 7 6 5 4 3 2 1

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
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QUAD MXFE PHASED-ARRAY PLATFORM

8 7 6 5 4 3 2 1

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
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QUAD MXFE PHASED-ARRAY PLATFORM

8 7 6 5 4 3 2 1

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
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QUAD MXFE PHASED-ARRAY PLATFORM

8 7 6 5 4 3 2 1

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
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2</			

REV	DESCRIPTION	DATE	APPROVED

SCHEMATIC

MXFE PHASED ARRAY PROTOTYPE
 SPACE AND DEFENSE GROUP
 ADQUADMXFE1EBZ_BRD, 2nd Rx Nyquist

EW
N_VIEW>

DEER
ES / C. FRICK

DRAWING NO.
02_057438-02

SCALE
1:1

SHEET 2 OF 80

REV
D

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

The diagram shows the timing relationships for the AD9548 pins. The signals are as follows:

- +3P3V**: Power supply signal.
- +5V PLL**: PLL power supply signal.
- +5V AMP**: AMP power supply signal.
- SPI_CLK**: SPI clock signal.
- SPI_CS#**: SPI chip select signal.
- 500MHZ_REFIN**: 500 MHz reference input signal.
- EXT_CLK**: External clock signal.
- ADRF5020_CTRL**: ADRF5020 control signal.
- LOW_FREQ_CLK_P**: Low frequency clock signal (positive).
- LOW_FREQ_CLK_N**: Low frequency clock signal (negative).

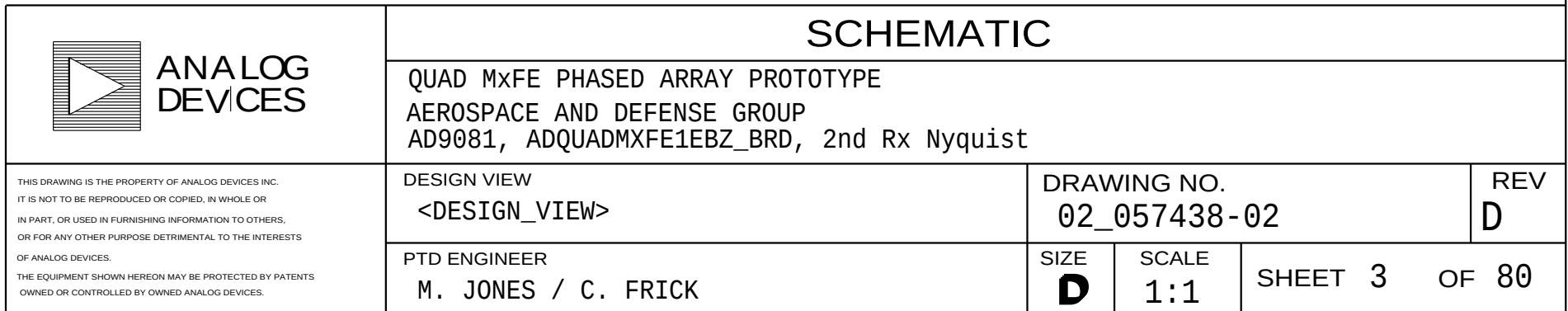
CLK_OUT_P

CLK_OUT_N

500MHZ_RF8_P

500MHZ_RF8_N

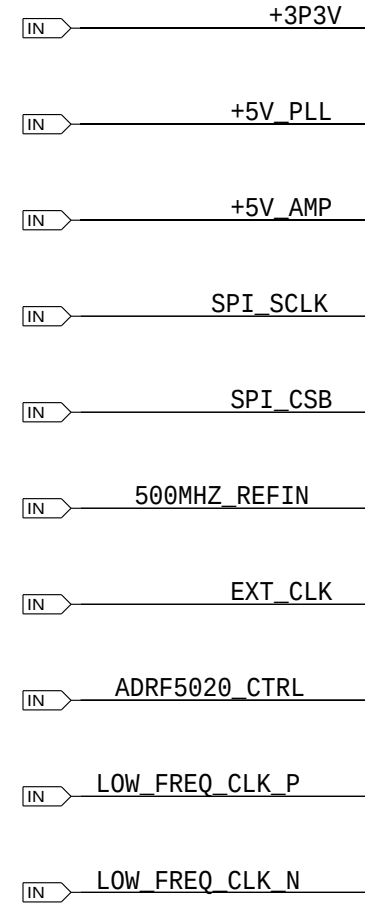
SPI_SDIO IO



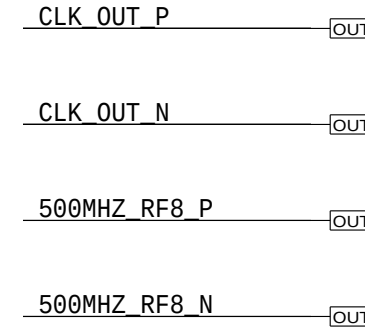
CLOCK GENERATION

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

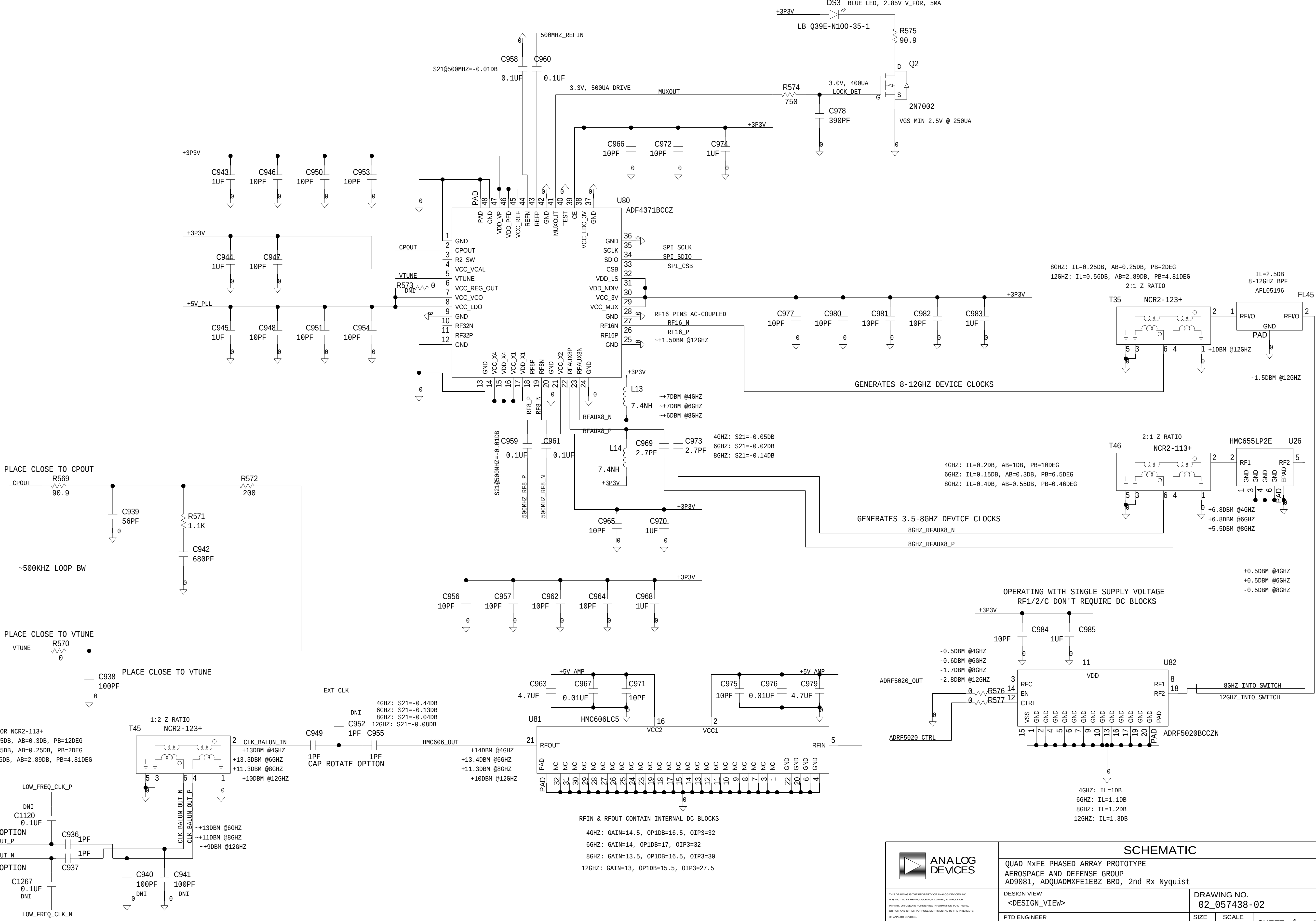
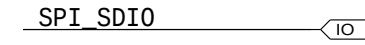
INPUTS



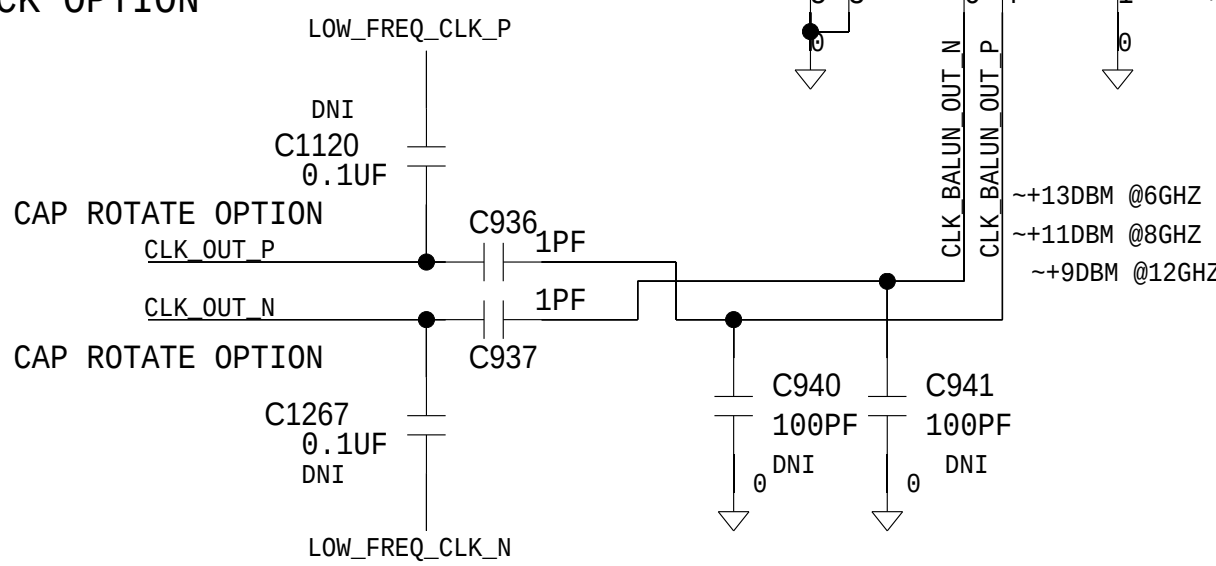
OUTPUTS



I/O



LOW FREQUENCY DEVICE CLOCK OPTION FROM HMC7043



RFIN & RFOUT CONTAIN INTERNAL DC BLOCKS

4GHZ: GAIN=14.5, OP1DB=16.5, OIP3=32
6GHZ: GAIN=14, OP1DB=17, OIP3=32
8GHZ: GAIN=13.5, OP1DB=16.5, OIP3=30
12GHZ: GAIN=13, OP1DB=15.5, OIP3=27.5

SCHEMATIC			
QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9081, ADQUADMxFE1EBZ_BRD, 2nd Rx Nyquist			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_057438-02		REV D
PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 4 OF 80

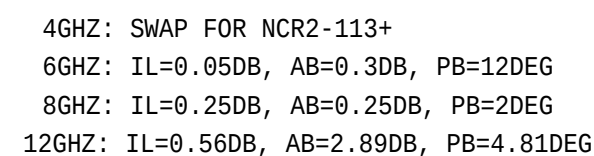
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

The diagram shows the timing relationships for the AD9288. The signals are as follows:

- +3P3V**: Power supply voltage, shown as a constant high level.
- +5V PLL**: PLL supply voltage, shown as a constant high level.
- +5V AMP**: AMP supply voltage, shown as a constant high level.
- SPI_CLK**: SPI clock signal, shown as a periodic square wave.
- SPI_CS#**: SPI chip select signal, shown as a periodic square wave.
- 500MHZ_REFIN**: 500 MHz reference input signal, shown as a periodic square wave.
- EXT_CLK**: External clock signal, shown as a periodic square wave.
- ADRF5020_CTRL**: ADRF5020 control signal, shown as a periodic square wave.
- LOW_FREQ_CLK_P**: Low frequency clock signal (positive), shown as a periodic square wave.
- LOW_FREQ_CLK_N**: Low frequency clock signal (negative), shown as a periodic square wave.

CLK_OUT_P	OUT
CLK_OUT_N	OUT
500MHZ_RF8_P	OUT
500MHZ_RF8_N	OUT

SPI_SDIO IO



CLK_OPTION

LOW_FREQ_CLK_P

DNI

C1293
0.1uF

CAP_ROTATE_OPTION

CLK_OUT_P

C986
1pF

CLK_OUT_N

C987
1pF

CAP_ROTATE_OPTION

C1312
0.1uF

DNI

LOW_FREQ_CLK_N

C990
100pF

DNI

C991
100pF

DNI

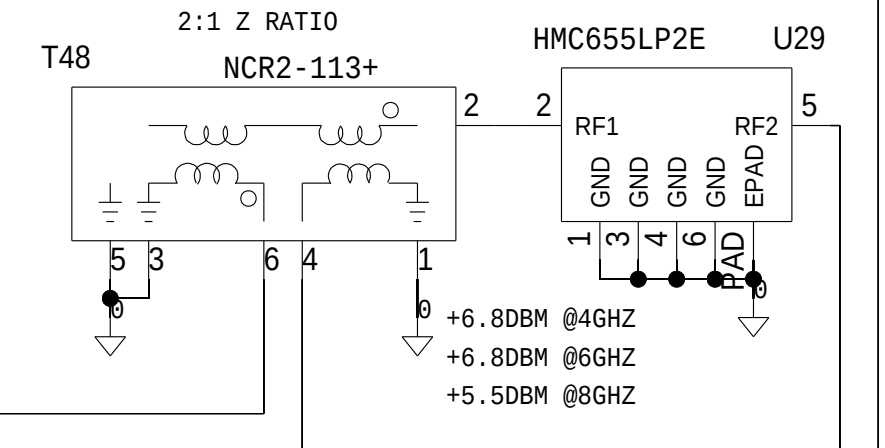
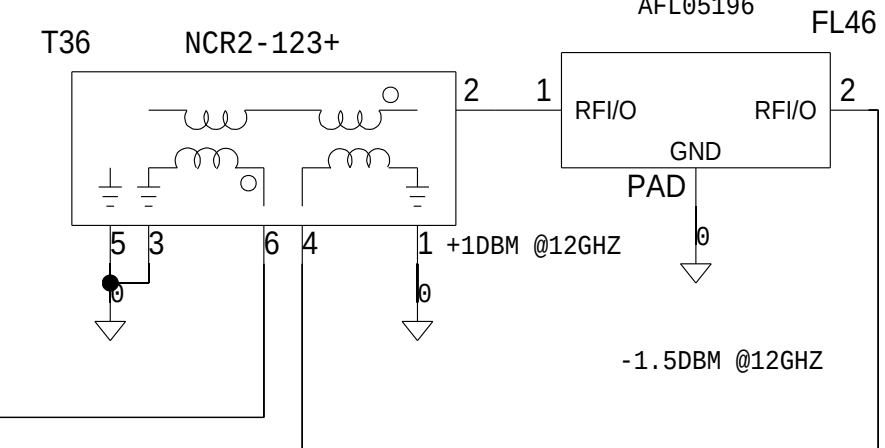
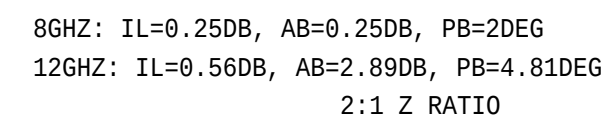
CLK_BALUN_OUT_N

CLK_BALUN_OUT_P

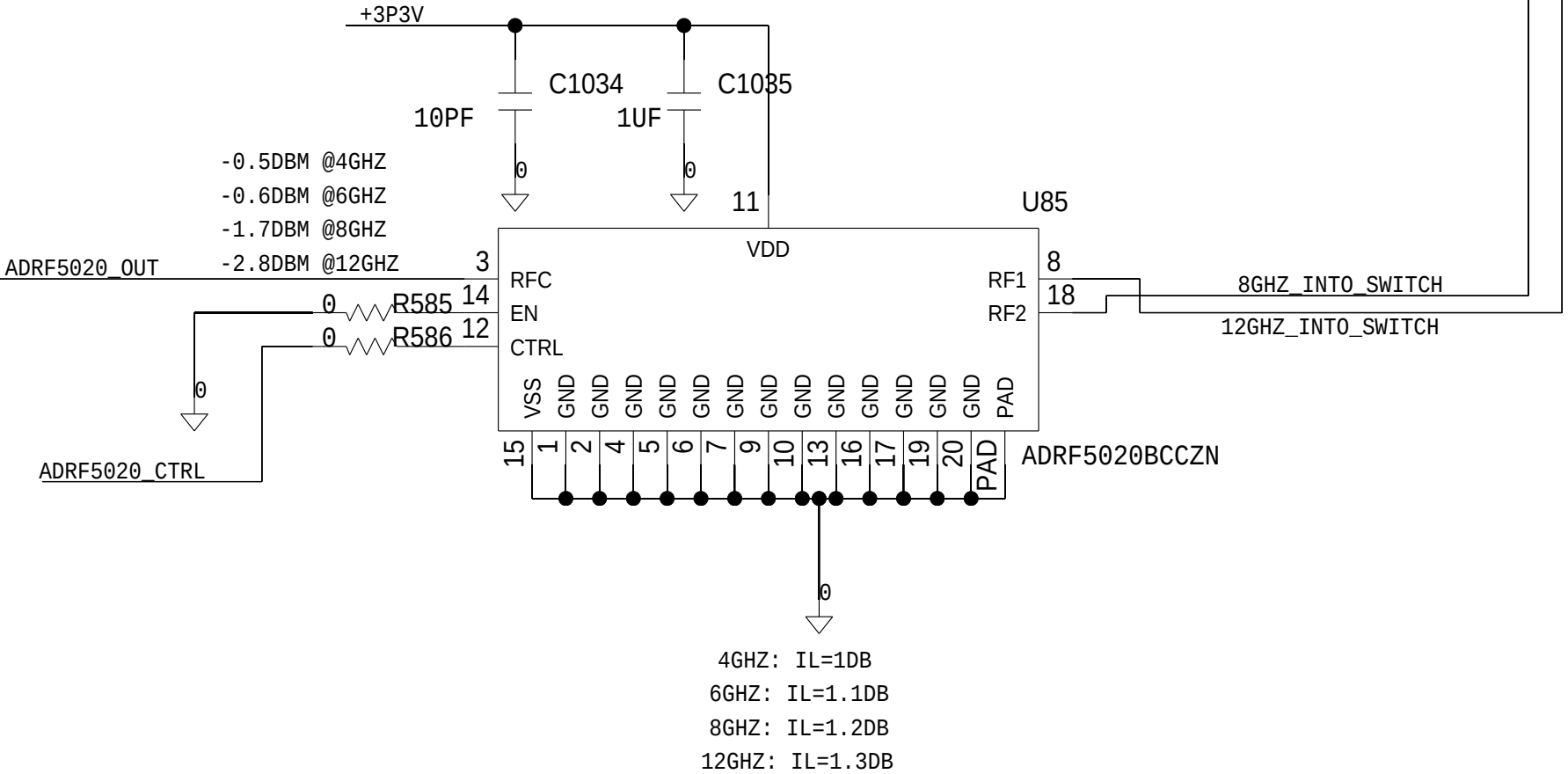
+13DBM @6GHZ

+11DBM @8GHZ

+9DBM @12GHZ

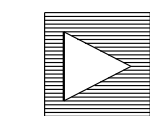


OPERATING WITH SINGLE SUPPLY VOLTAGE
RF1/2/C DON'T REQUIRE DC BLOCKS



RFIN & RFOUT CONTAIN INTERNAL DC BLOCKS

4GHZ: GAIN=14.5, OP1DB=16.5, OIP3=32
6GHZ: GAIN=14, OP1DB=17, OIP3=32
8GHZ: GAIN=13.5, OP1DB=16.5, OIP3=30
12GHZ: GAIN=13, OP1DB=15.5, OIP3=27.5

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QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9081, ADQUADMXFE1EBZ_BRD, 2nd Rx Nyquist

DESIGN VIEW	<DESIGN_VIEW>
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PTD ENGINEER
M. JONES / C. FRICK

DRAWING NO.
02 057438-02

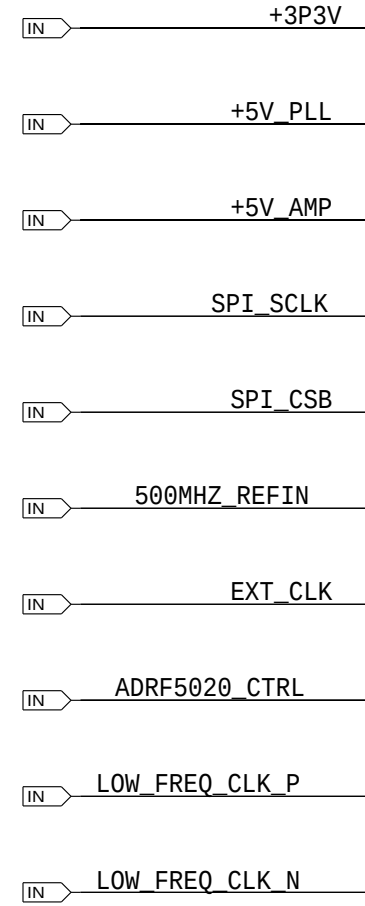
SIZE D	SCALE 1:1	SHEET 5 OF 80
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REV
D

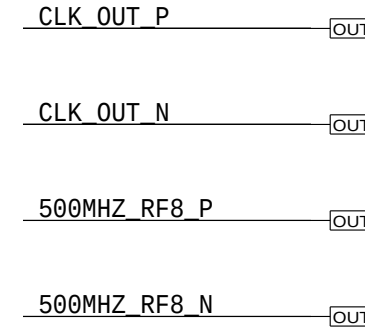
CLOCK GENERATION

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

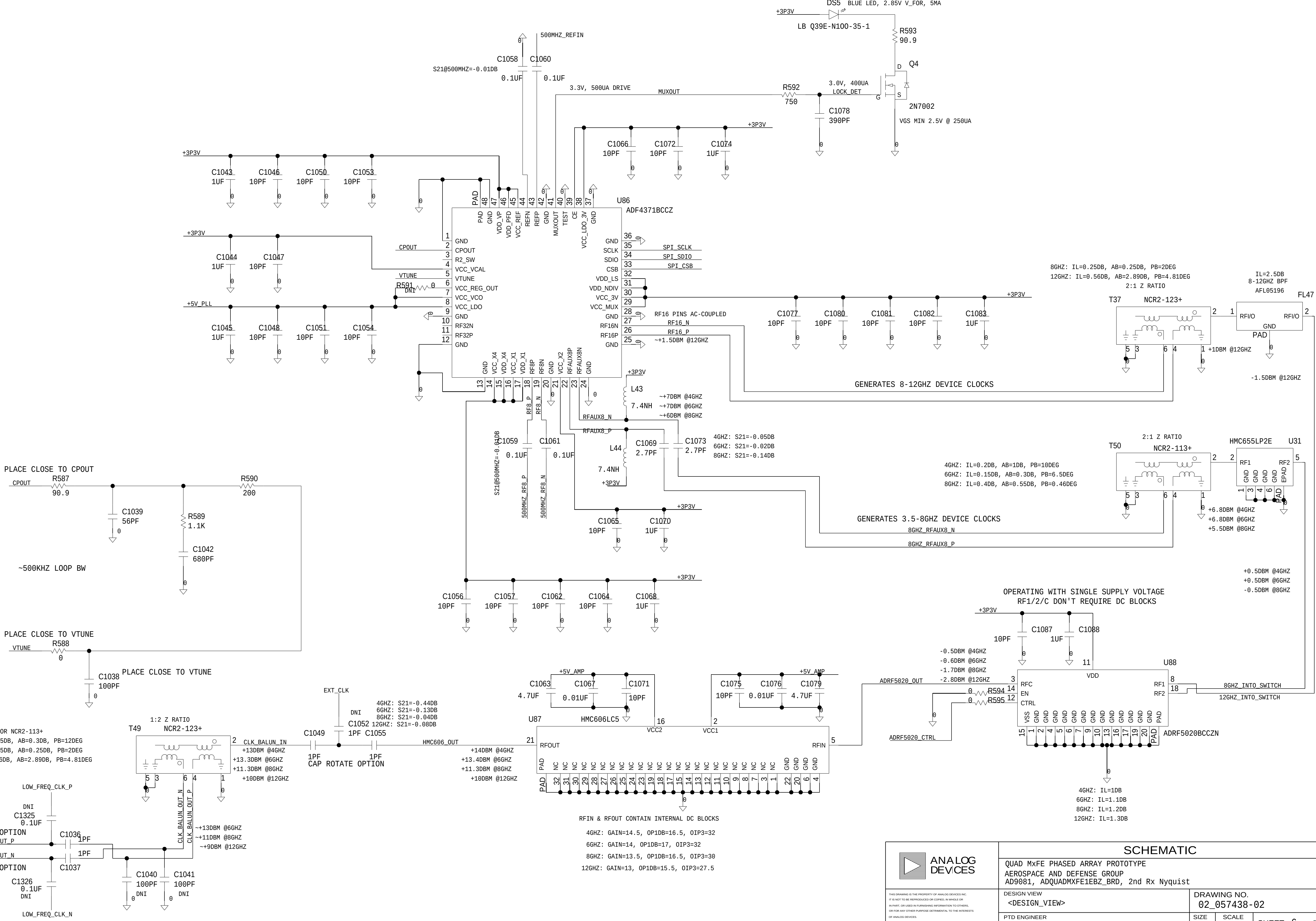
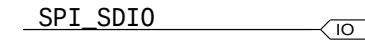
INPUTS



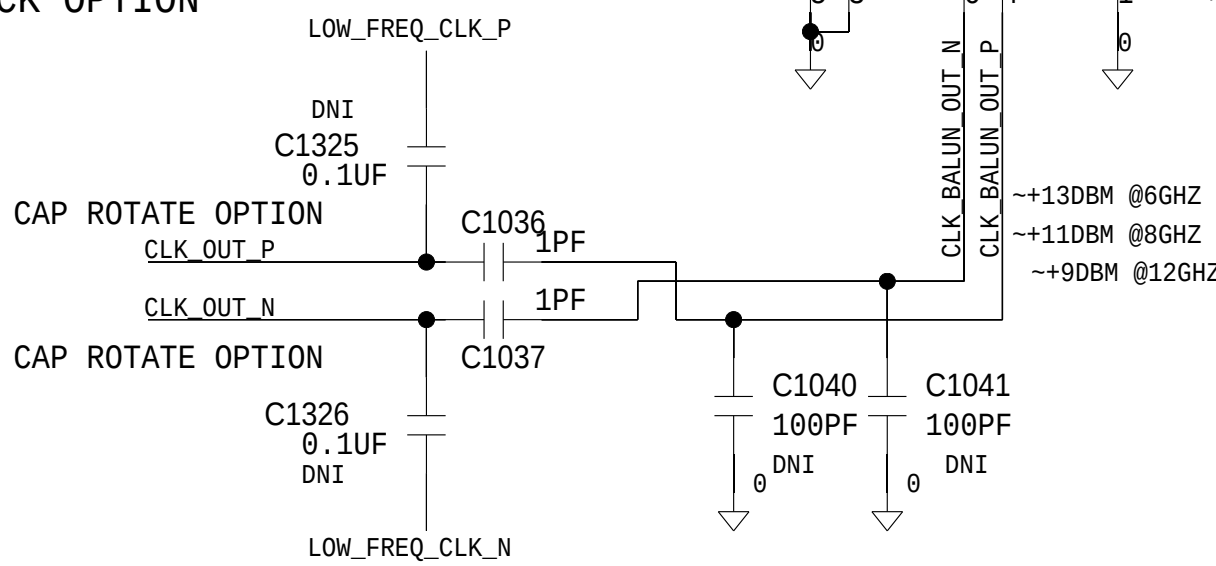
OUTPUTS



I/O



LOW FREQUENCY DEVICE CLOCK OPTION FROM HMC7043



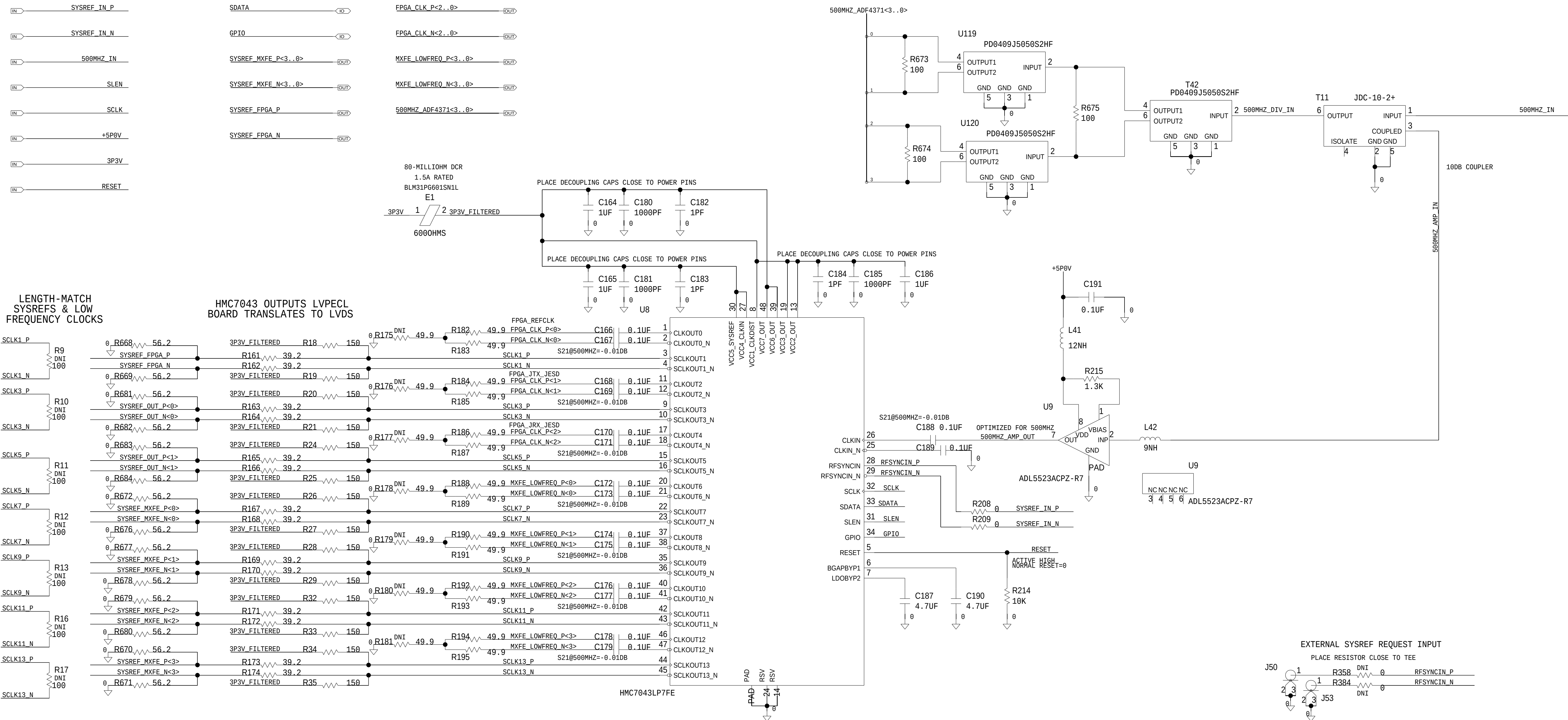
RFIN & RFOUT CONTAIN INTERNAL DC BLOCKS

4GHZ: GAIN=14.5, OP1DB=16.5, OIP3=32
6GHZ: GAIN=14, OP1DB=17, OIP3=32
8GHZ: GAIN=13.5, OP1DB=16.5, OIP3=30
12GHZ: GAIN=13, OP1DB=15.5, OIP3=27.5

SCHEMATIC			
QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9081, ADQUADMxFE1EBZ_BRD, 2nd Rx Nyquist			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_057438-02	REV D	
PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 6 OF 80

CLOCK FRONT END

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

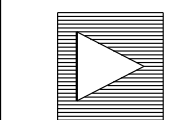


LENGTH-MATCH
SYSREFS & LOW
FREQUENCY CLOCKS

HMC7043 OUTPUTS LVPECL
BOARD TRANSLATES TO LVDS

EXTERNAL SYSREF REQUEST INPUT

PLACE RESISTOR CLOSE TO TEE



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SCHEMATIC

QUAD MXFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9081, ADQUADMXFE1EBZ_BRD, 2nd Rx Nyquist

DESIGN VIEW
<DESIGN_VIEW>

DRAWING NO.
02_057438-02

REV
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PTD ENGINEER
M. JONES / C. FRICK

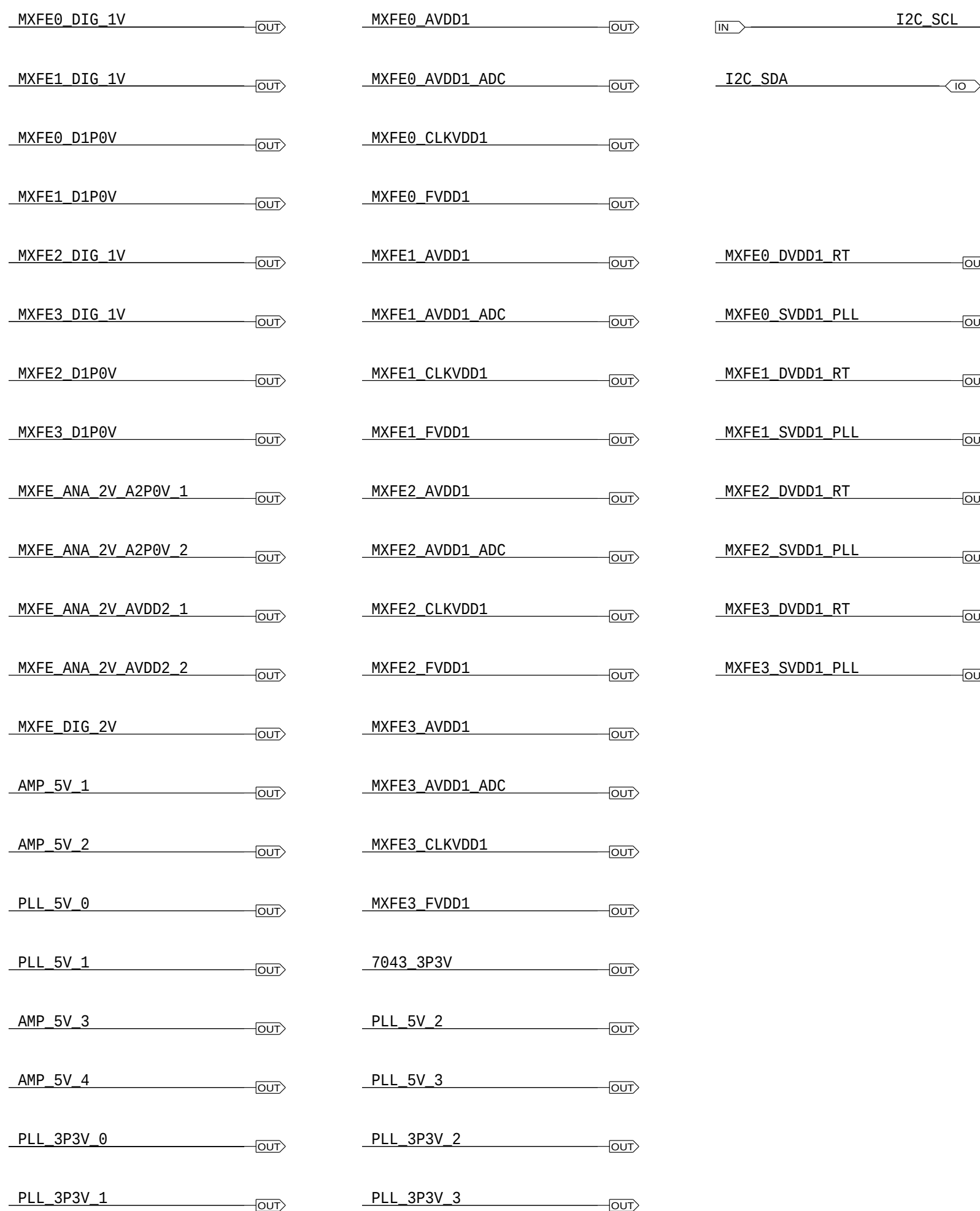
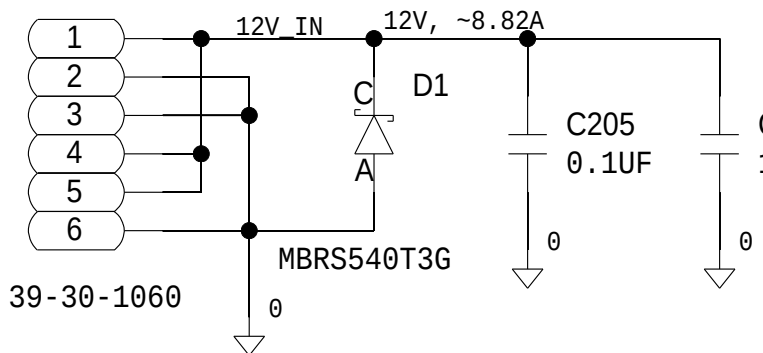
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SCALE
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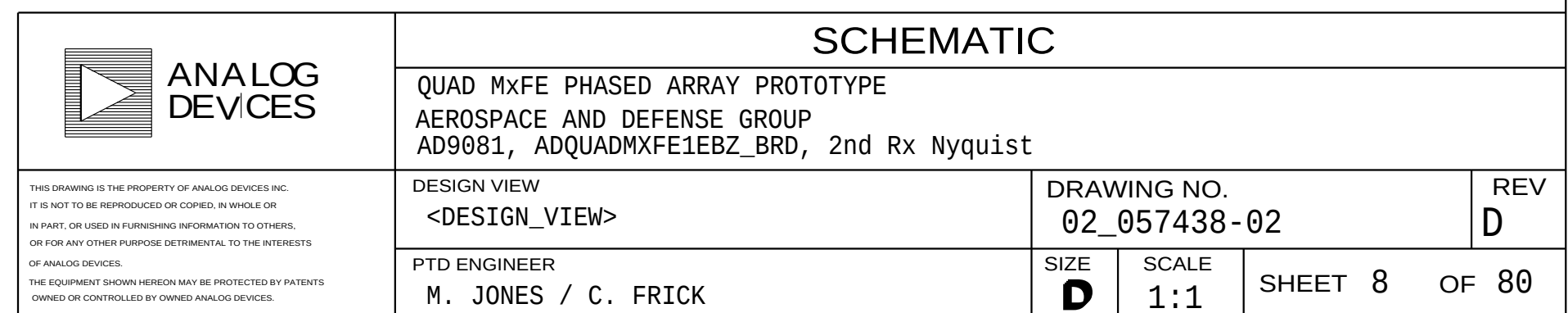
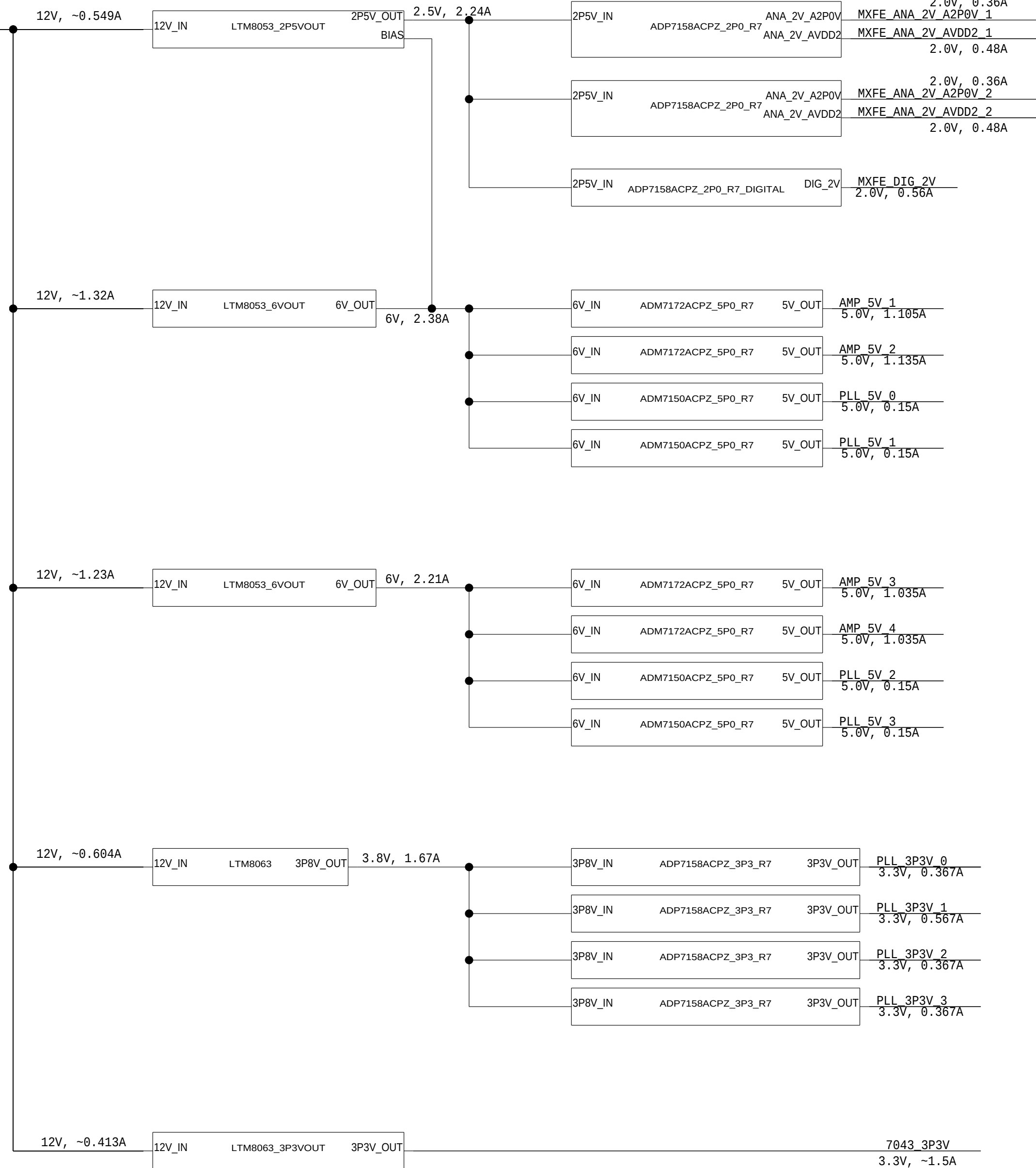
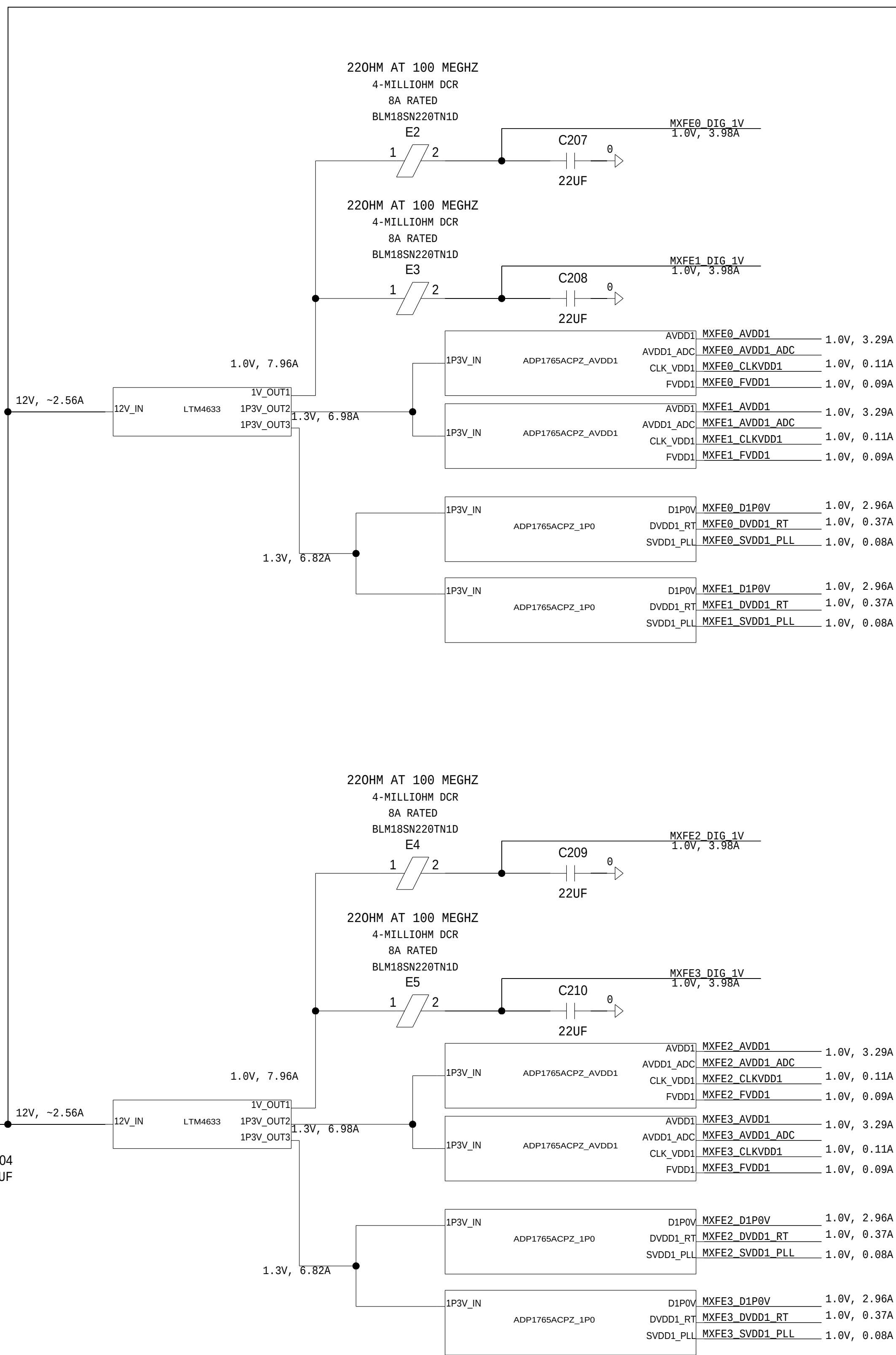
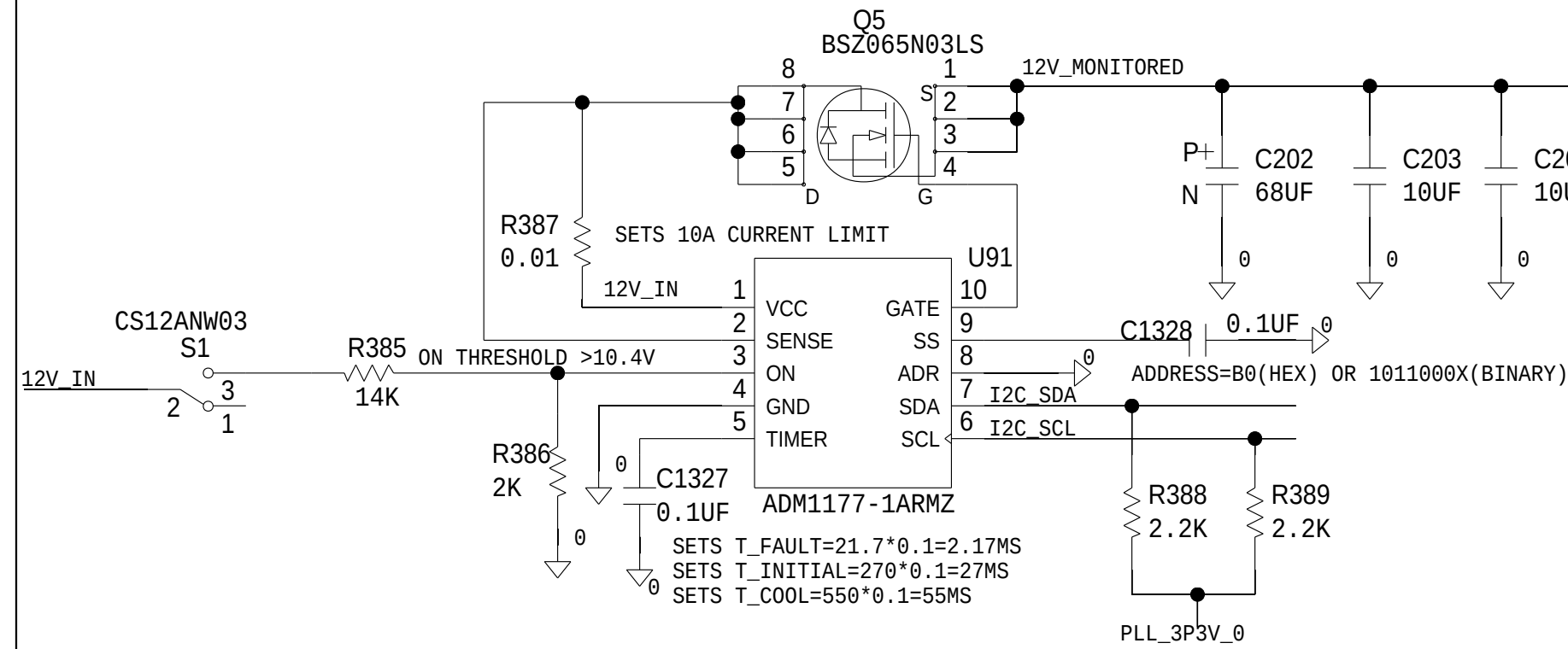
SHEET 7 OF 80

POWER

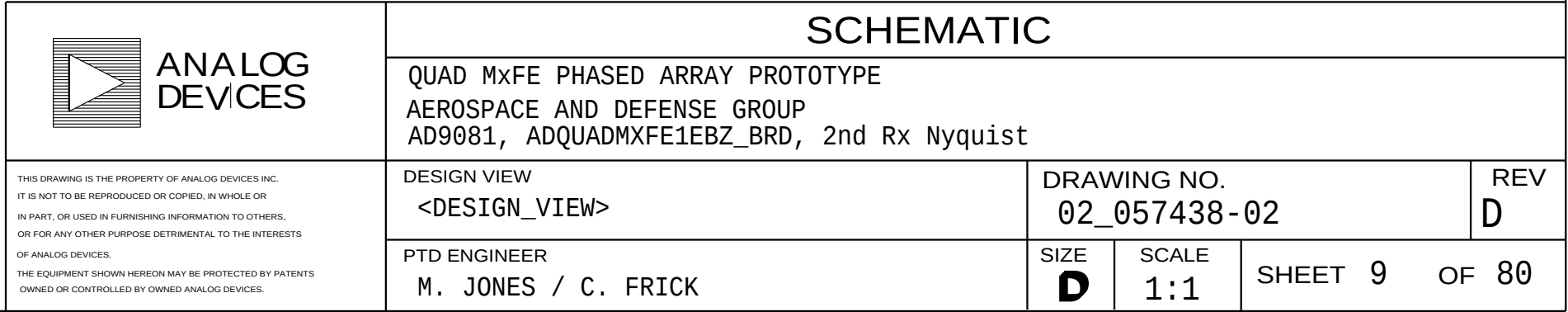
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



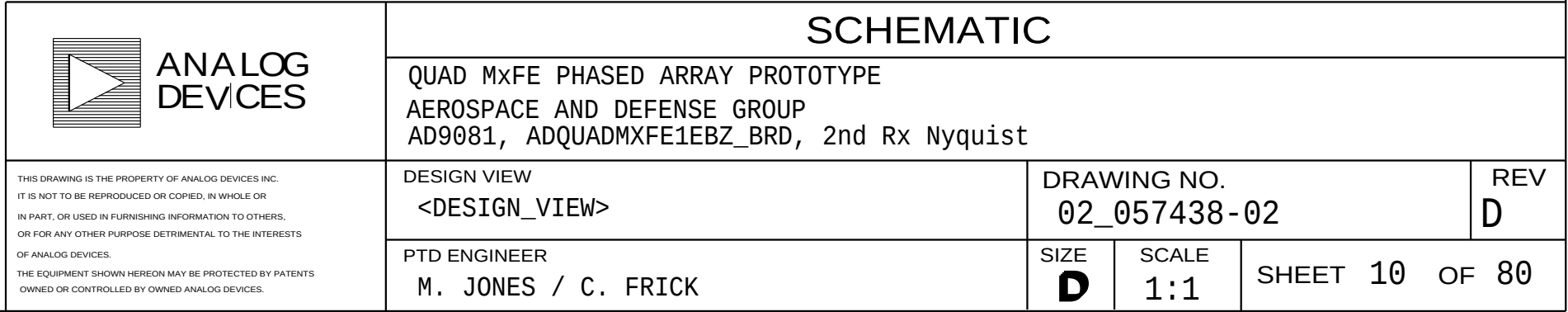
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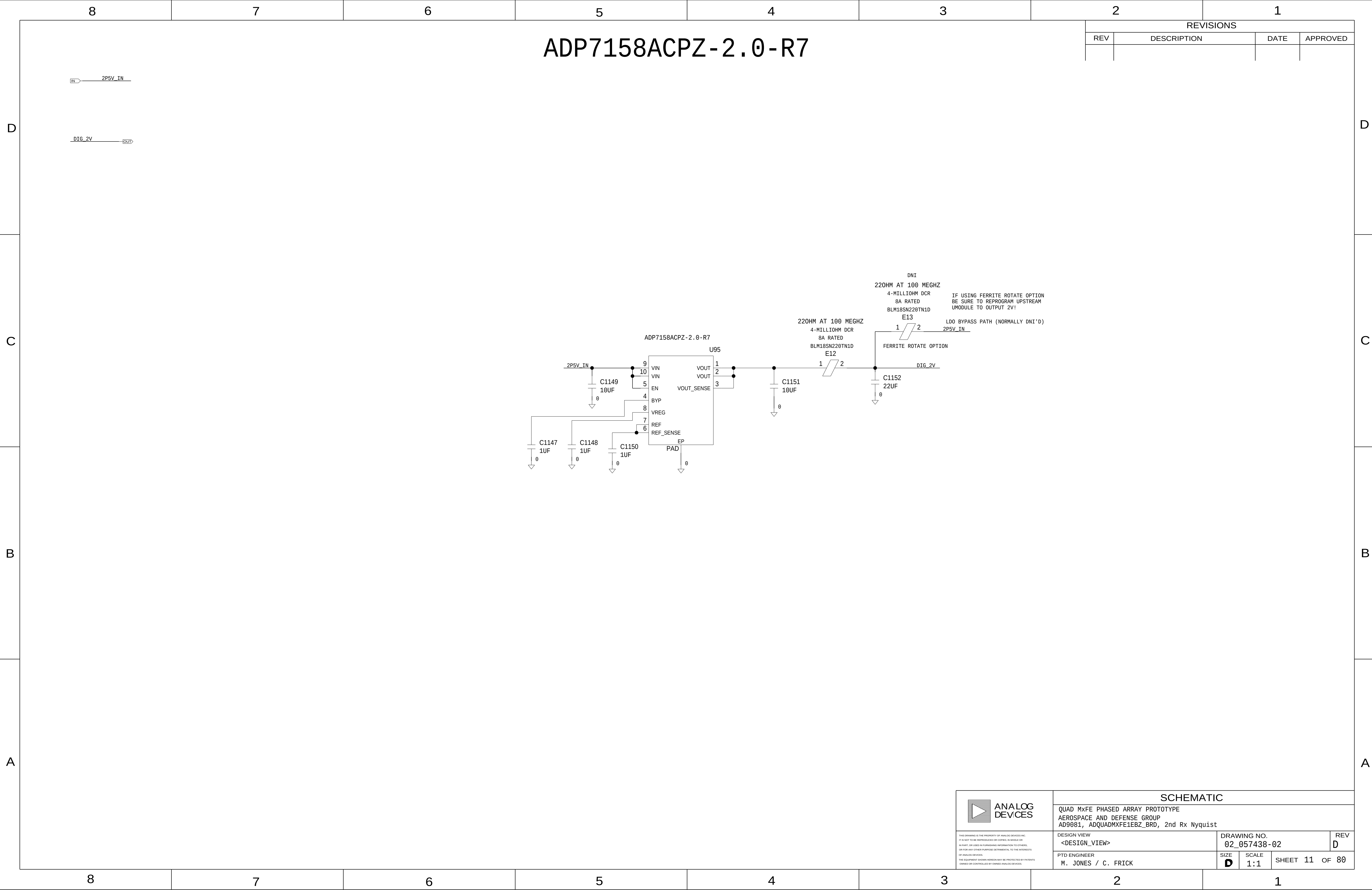


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



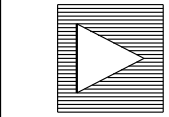
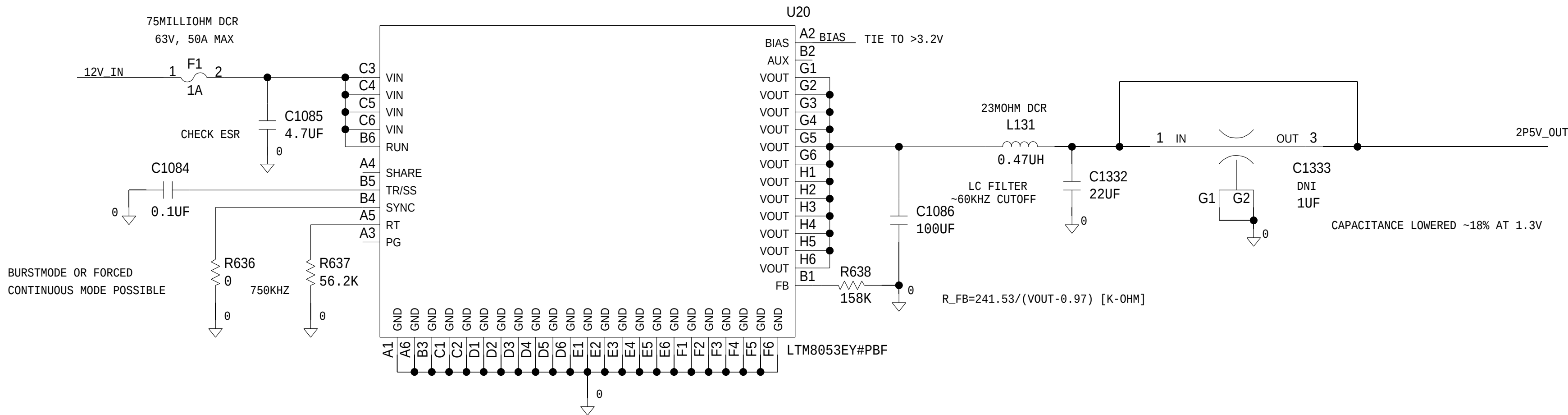


LTM8053 2.5V OUTPUT

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

12V_IN
BIAS

2P5V_OUT



ANALOG
DEVICES

SCHEMATIC

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9081, ADQUADMxFE1EBZ_BRD, 2nd Rx Nyquist

DESIGN VIEW
<DESIGN_VIEW>

DRAWING NO.
02_057438-02

REV
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PTD ENGINEER
M. JONES / C. FRICK

SIZE
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SCALE
1:1

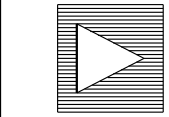
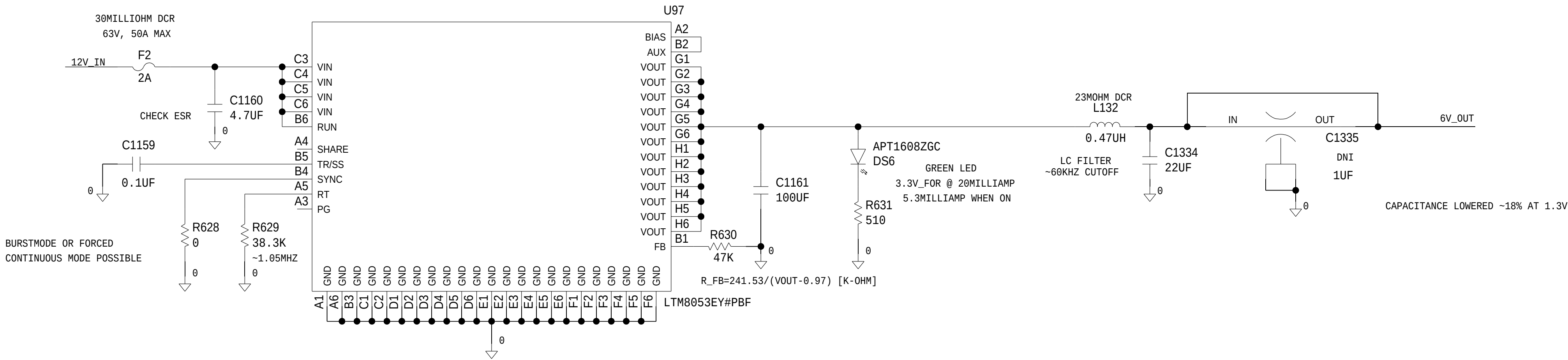
SHEET 12 OF 80

LTM8053 6V OUTPUT

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

12V_IN

6V_OUT



ANALOG
DEVICES

SCHEMATIC

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9081, ADQUADMxFE1EBZ_BRD, 2nd Rx Nyquist

DESIGN VIEW
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DRAWING NO.
02_057438-02

REV
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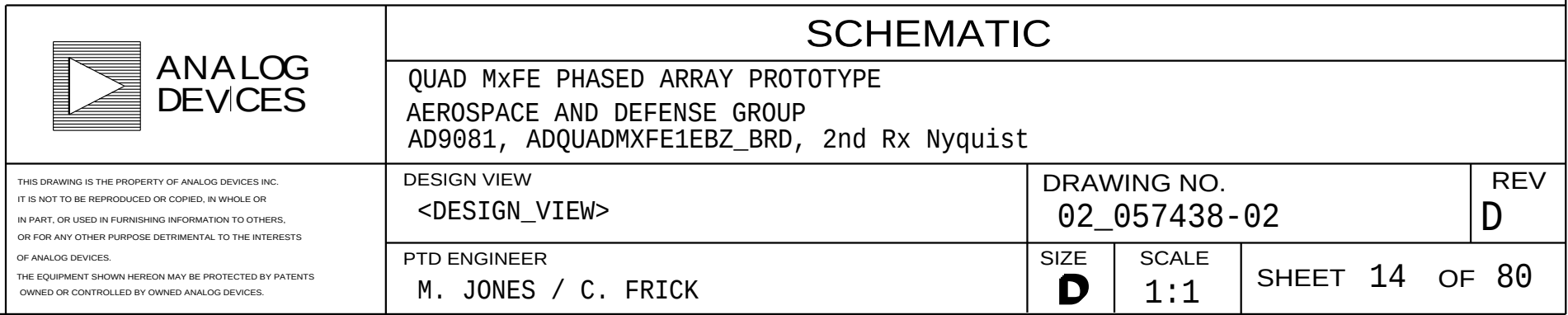
PTD ENGINEER
M. JONES / C. FRICK

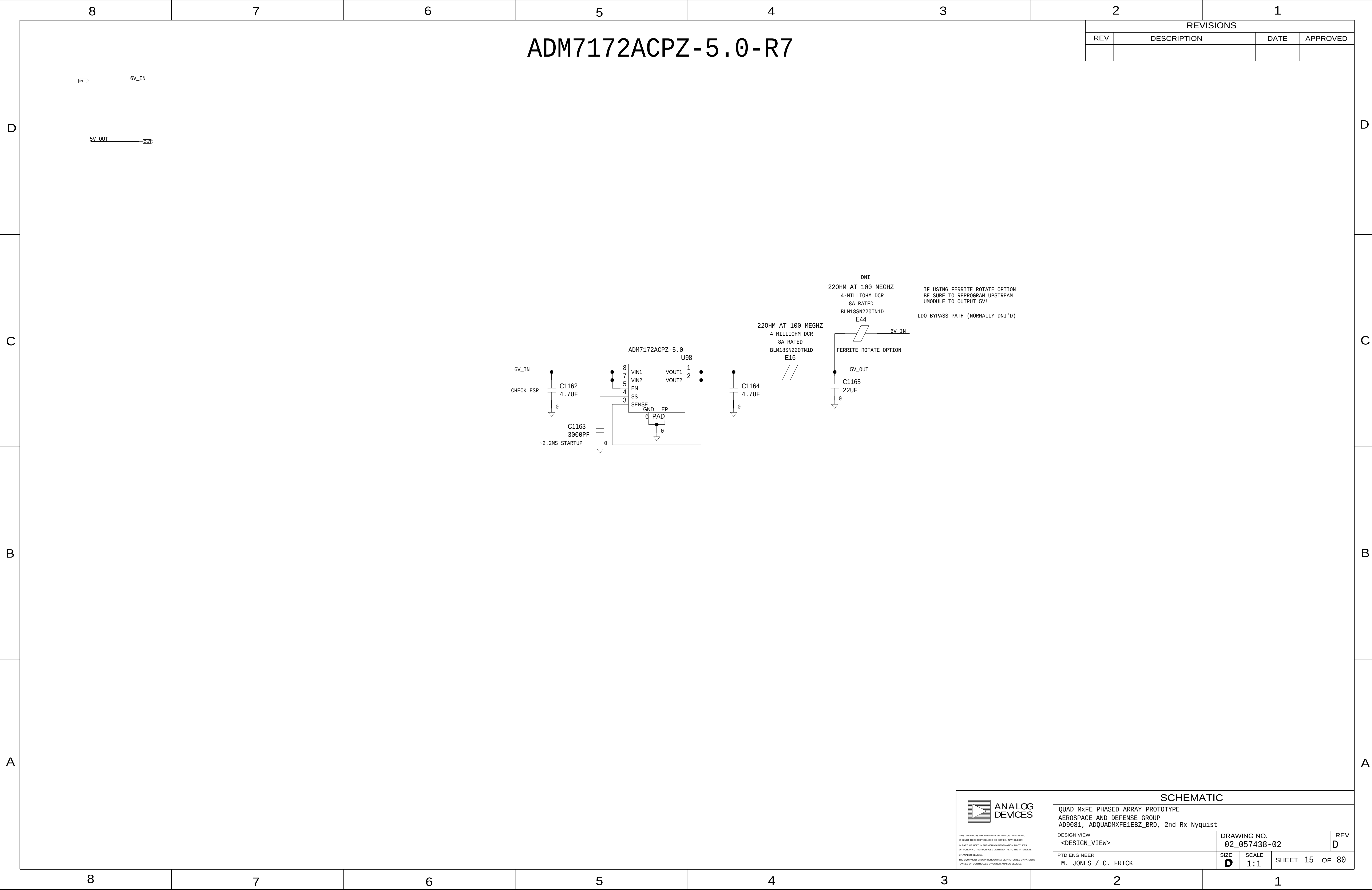
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SCALE
1:1

SHEET 13 OF 80

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED





87654321

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

ADM7172ACPZ-5.0-R7

6V_IN

5V_OUT

6V_IN

5V_OUT

ADM7172ACPZ-5.0

U99

VIN1

VIN2

EN

SS

SENSE

GND

EP

PAD

1

2

VOUT1

VOUT2

C1166

4.7UF

C1167

3000PF

-2.2MS

STARTUP

C1168

4.7UF

C1169

22UF

220HM

AT 100

MEGHZ

4-MILLIOHM

DCR

8A

RATED

BLM18SN220TN1D

E17

DNI

220HM

AT 100

MEGHZ

4-MILLIOHM

DCR

8A

RATED

BLM18SN220TN1D

E45

FERRITE

ROTATE

OPTION

IF USING FERRITE ROTATE OPTION

BE SURE TO REPROGRAM UPSTREAM

UMODULE TO OUTPUT 5V!

LDO BYPASS PATH (NORMALLY DNI'D)

ANALOG

DEVICES

SCHEMATIC

QUAD MxFE PHASED ARRAY PROTOTYPE

AEROSPACE AND DEFENSE GROUP

AD9081, ADQUADMxFE1EBZ_BRD, 2nd Rx Nyquist

DESIGN VIEW

<DESIGN_VIEW>

PTD ENGINEER

M. JONES / C. FRICK

DRAWING NO.

02_057438-02

REV

D

SIZE

D

SCALE

1:1

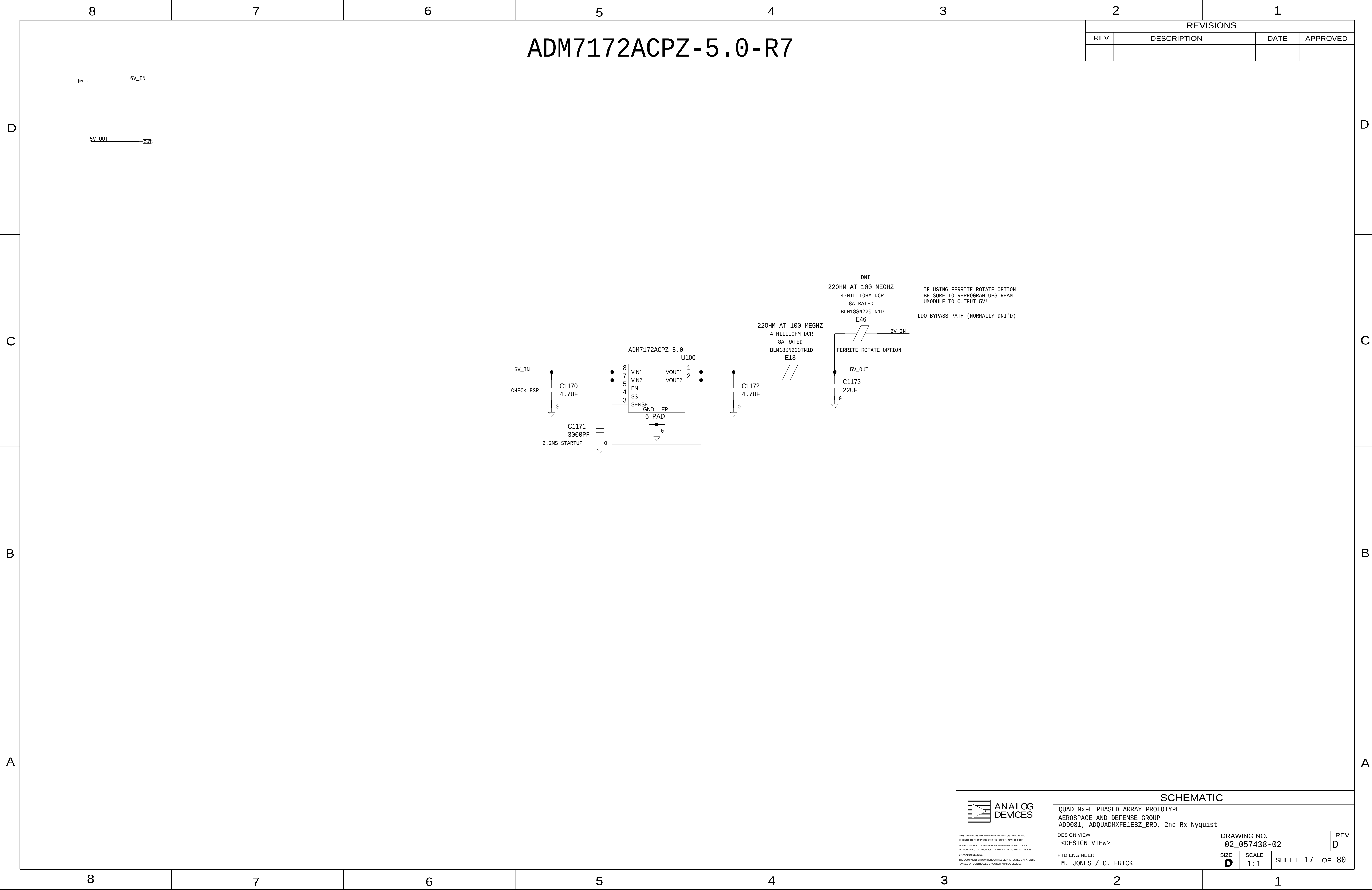
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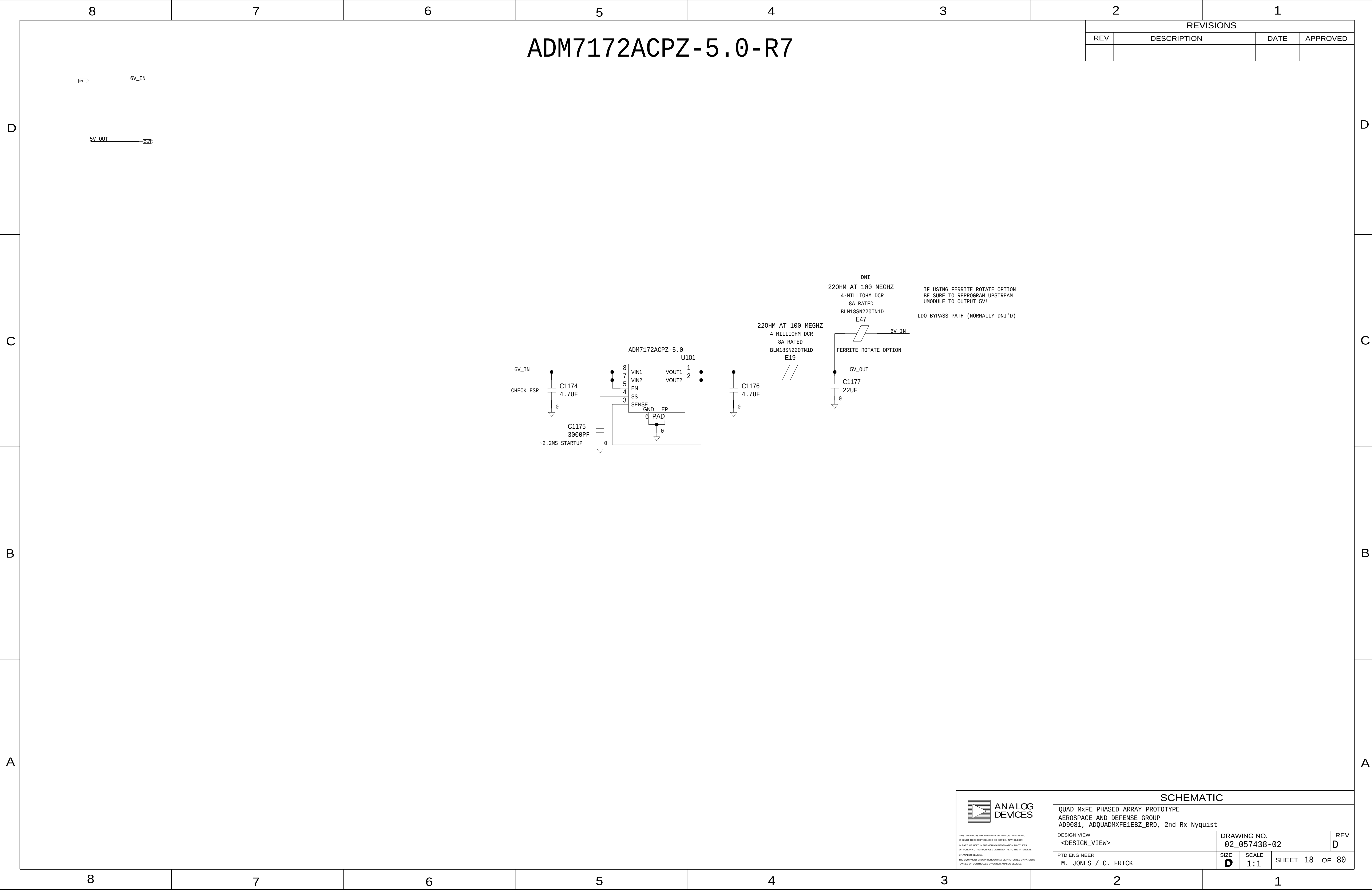
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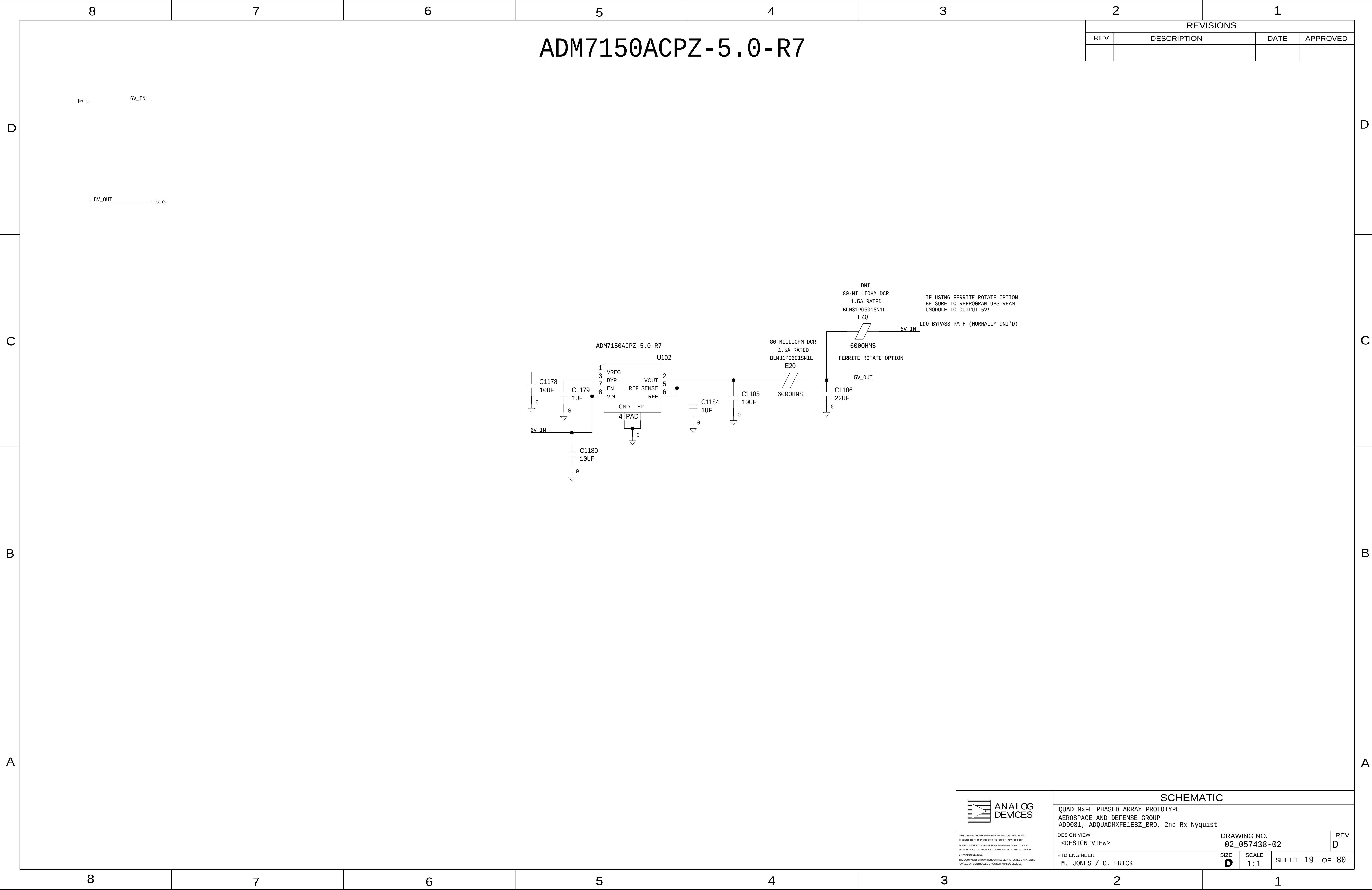
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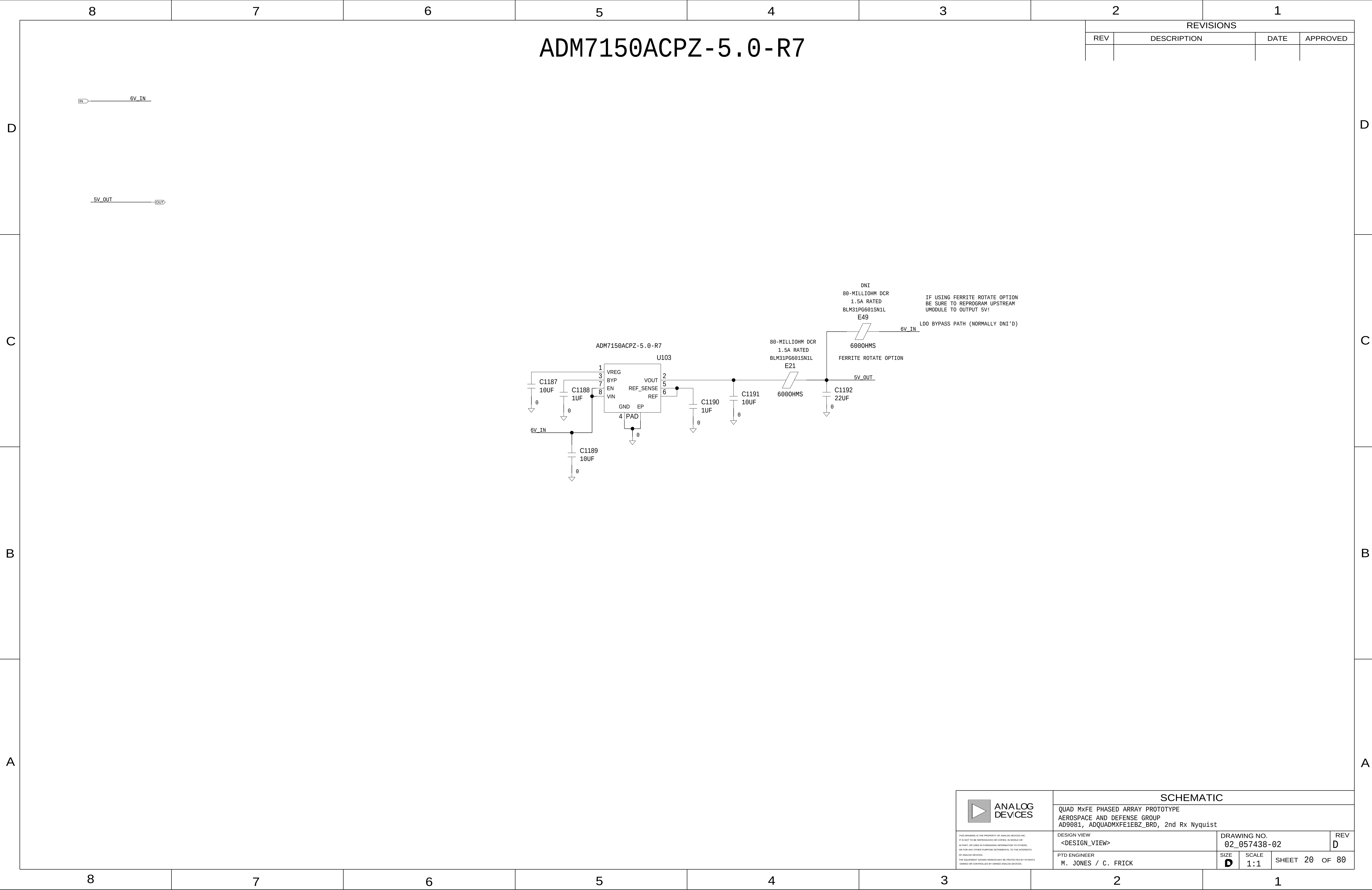
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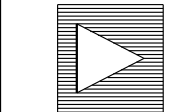




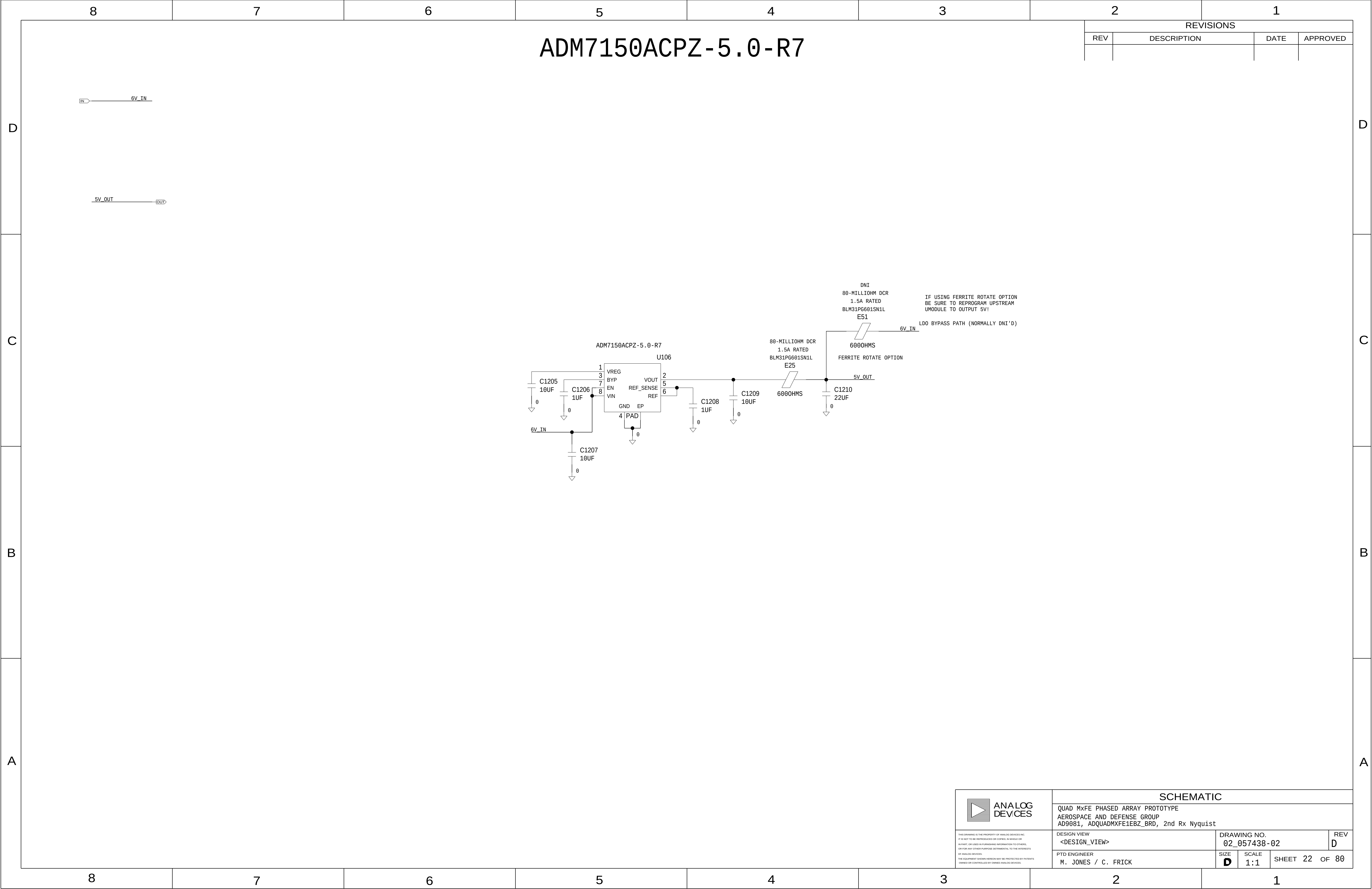




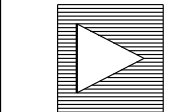
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REV	DESCRIPTION	DATE	APPROVED



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DESIGN VIEW <DESIGN_VIEW>		DRAWING NO. 02_057438-02	REV D
PTD ENGINEER M. JONES / C. FRICK		SIZE D	SCALE 1:1
		SHEET 21	OF 80

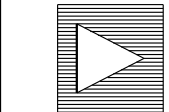


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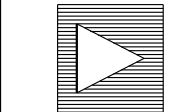
SIZE D	SCALE 1:1	SHEET 23 OF 80
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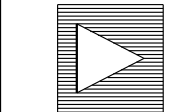
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		SHEET 24	OF 80

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

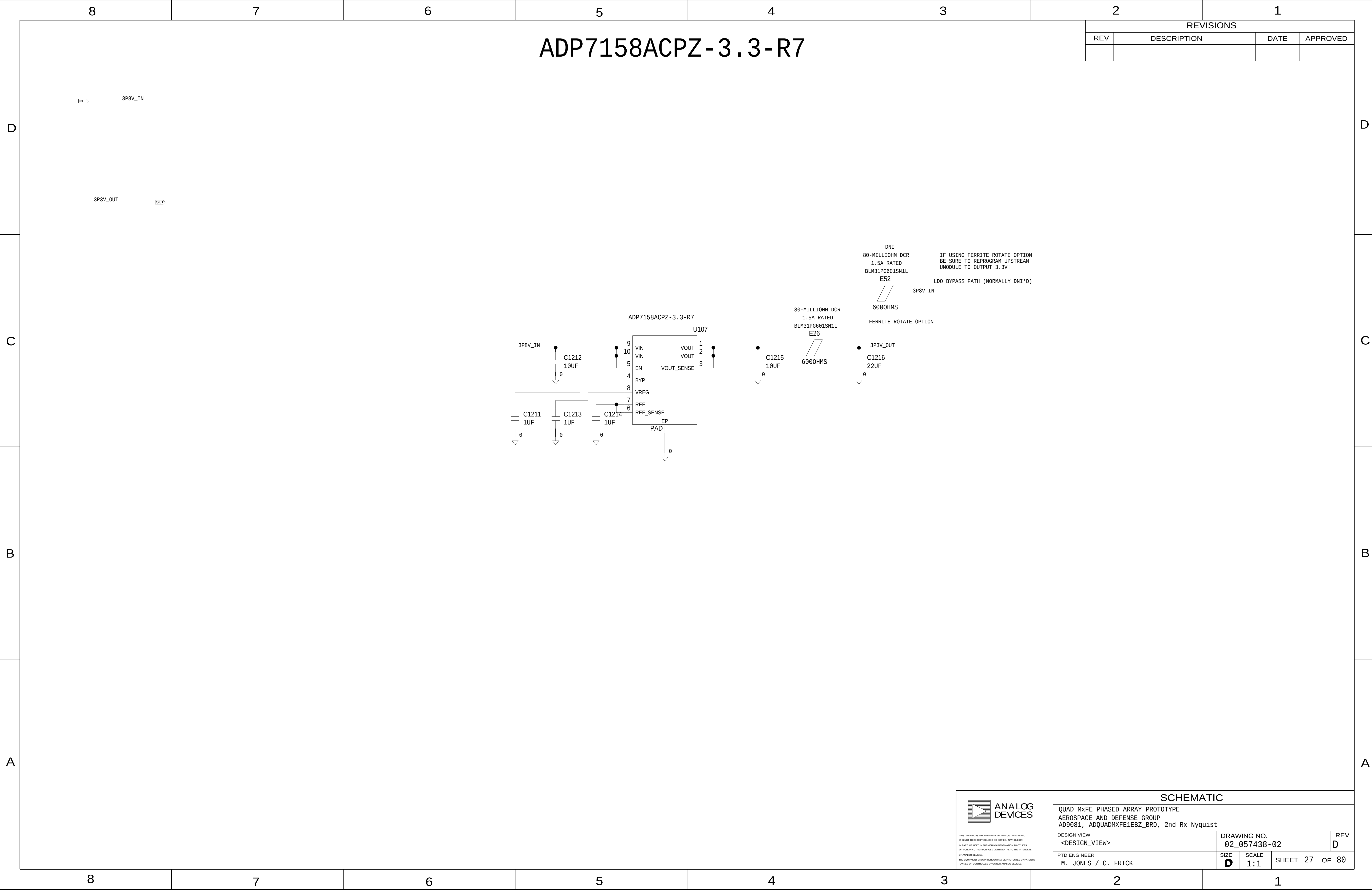


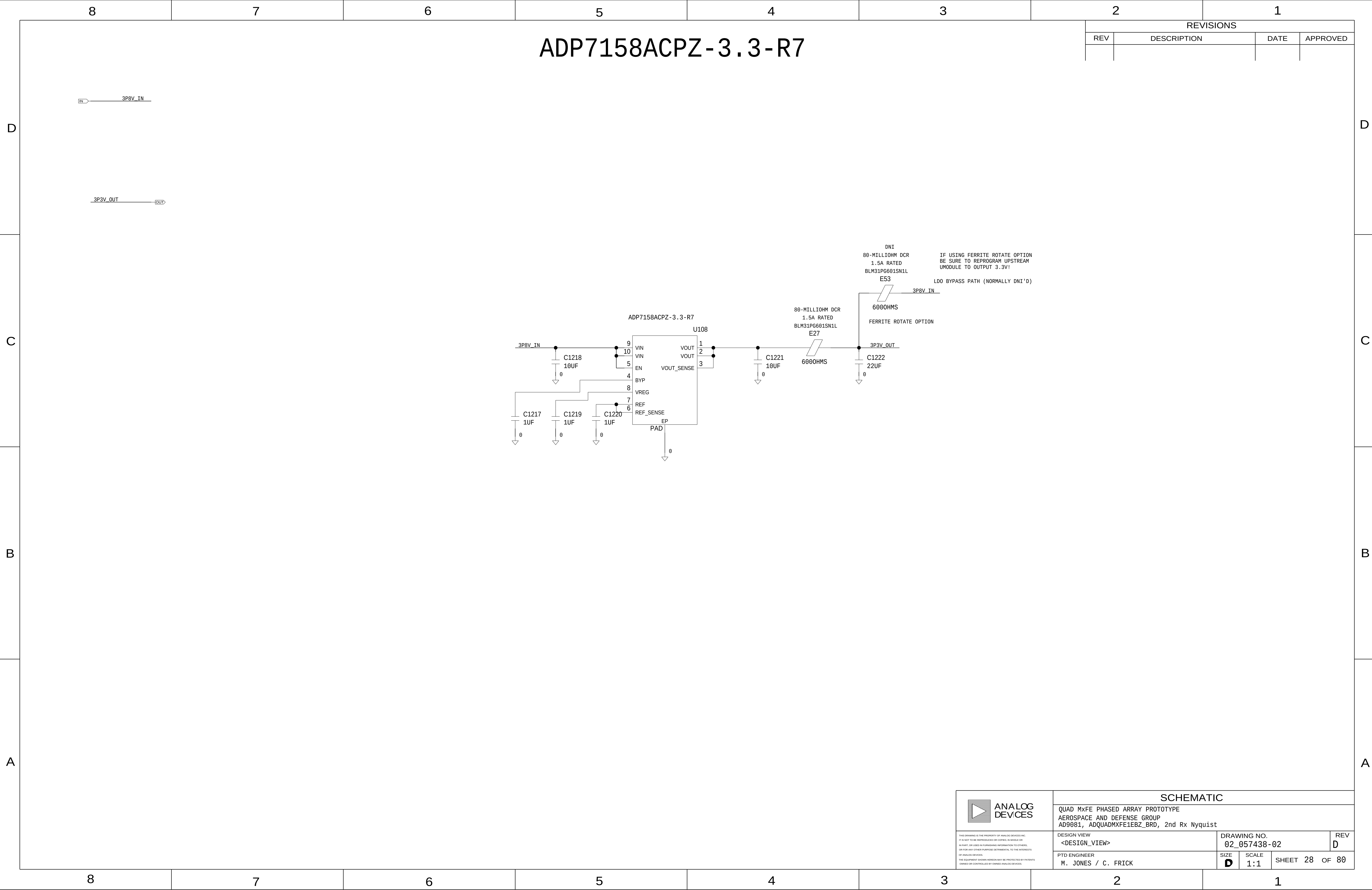
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PTD ENGINEER M. JONES / C. FRICK		SIZE D	SCALE 1:1
		SHEET	25 OF 80

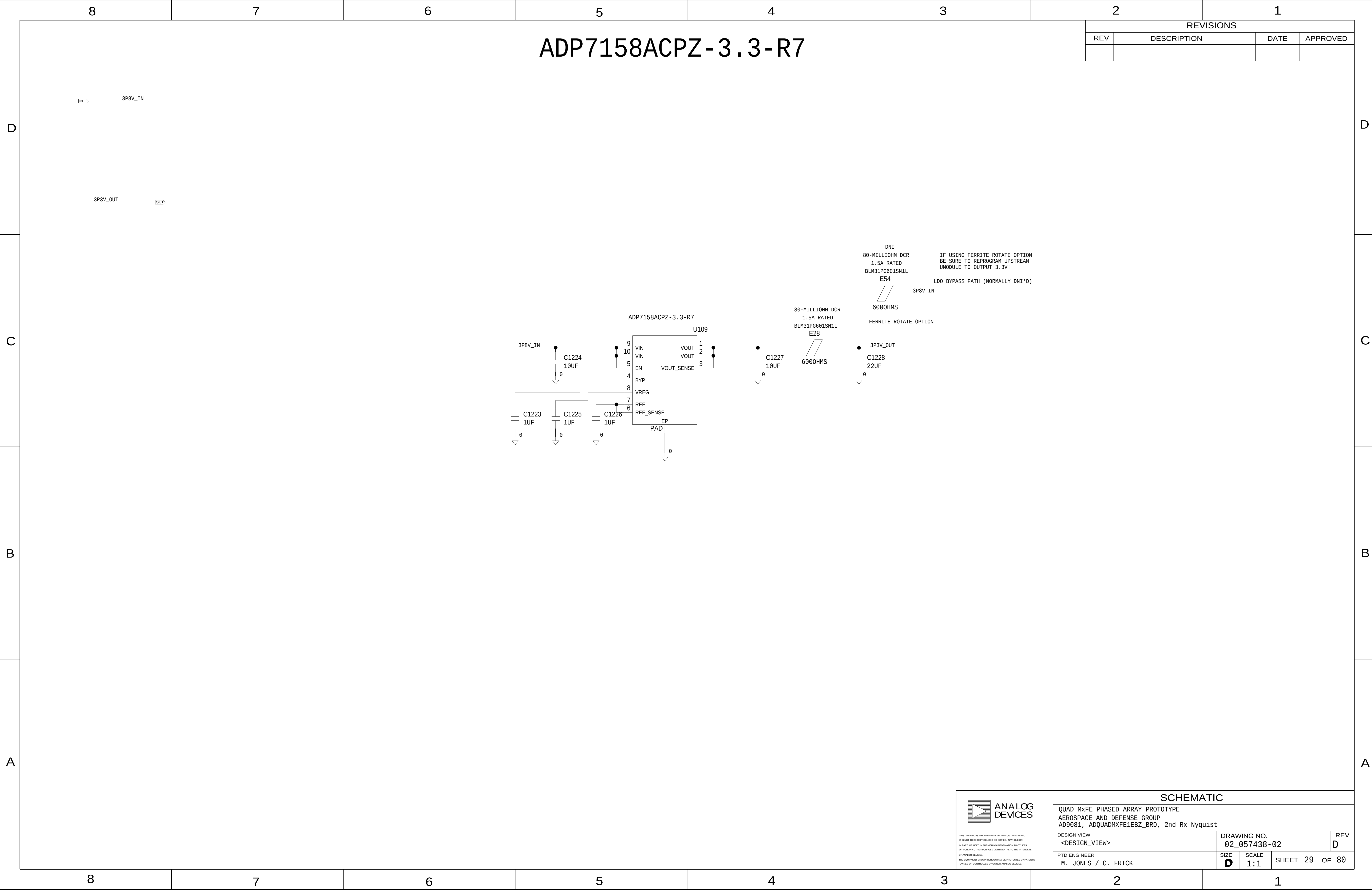
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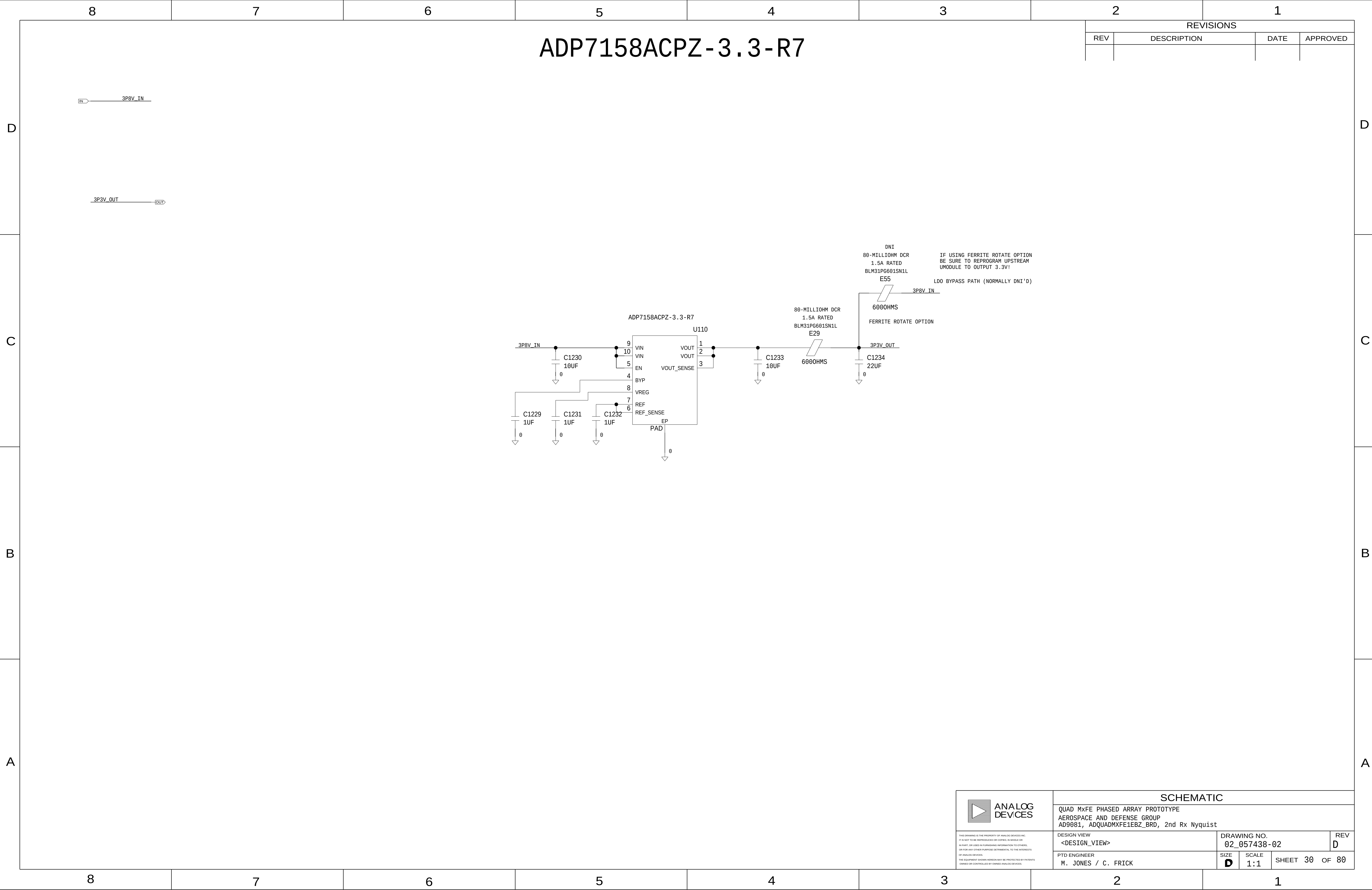


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PTD ENGINEER M. JONES / C. FRICK		SIZE D	SCALE 1:1
		SHEET 26	OF 80



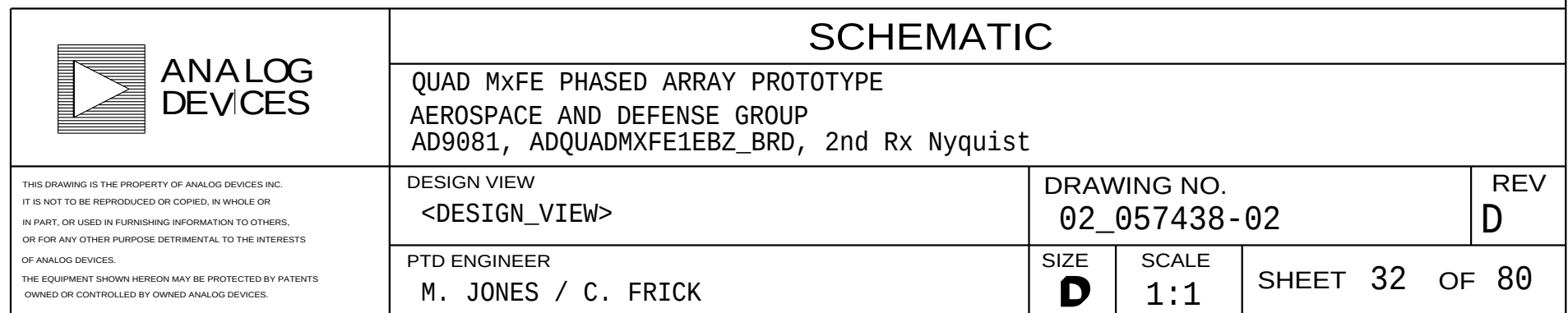


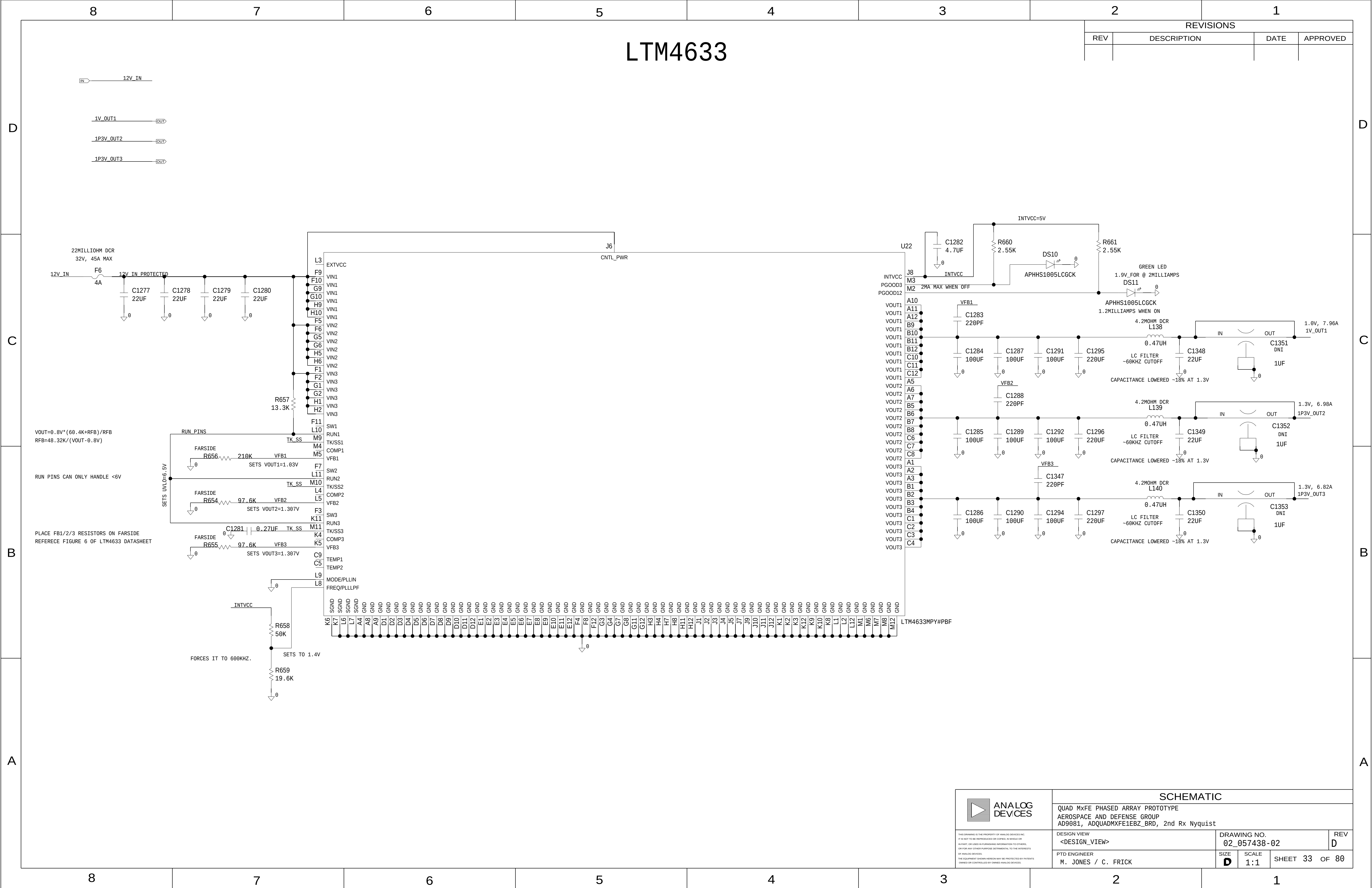




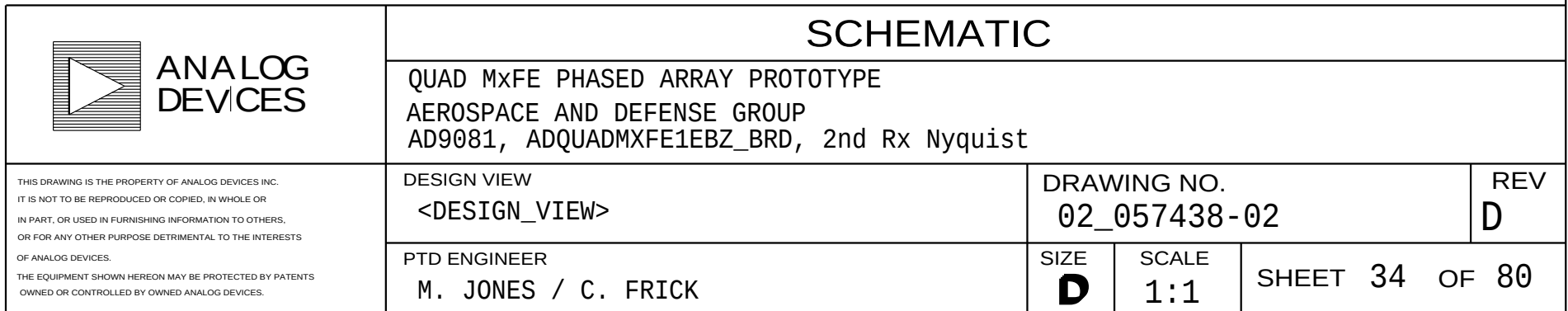
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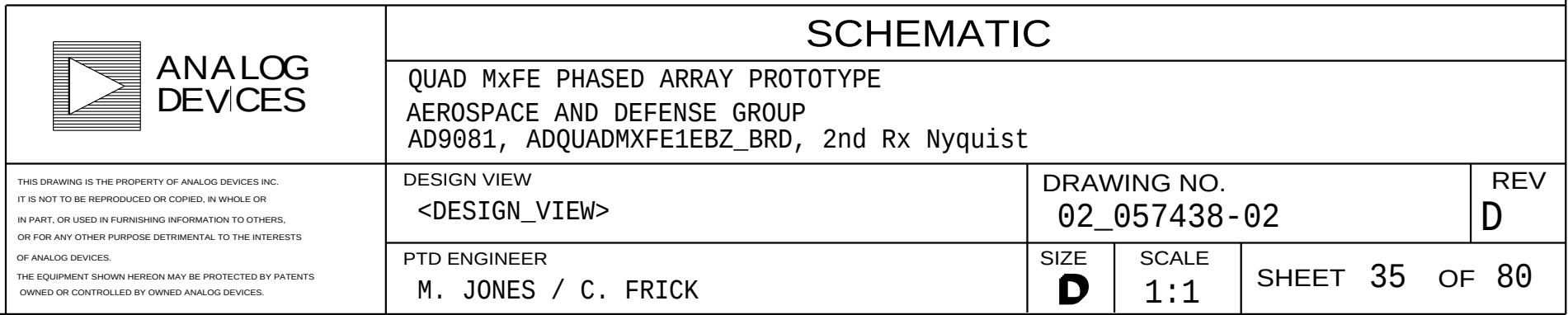




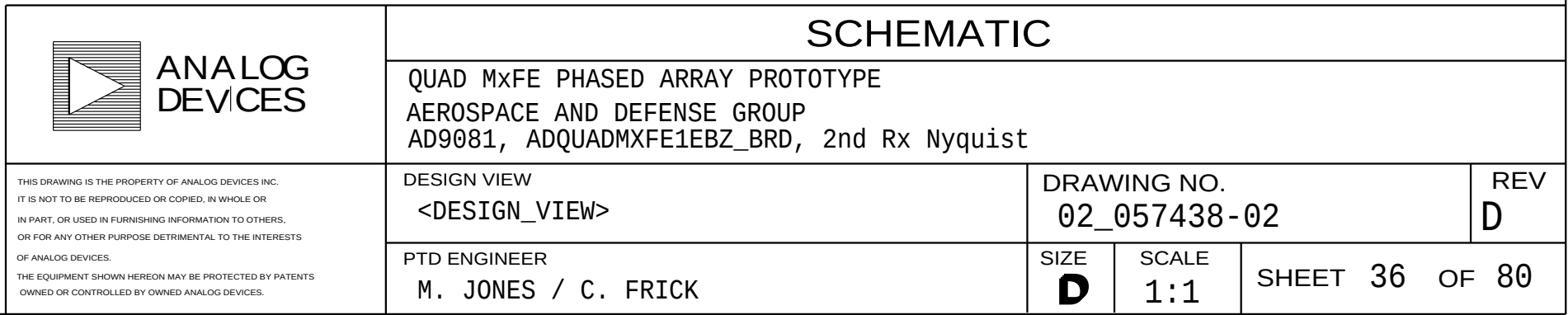
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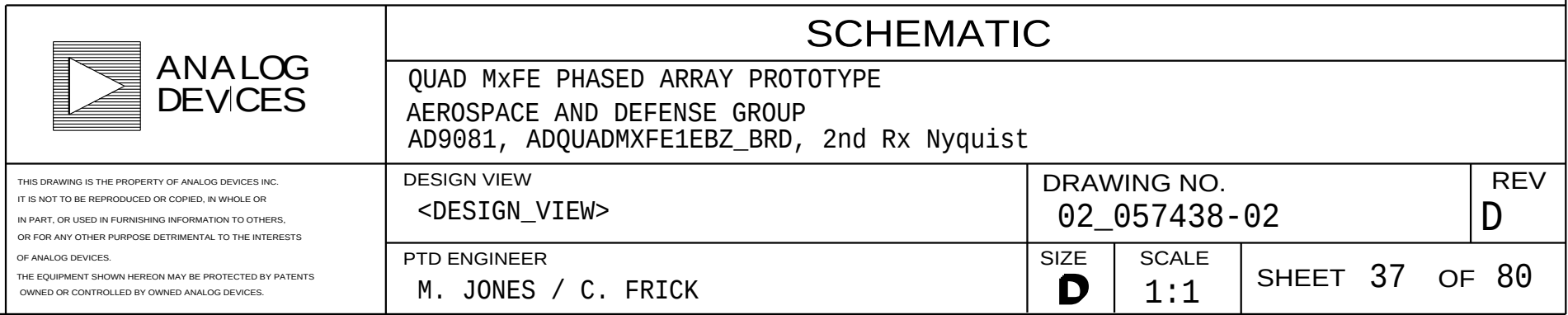
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REV	DESCRIPTION	DATE	APPROVED



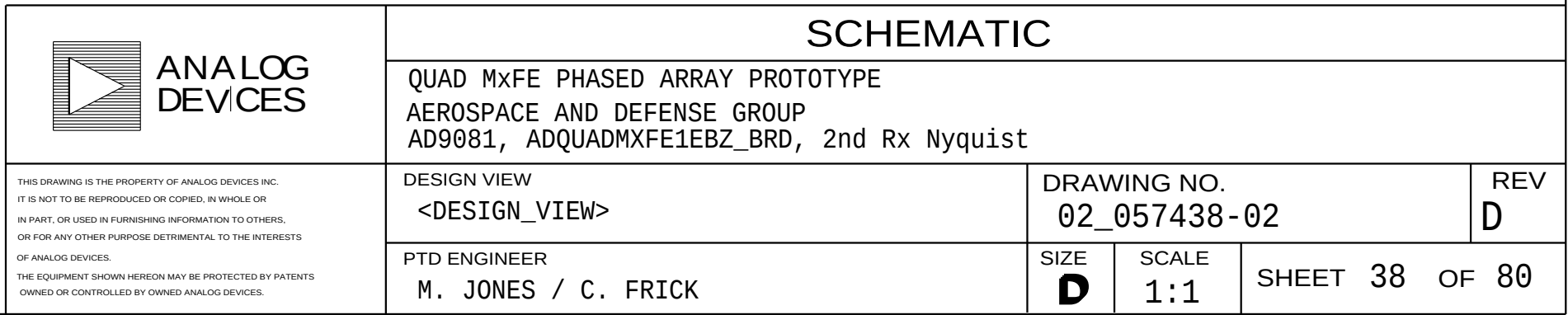
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REV	DESCRIPTION	DATE	APPROVED



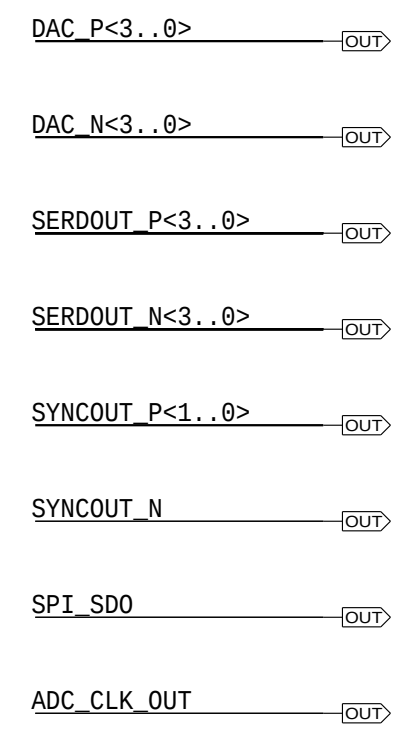
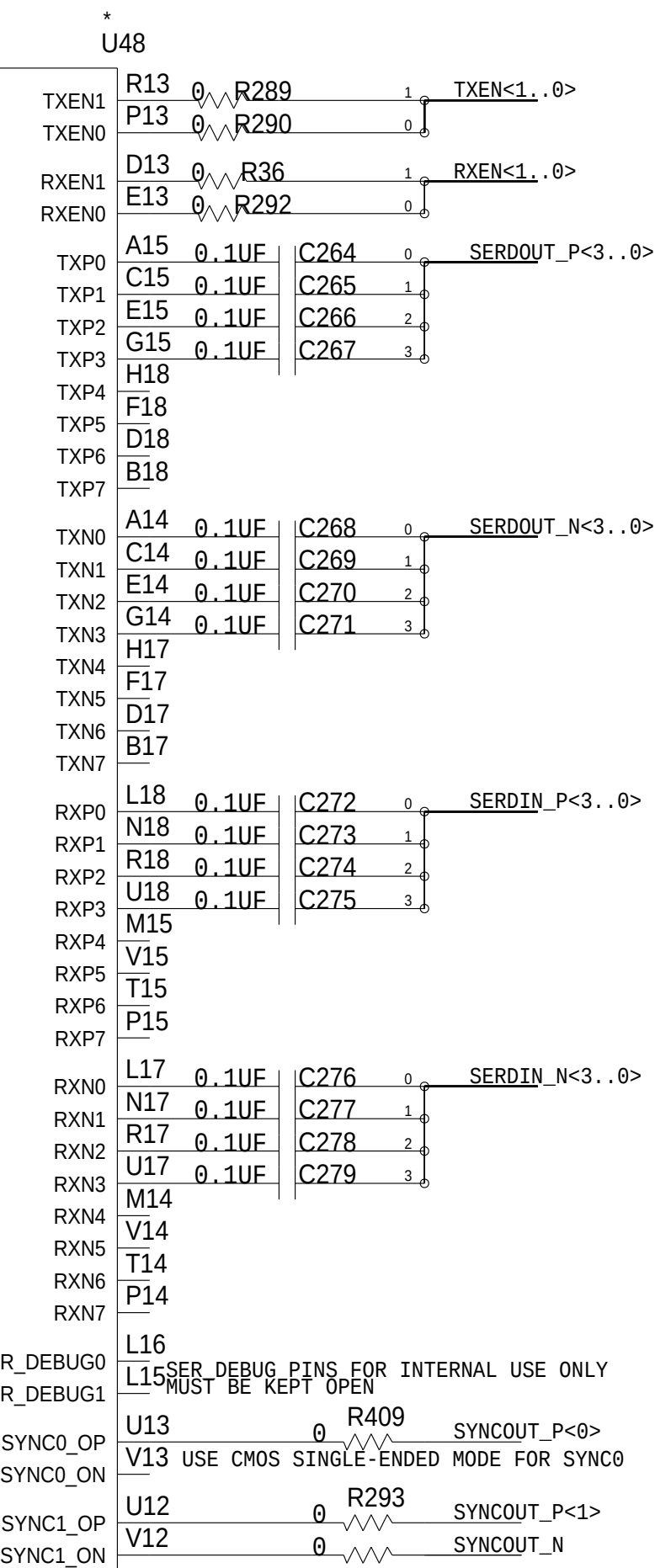
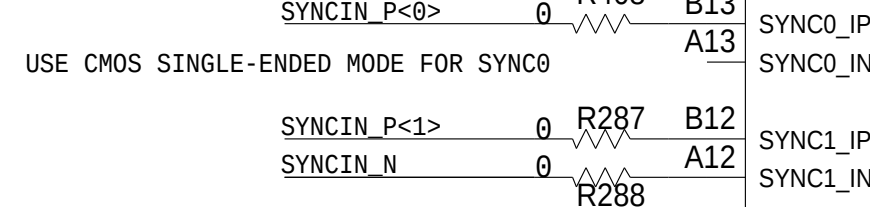
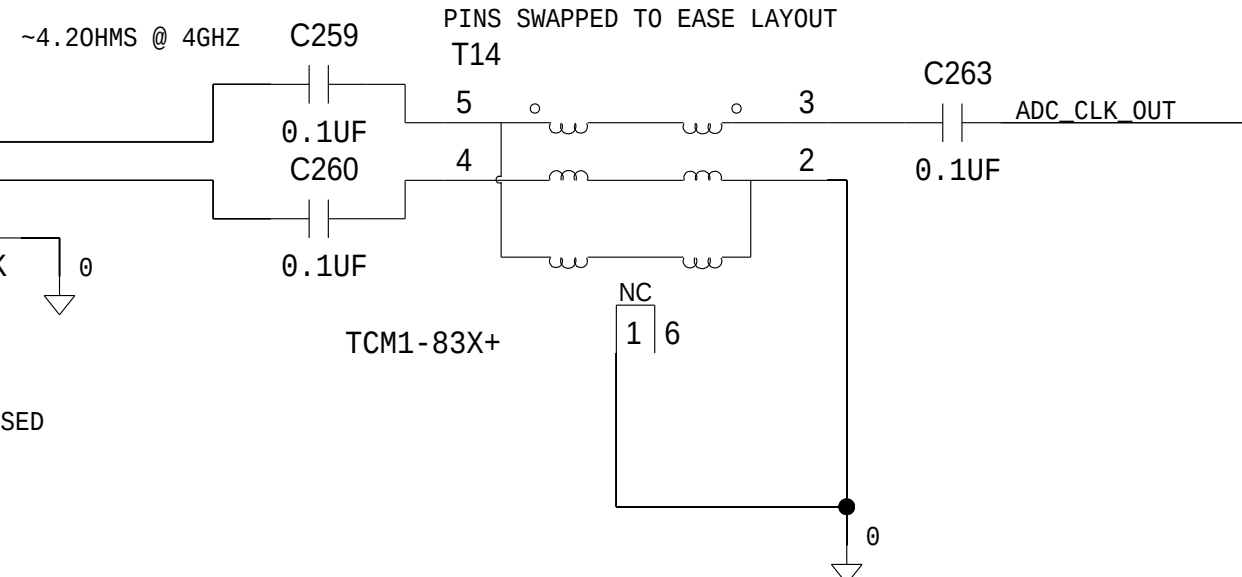
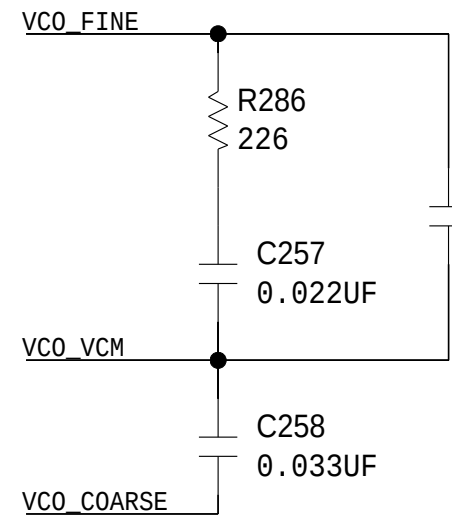
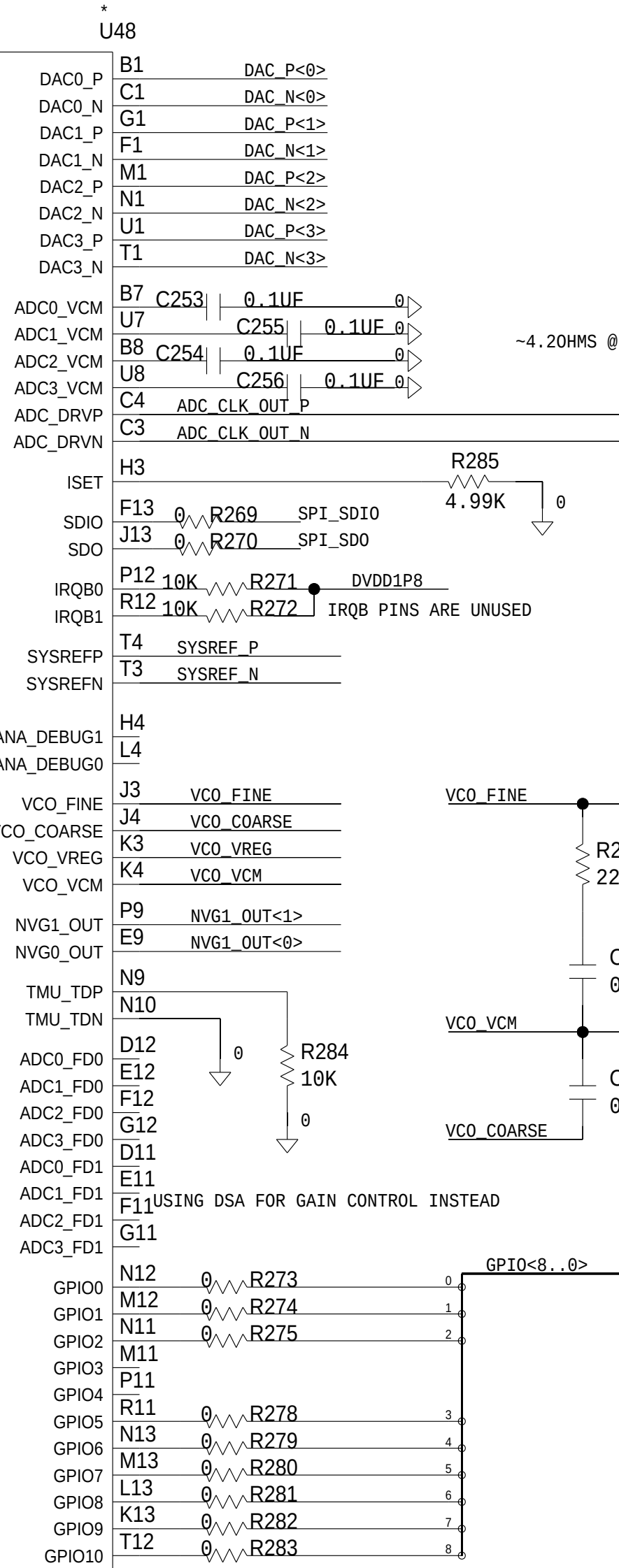
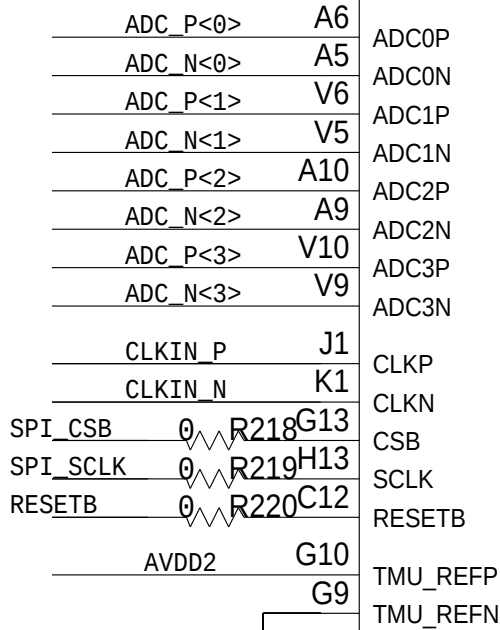
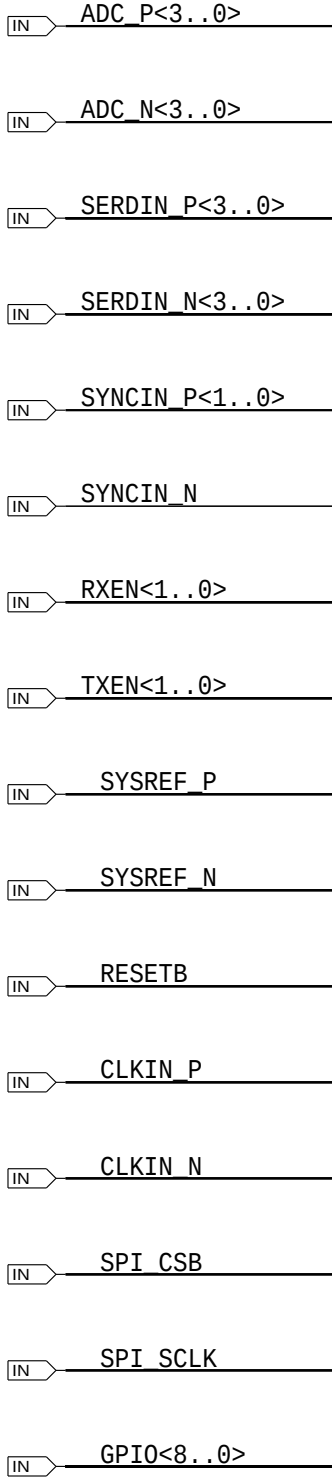
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REV	DESCRIPTION	DATE	APPROVED

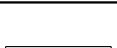




MXFE INPUT / OUTPUT

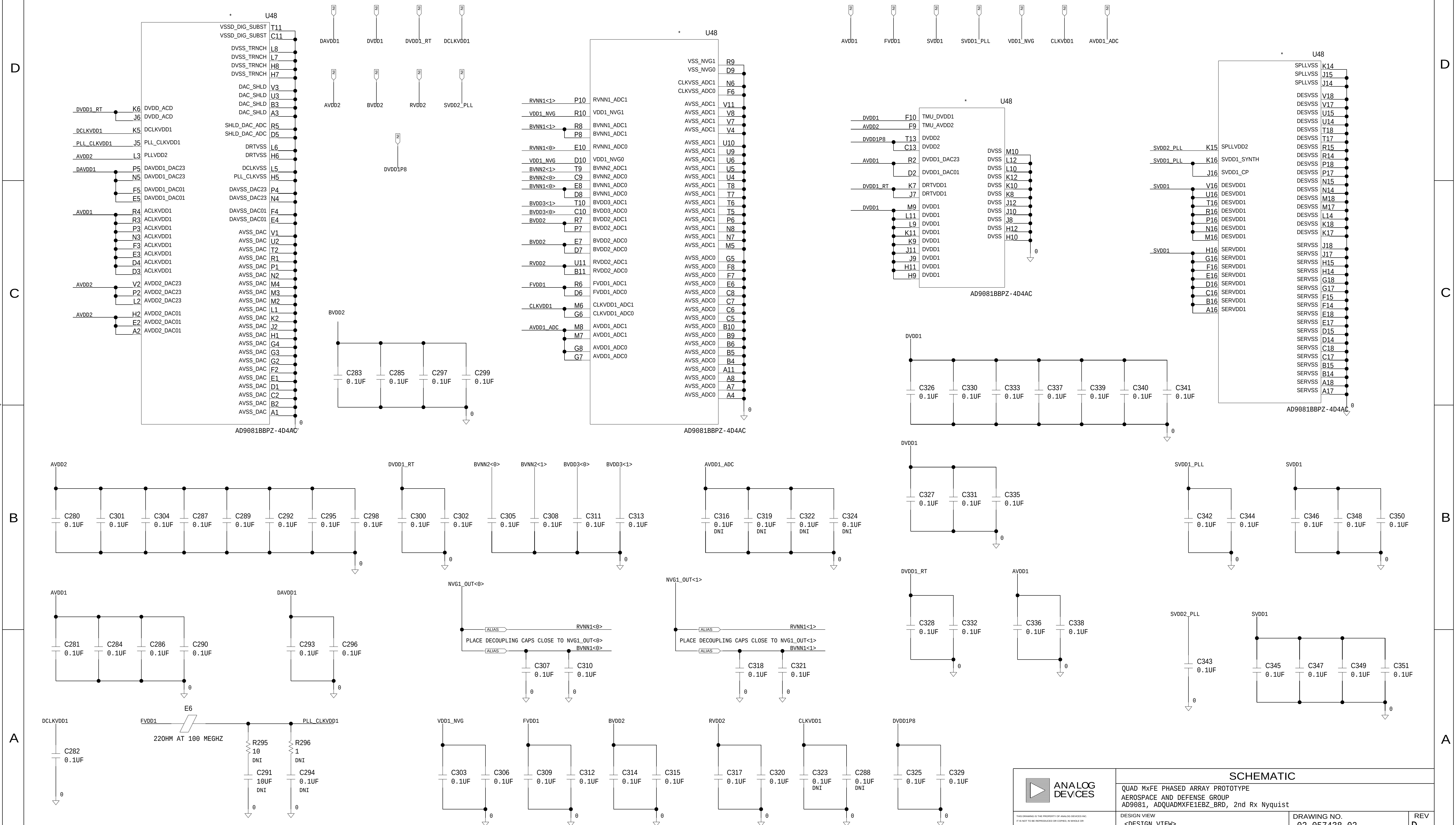
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



 ANALOG DEVICES	SCHEMATIC			
	QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9081, ADQUADMxFE1EBZ_BRD, 2nd Rx Nyquist			
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PTD ENGINEER M. JONES / J. C. FRICK	SIZE D	SCALE 1:1	SHEET 41 OF 80	

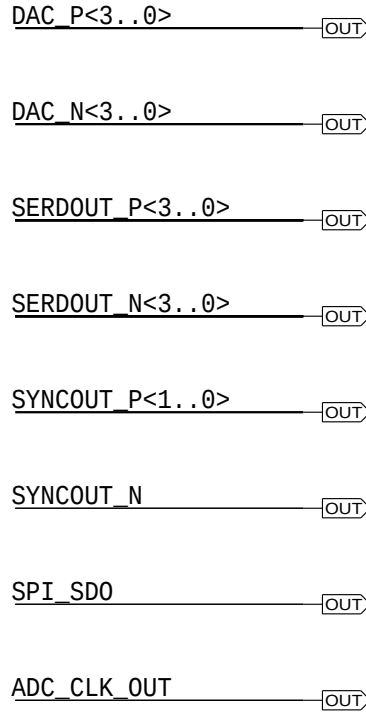
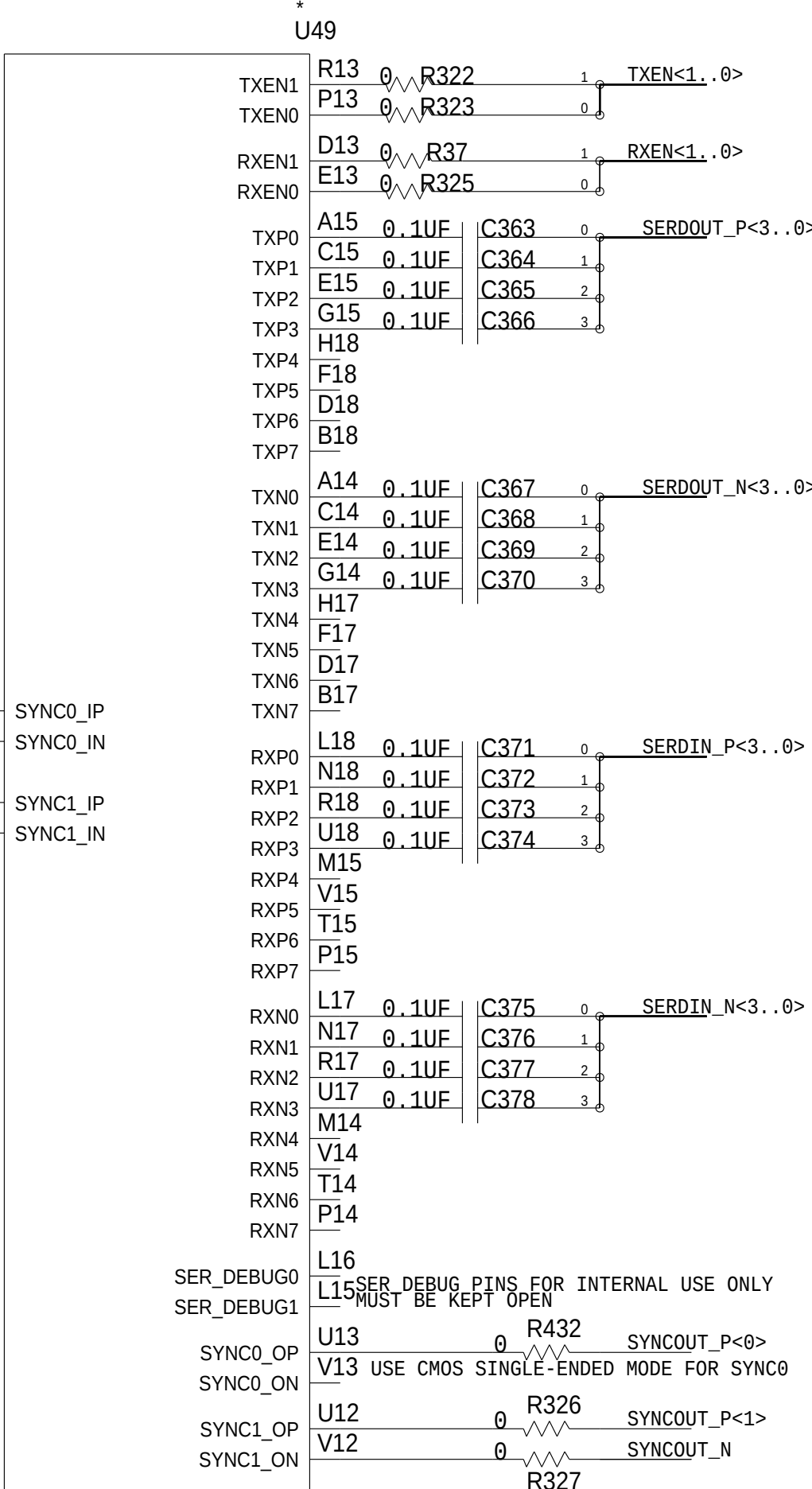
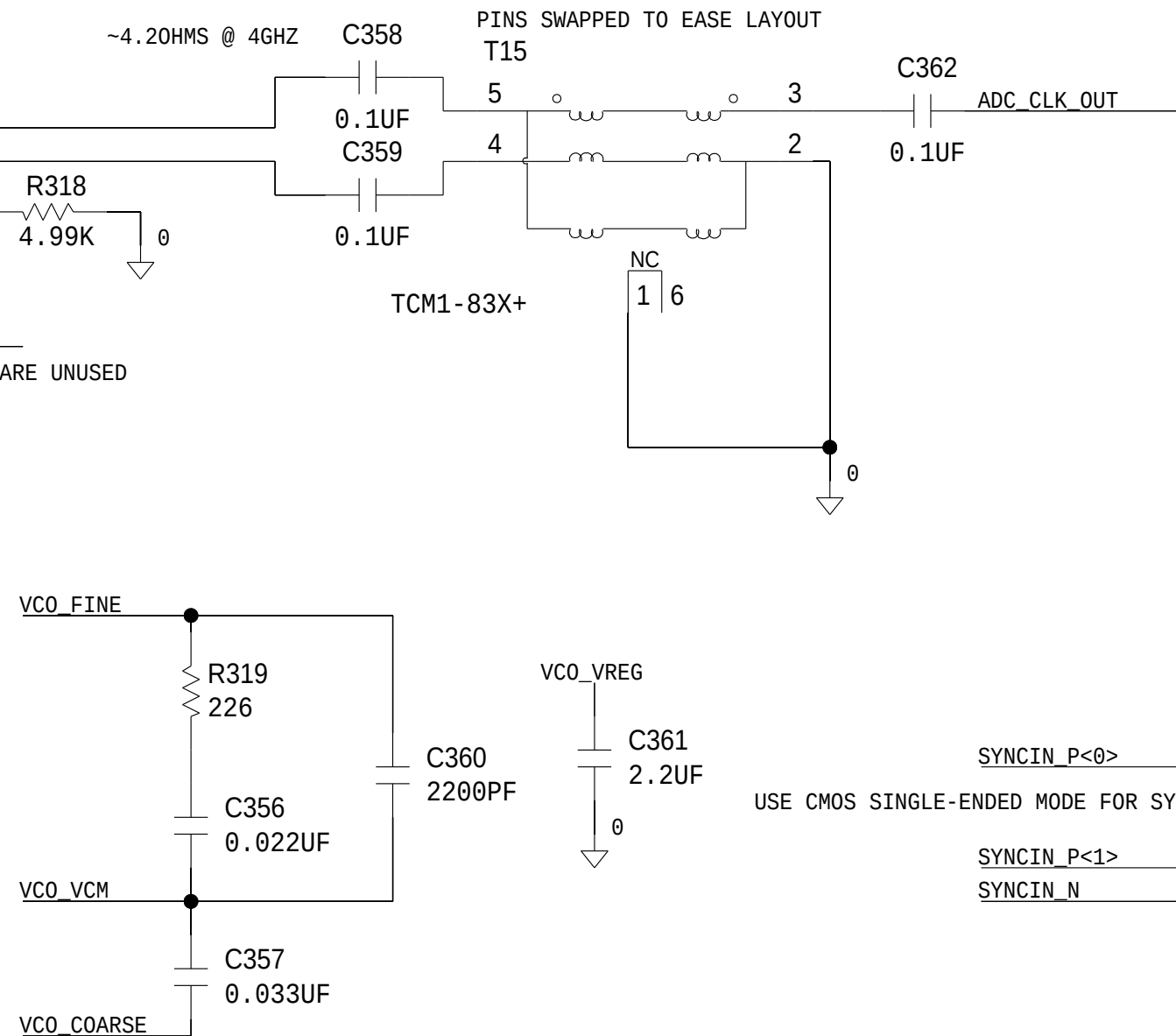
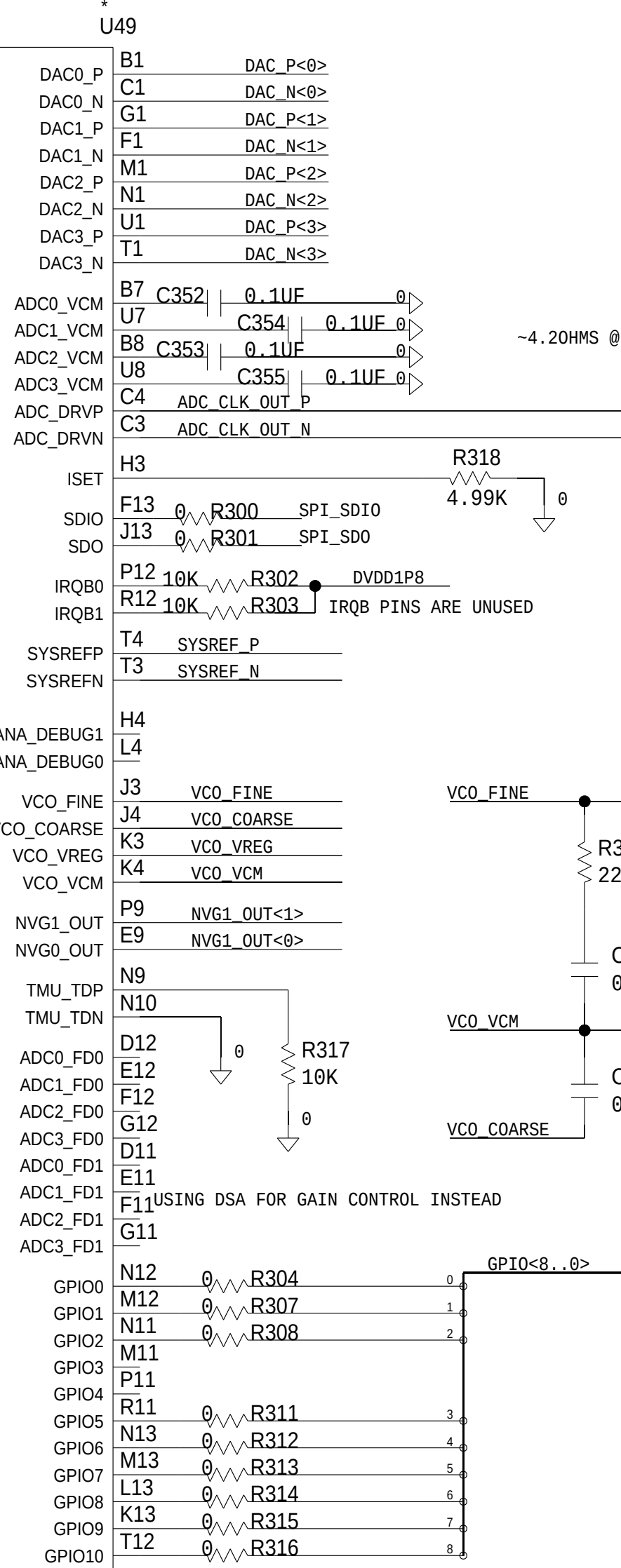
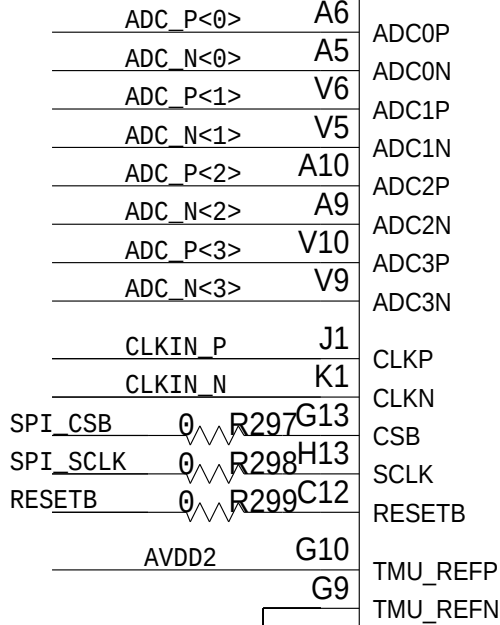
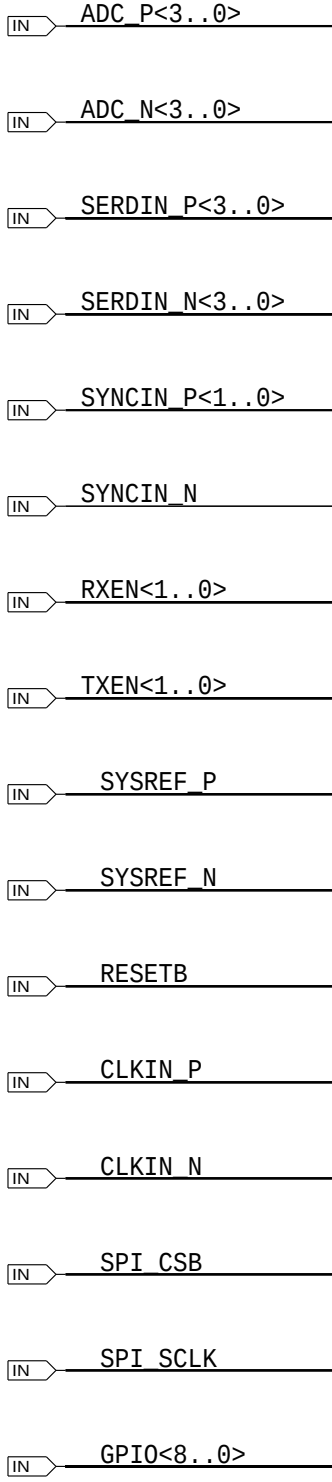
MXFE SUPPLIES

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REV	DESCRIPTION	DATE	APPROVED



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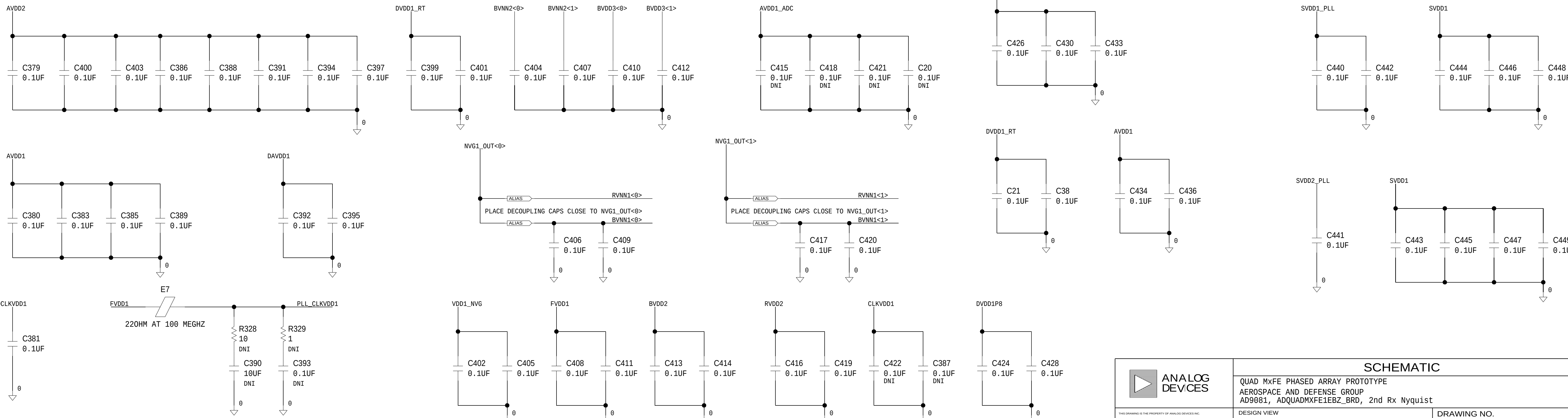
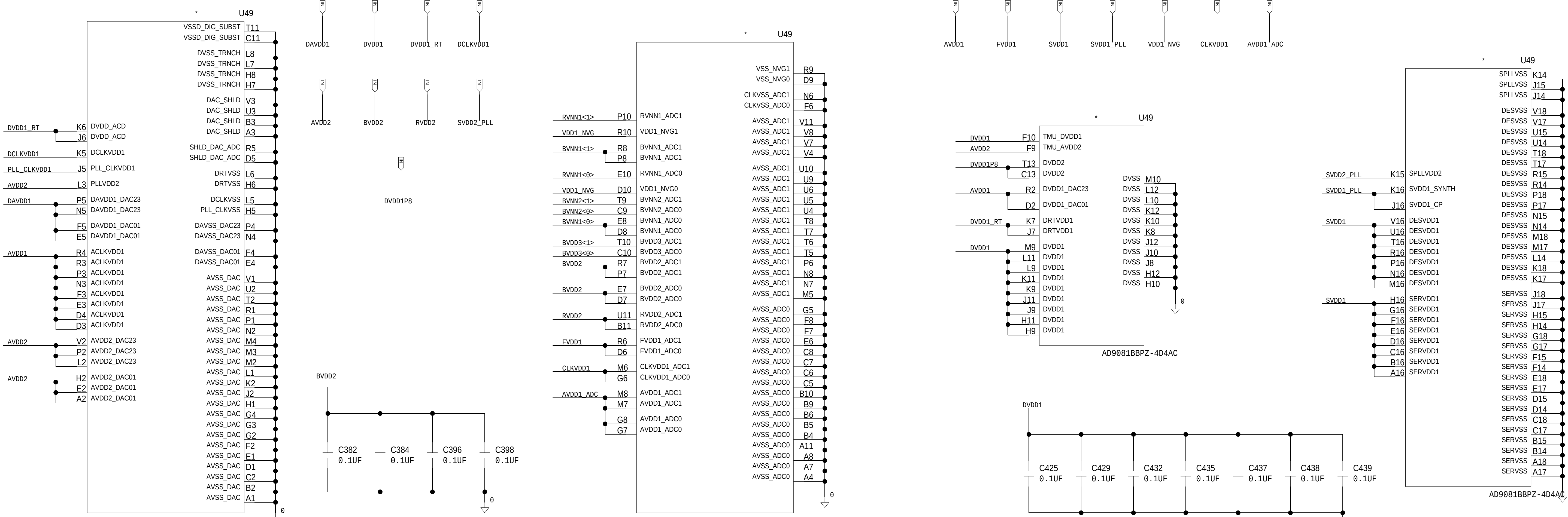
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



 ANALOG DEVICES	SCHEMATIC			
	QUAD MxFe PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9081, ADQUADMxFe1EBZ_BRD, 2nd Rx Nyquist			
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THE EXPANDED/REMOVED AREAS MAY BE CONTROLLED BY PATENTS NAMES DESCRIBED/CONTROLLED BY OWNED ANALOG DEVICES	PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 43 OF 80

MXFE SUPPLIES

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



 ANALOG DEVICES	SCHEMATIC				
	QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9081, ADQUAMXFE1EBZ_BRD, 2nd Rx Nyquist				
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PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 44 OF 80		

MXFE INPUT / OUTPUT

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

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DAC_N<3..0> OUT

SERDOUT_P<3..0> OUT

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SYNCOUT_N OUT

SPI_SD0 OUT

ADC_CLK_OUT OUT

D

D

C

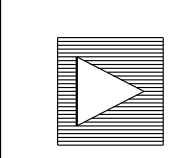
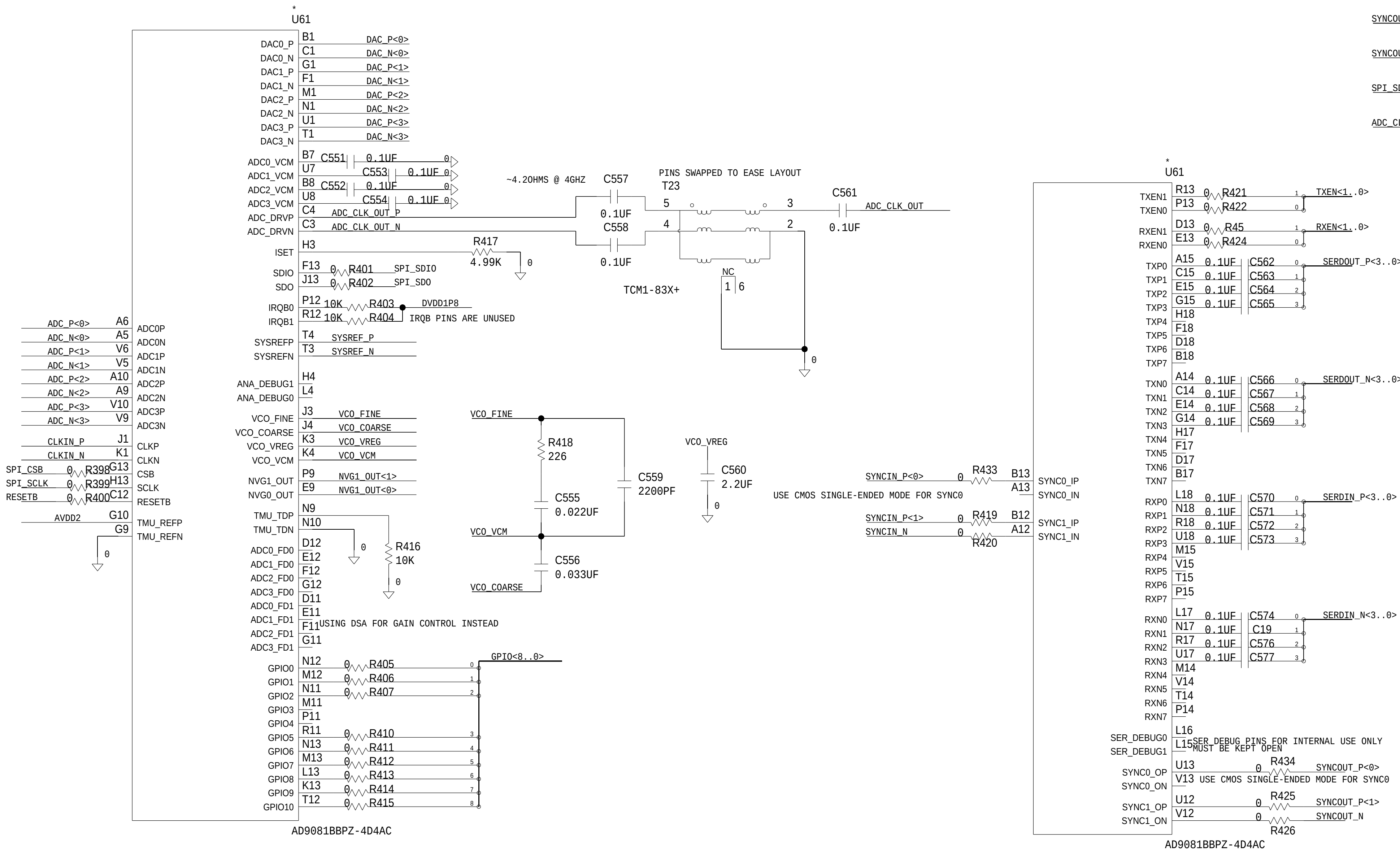
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B

B

A

A



ANALOG
DEVICES

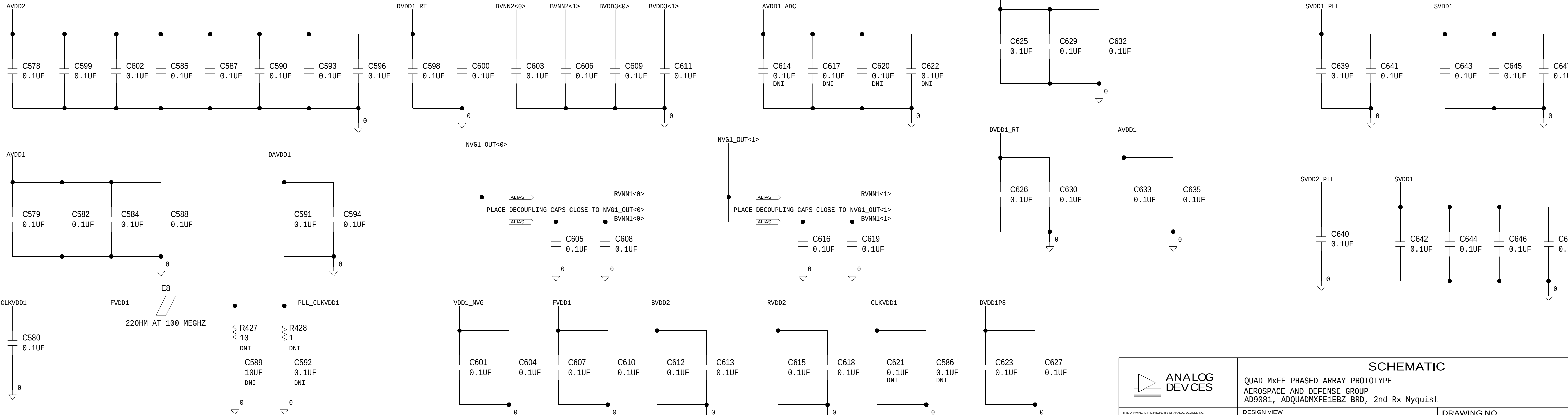
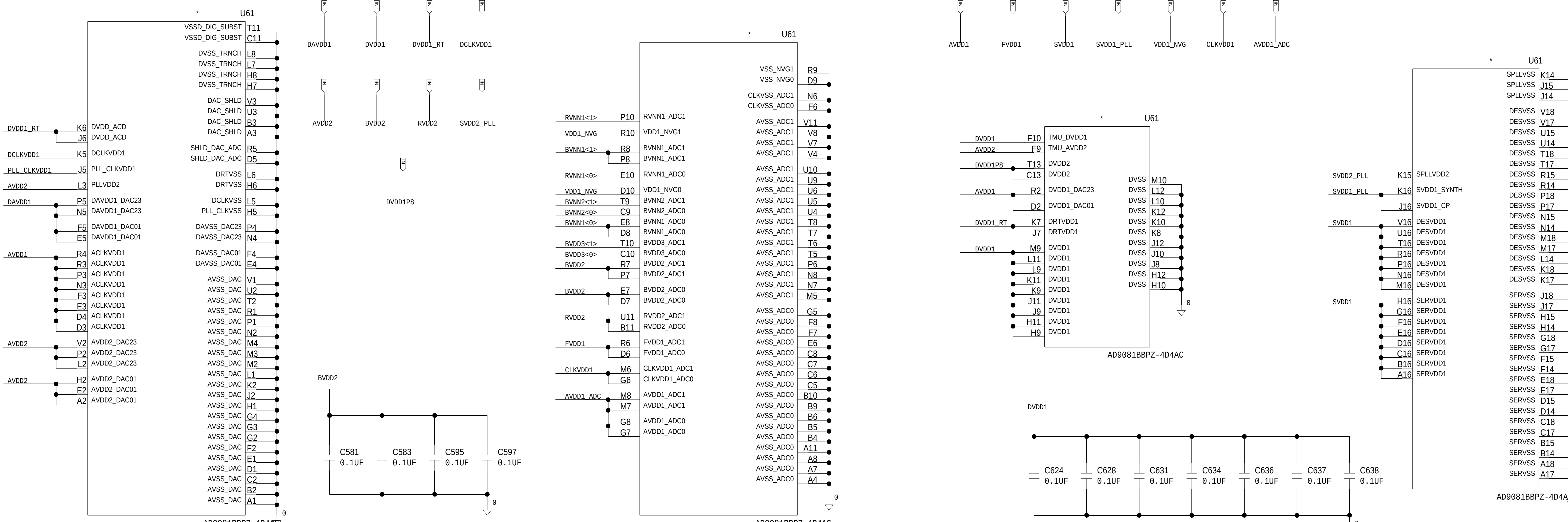
SCHEMATIC

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9081, ADQUADMxFE1EBZ_BRD, 2nd Rx Nyquist

DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_057438-02	REV D
PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1
SHEET 45 OF 80		

MXFE SUPPLIES

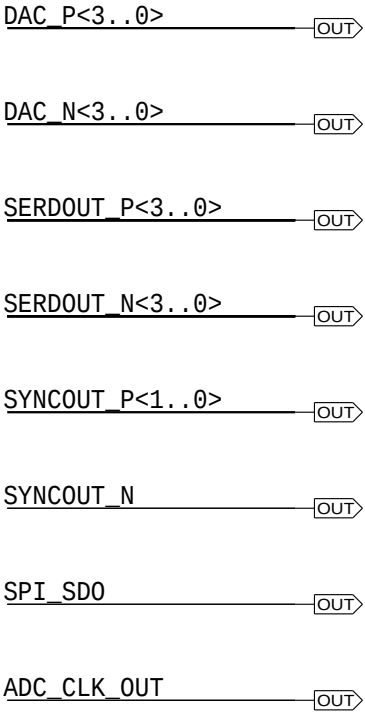
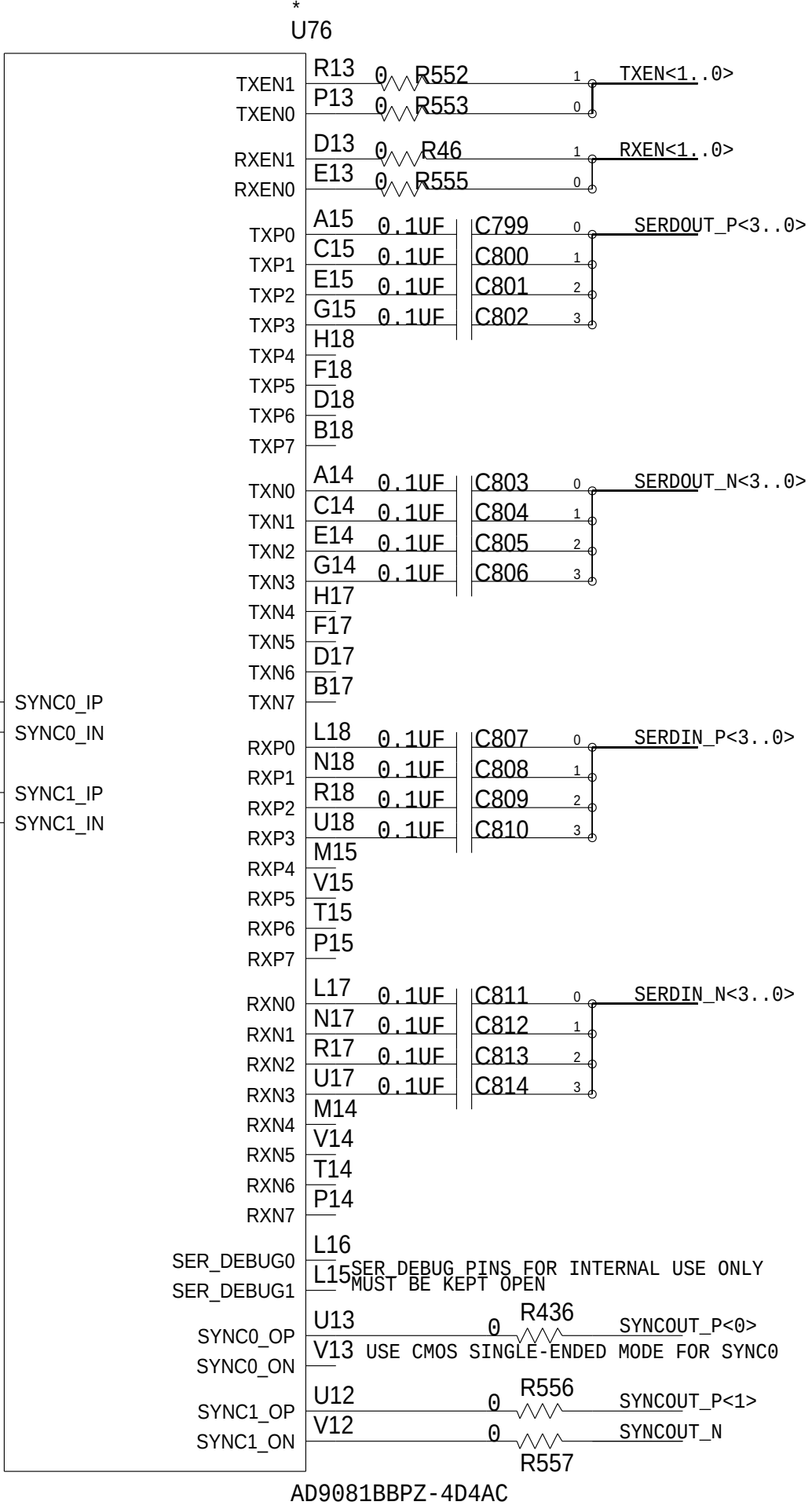
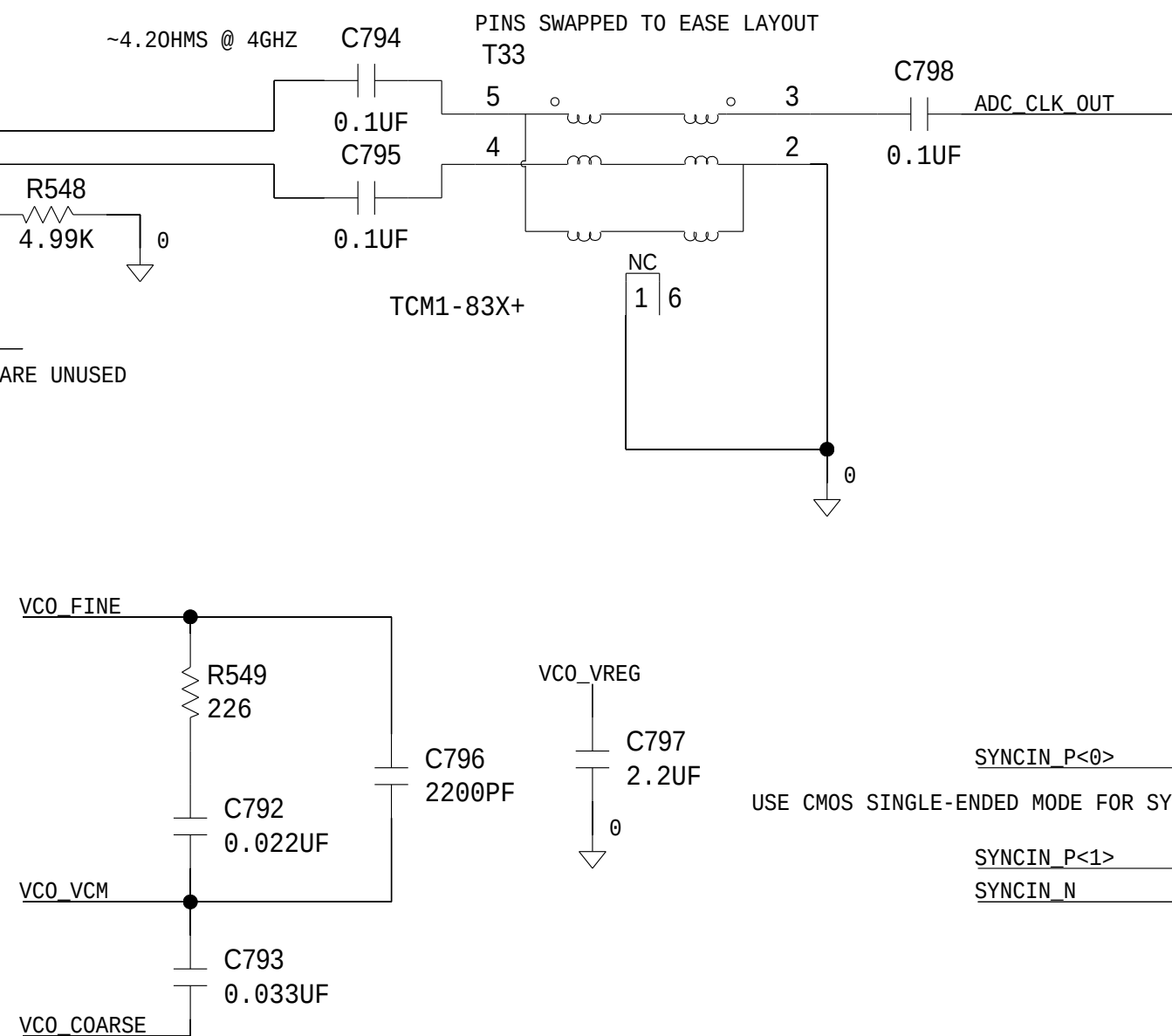
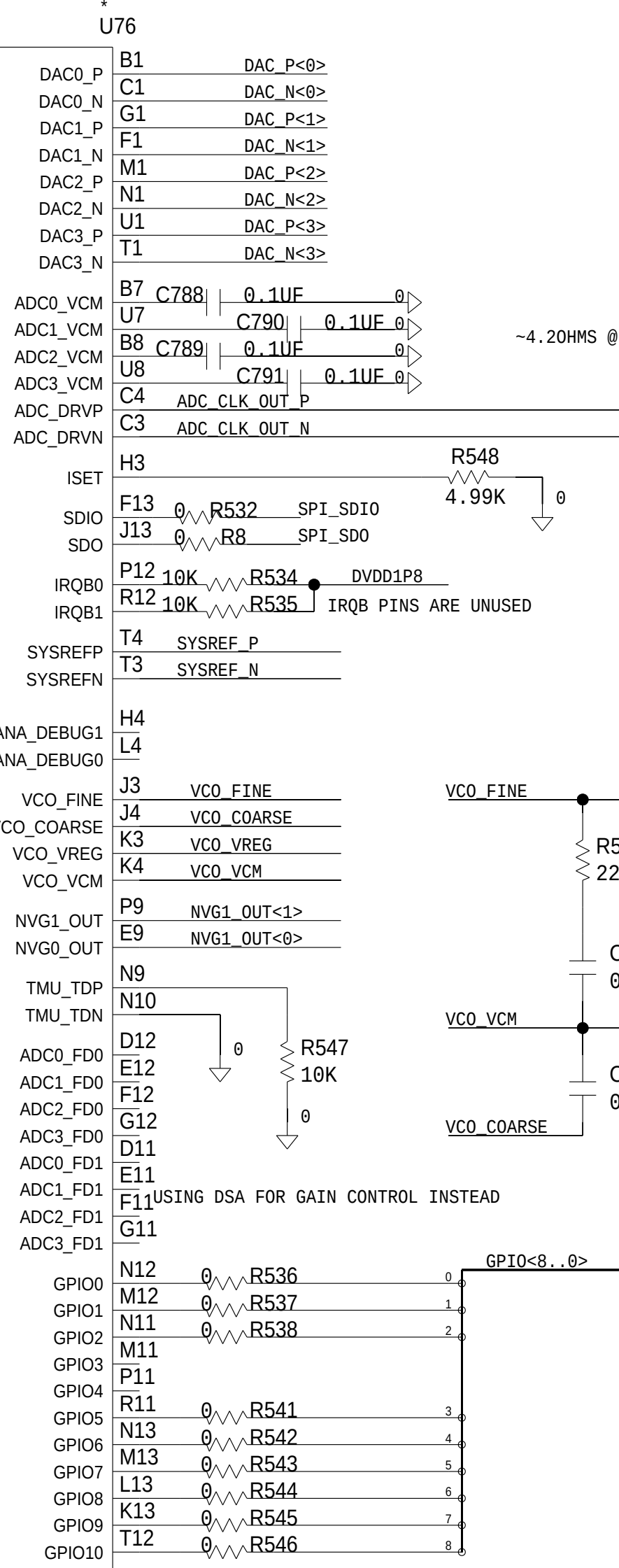
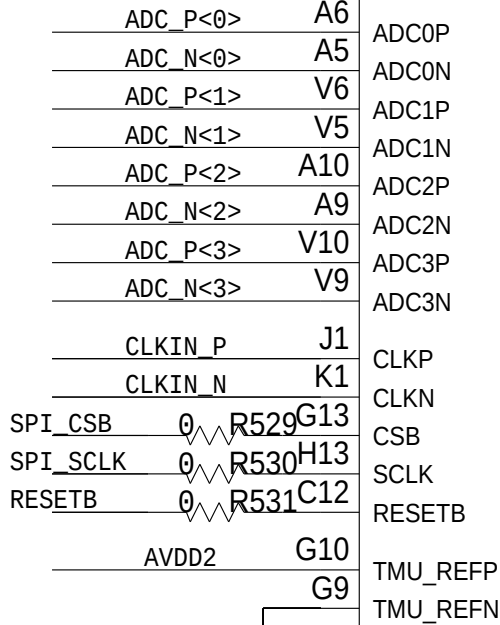
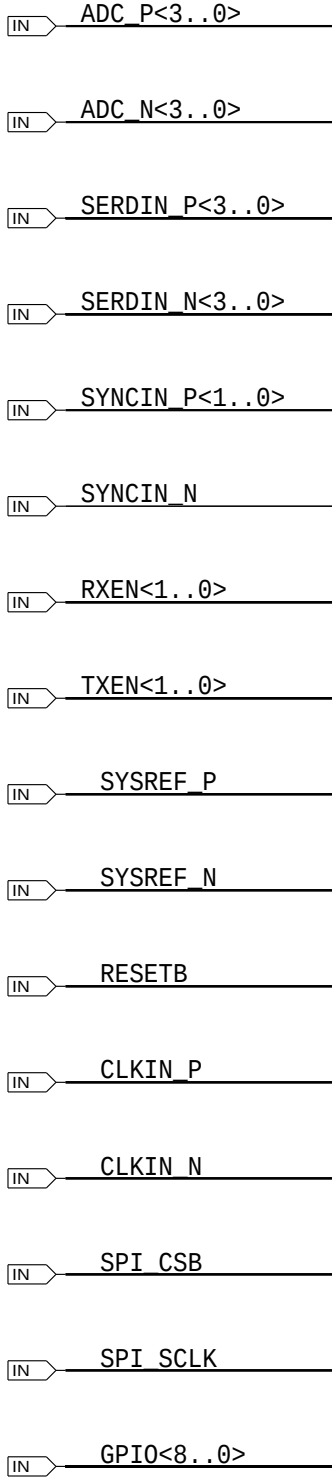
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



 ANALOG DEVICES	SCHEMATIC			
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PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 46 OF 80	

MXFE INPUT / OUTPUT

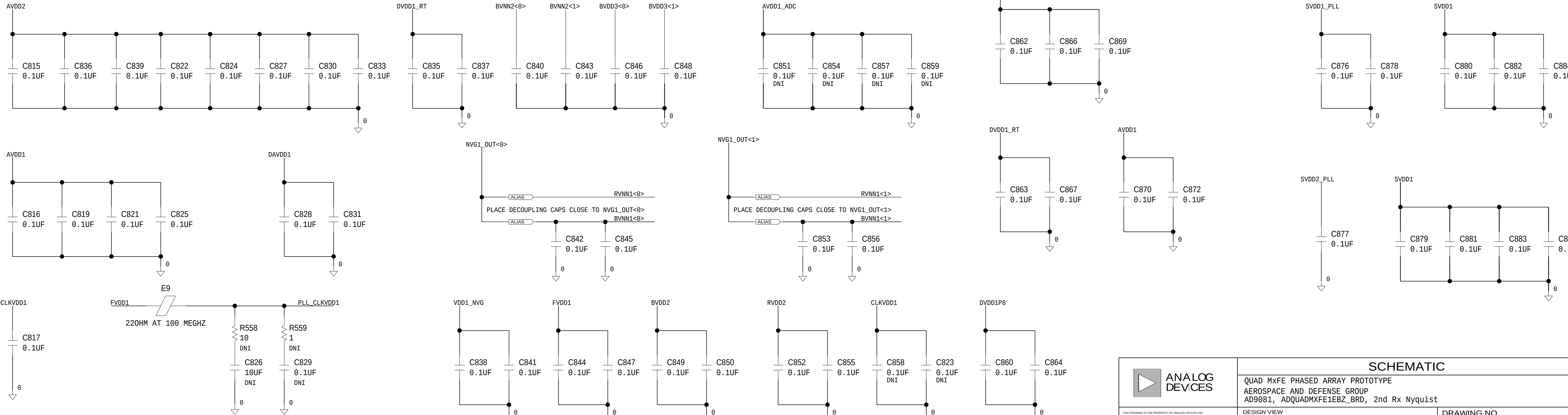
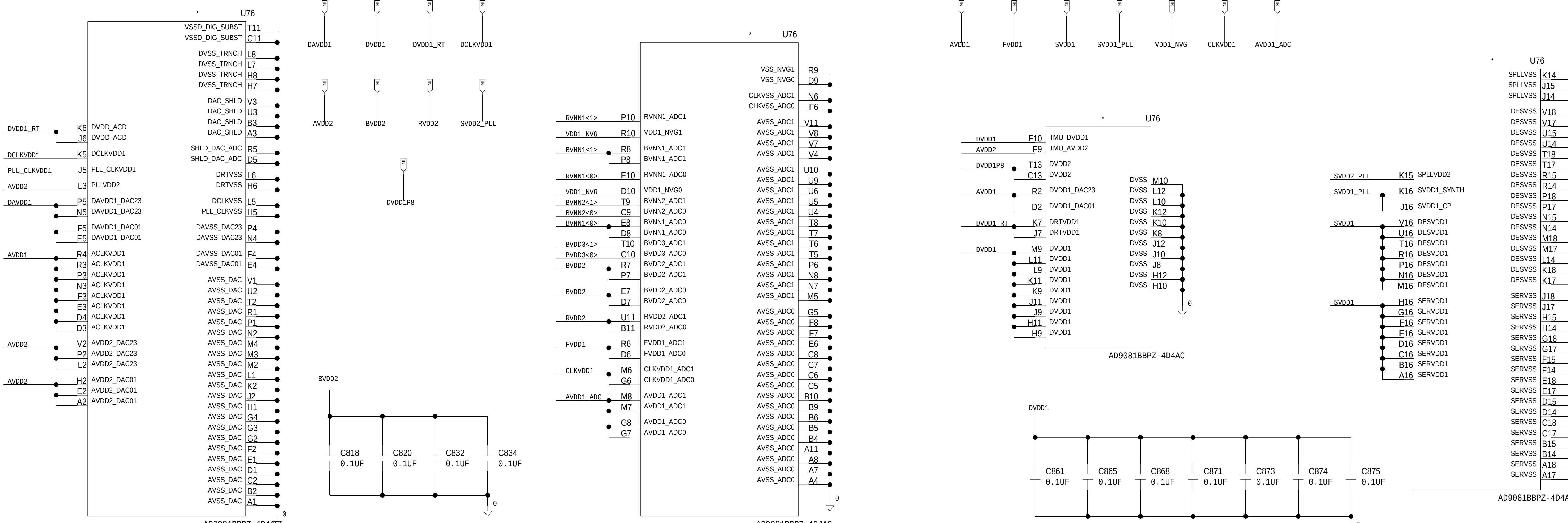
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REV	DESCRIPTION	DATE	APPROVED



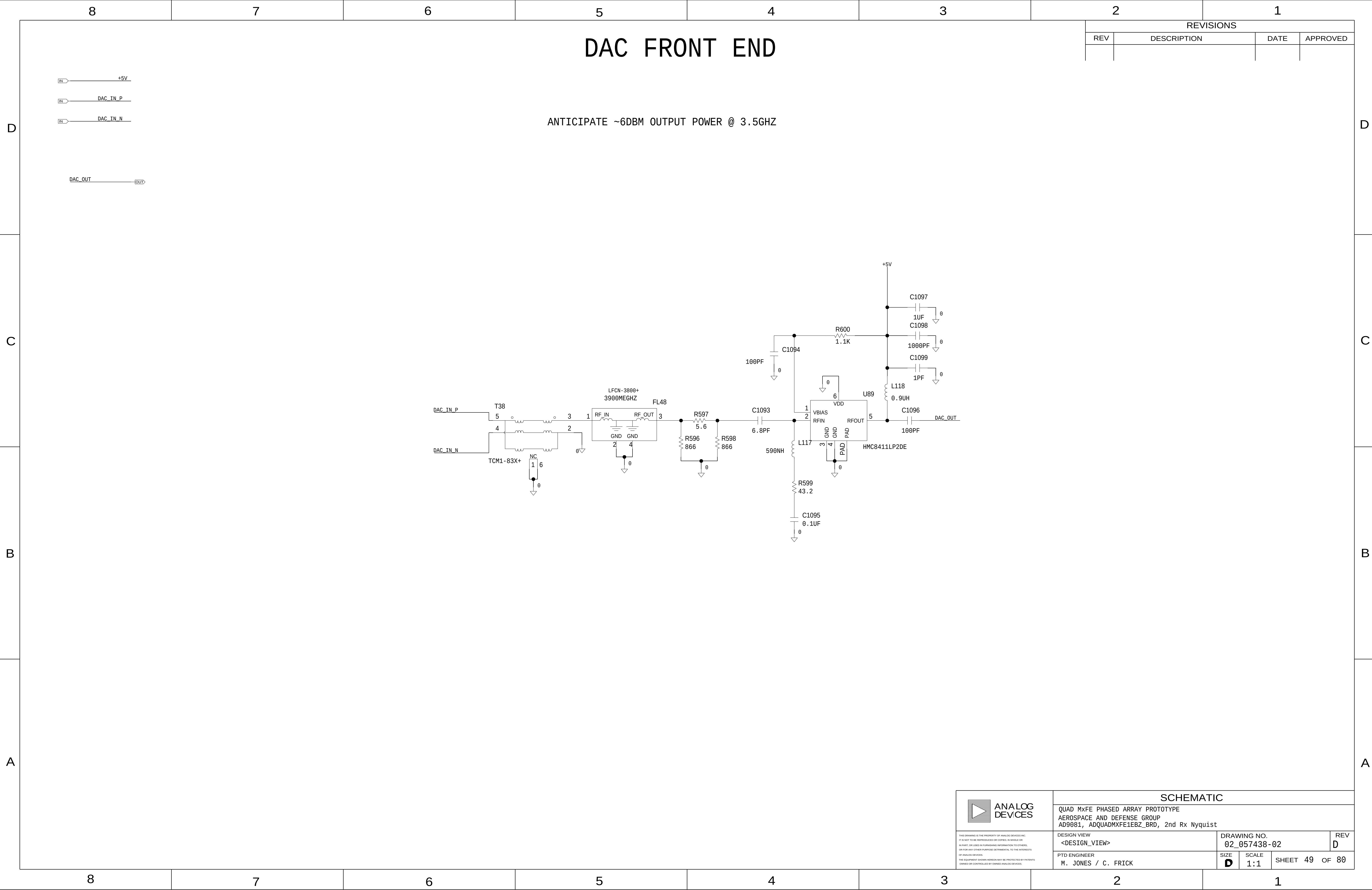
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	QUAD MxFe PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9081, ADQUAMXFE1EBZ_BRD, 2nd Rx Nyquist			
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THE EQUIPMENT AND SERVICES MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG ANALOG DEVICES.	PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 47 OF 80

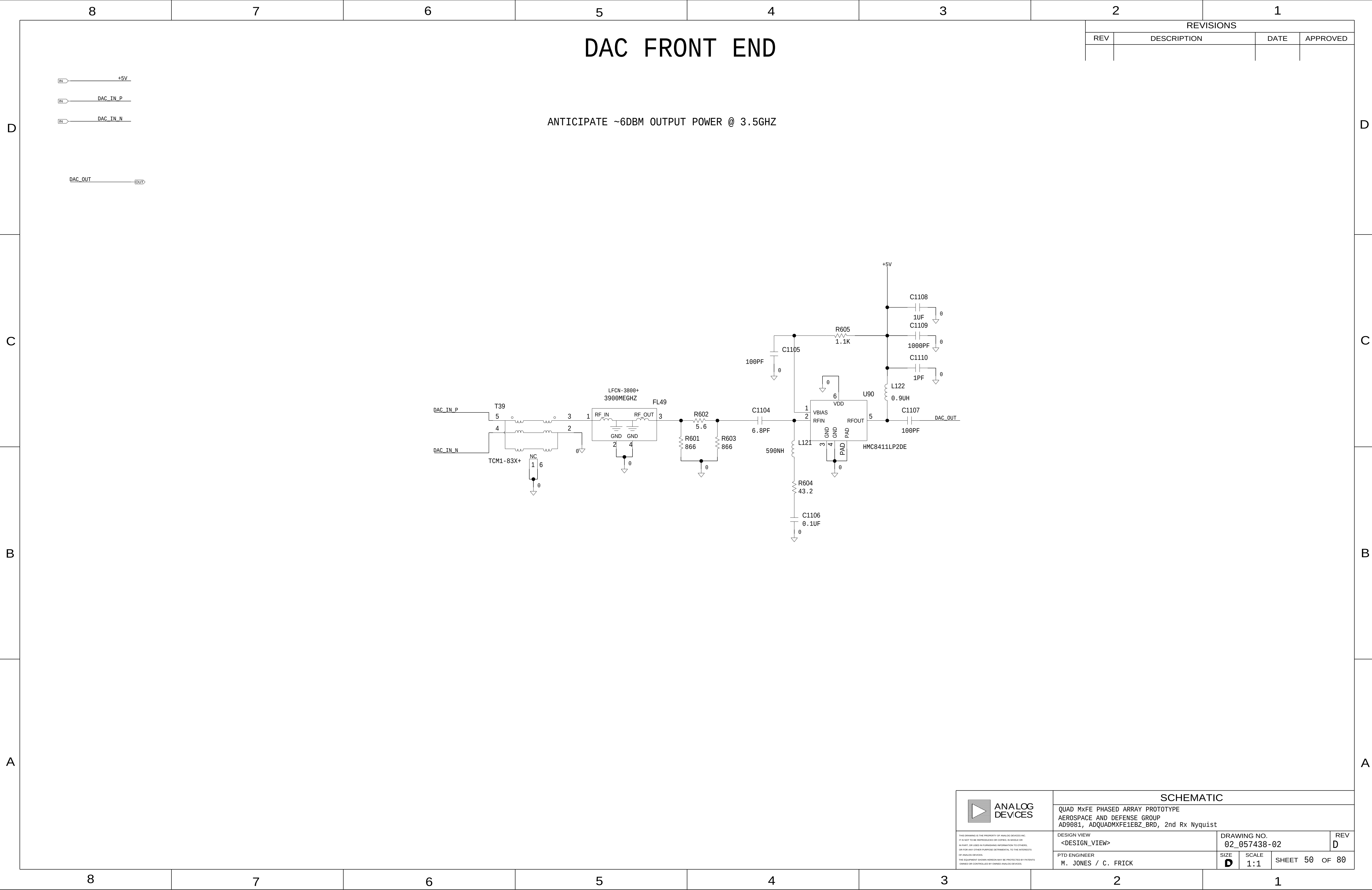
MXFE SUPPLIES

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



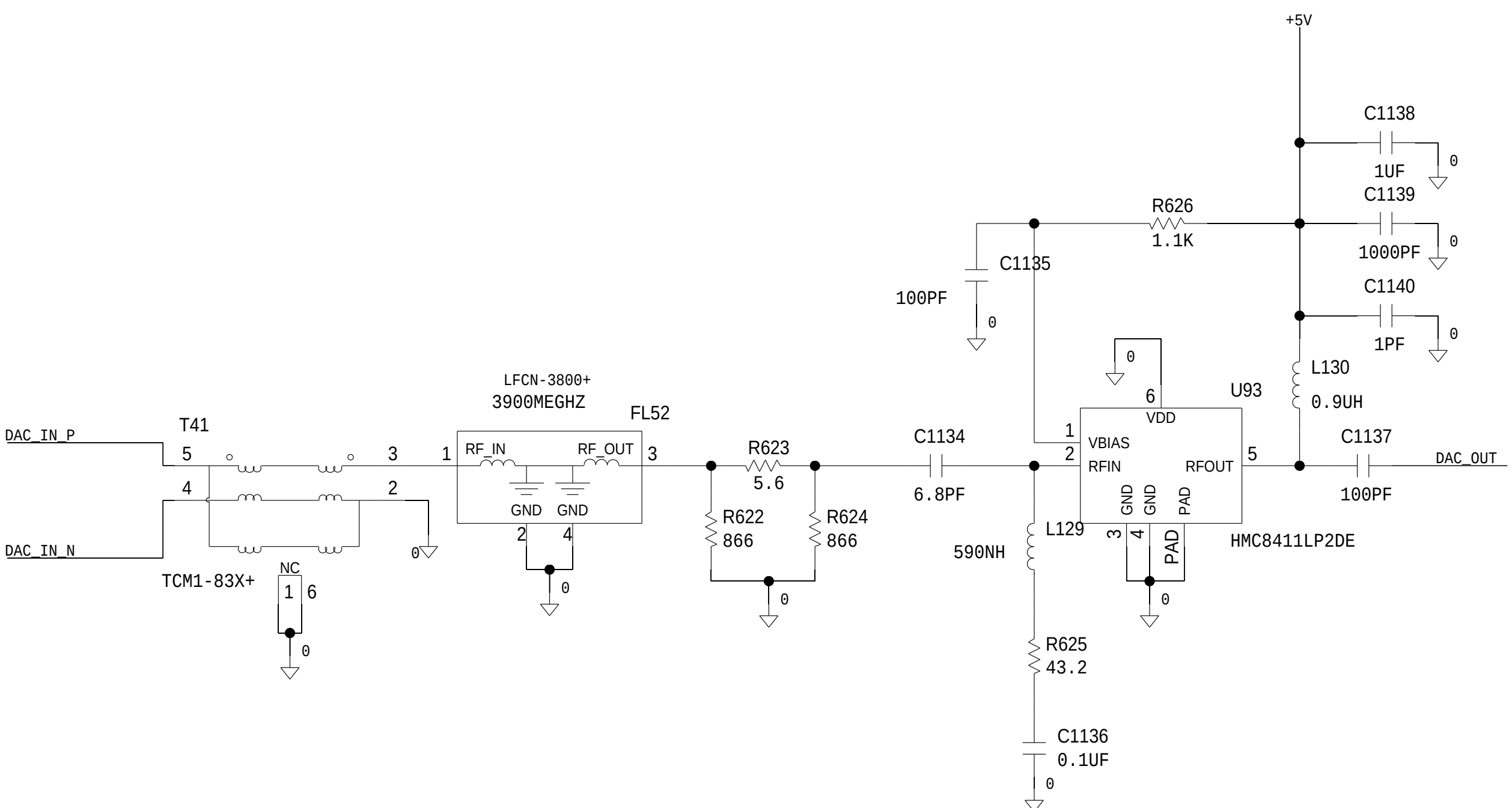
 ANALOG DEVICES	SCHEMATIC				
	QUAD MxFe PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9081, ADQUADMXFE1EBZ_BRD, 2nd Rx Nyquist				
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	PTD ENGINEER M. JONES / C. FRICK		SIZE D	SCALE 1:1	SHEET 48 OF 80



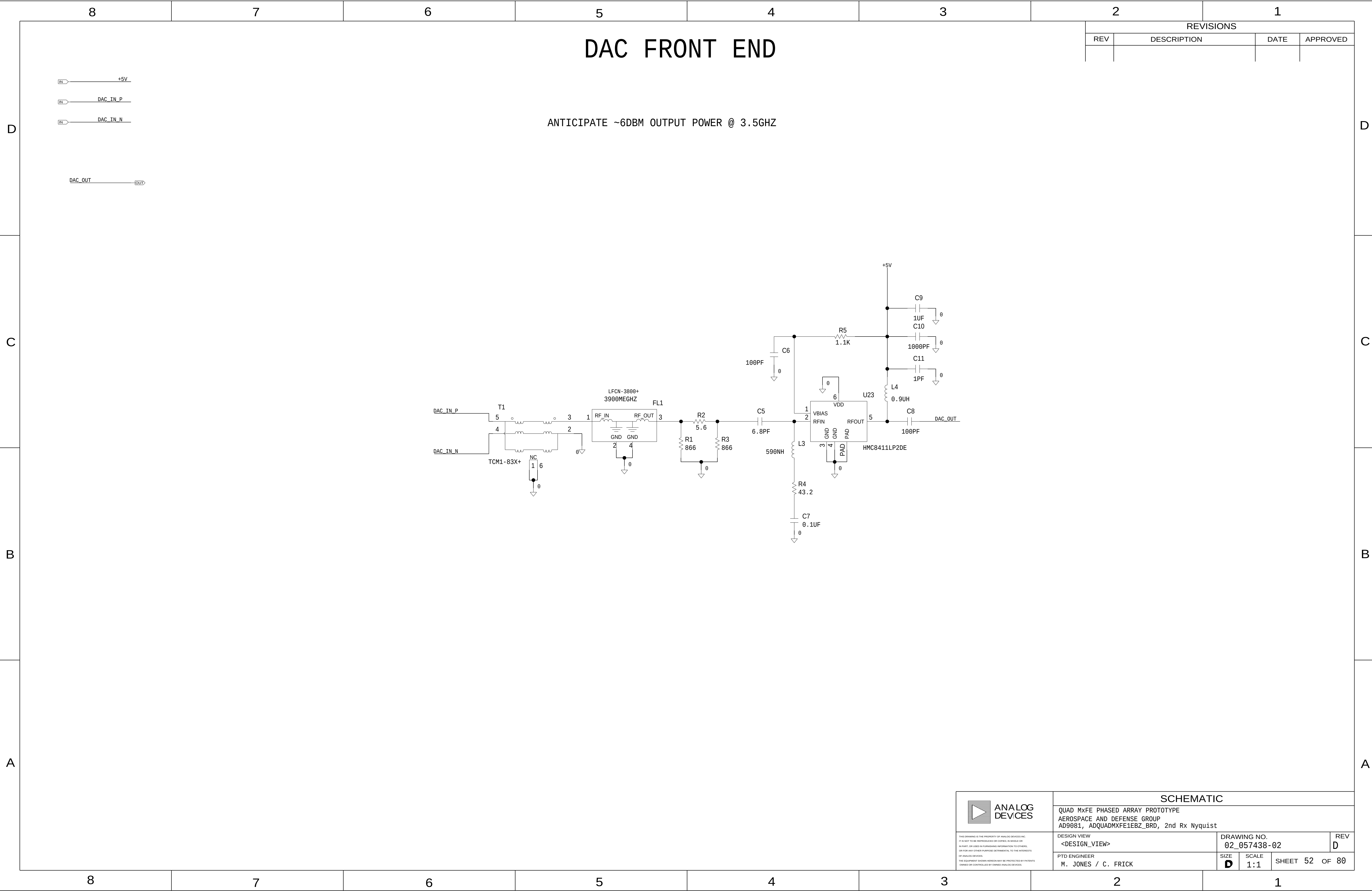


DAC FRONT END

ANTICIPATE ~6DBM OUTPUT POWER @ 3.5GHZ

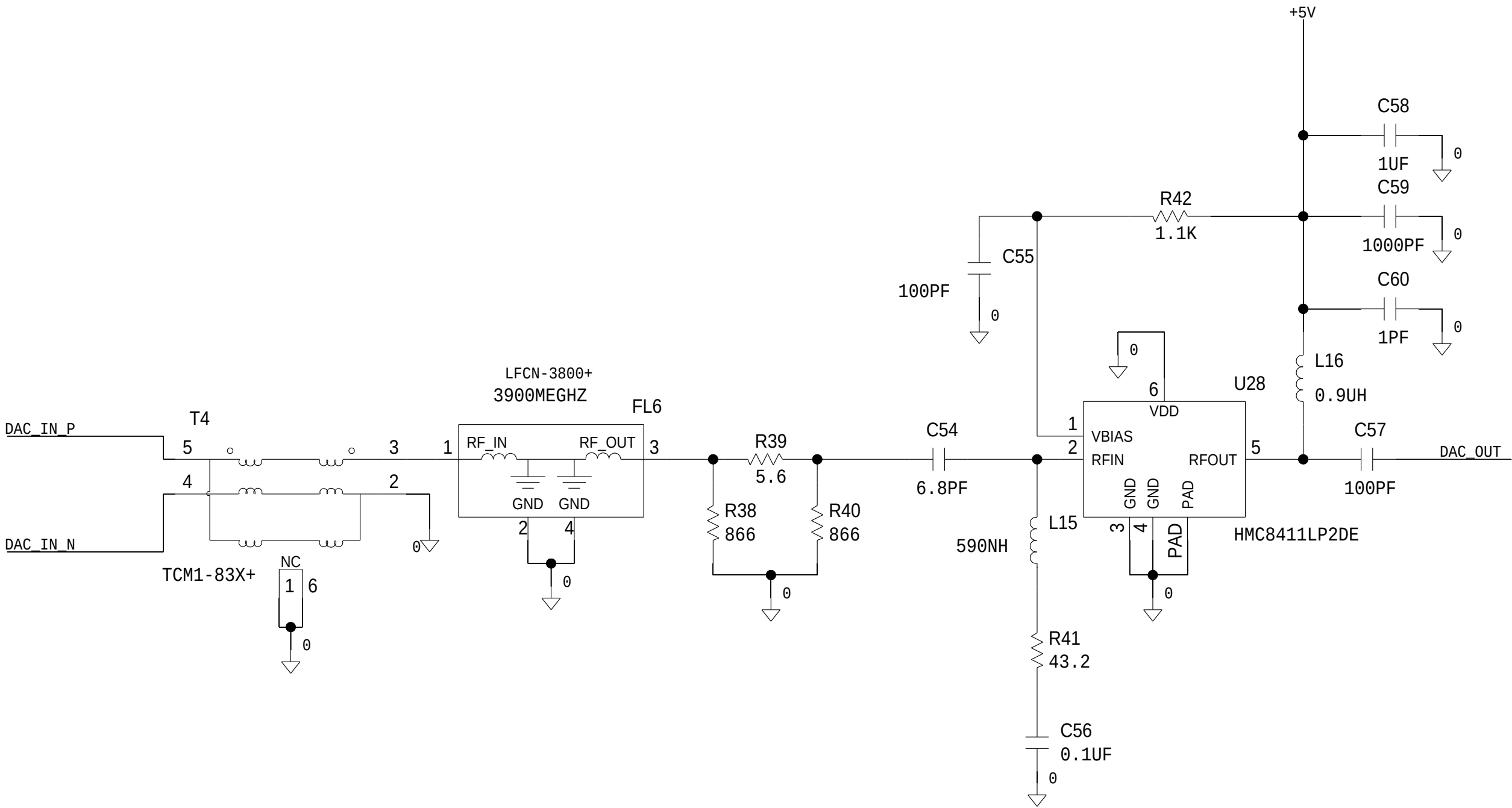


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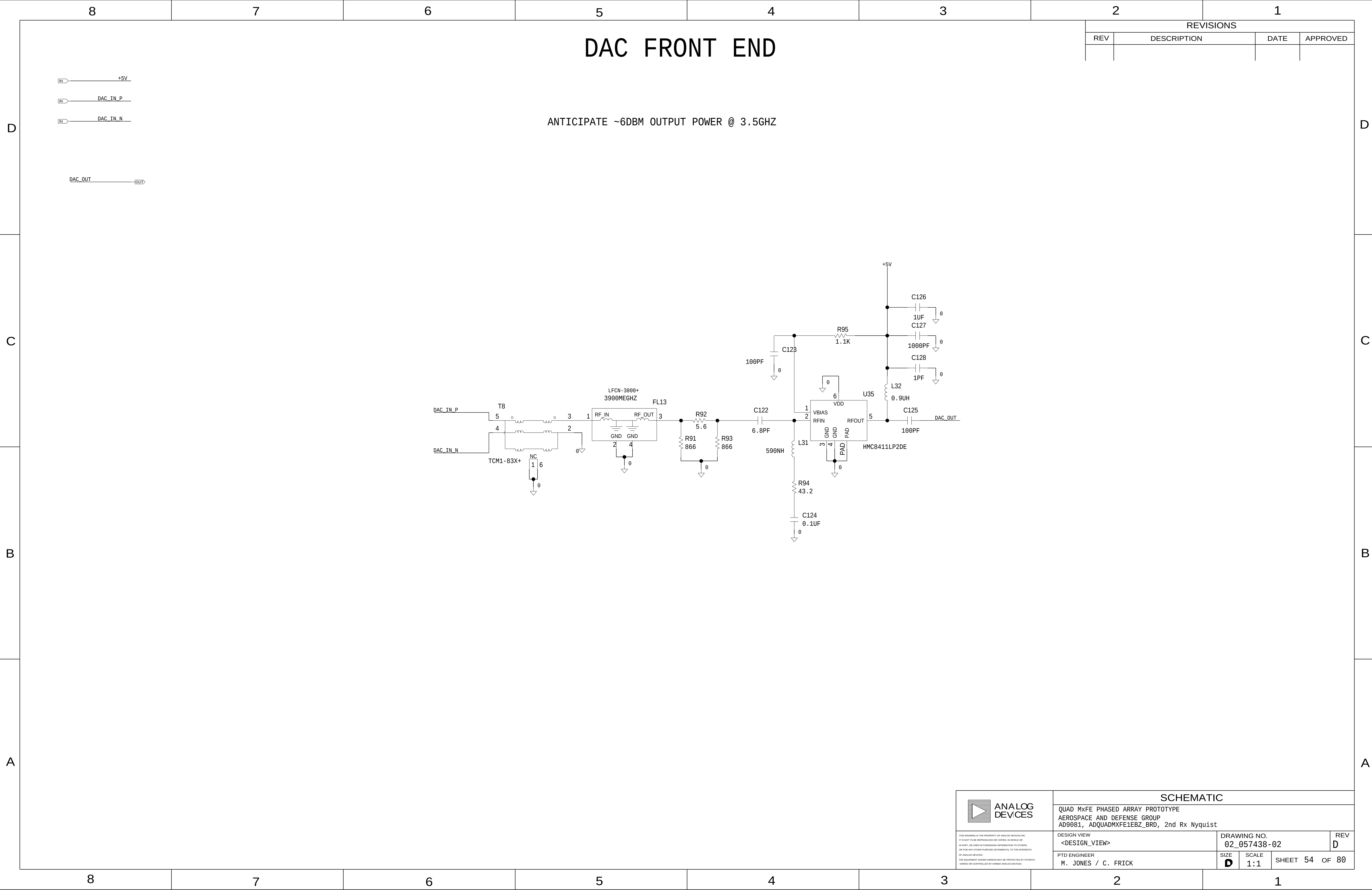


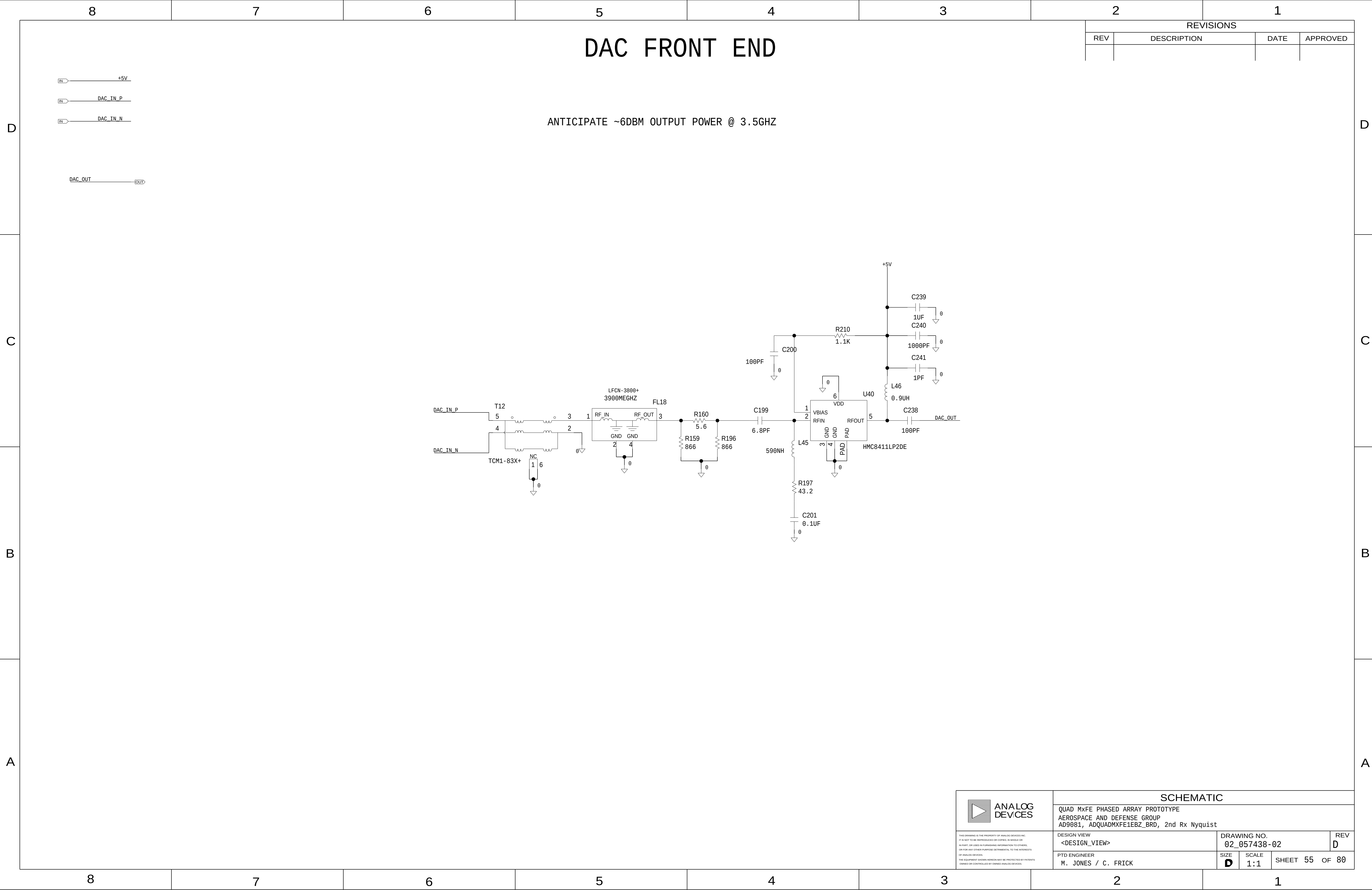
DAC FRONT END

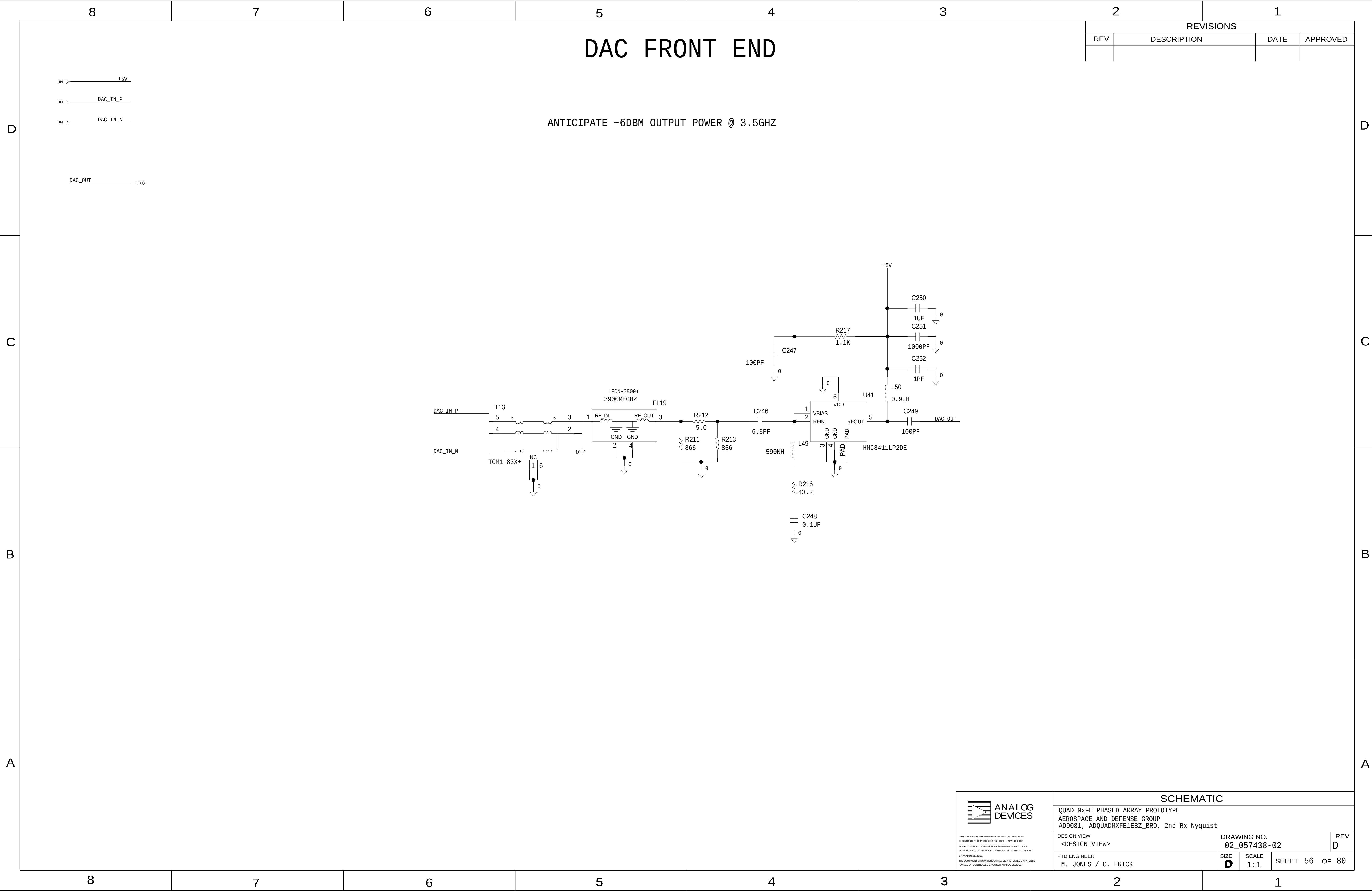
ANTICIPATE ~6DBM OUTPUT POWER @ 3.5GHZ



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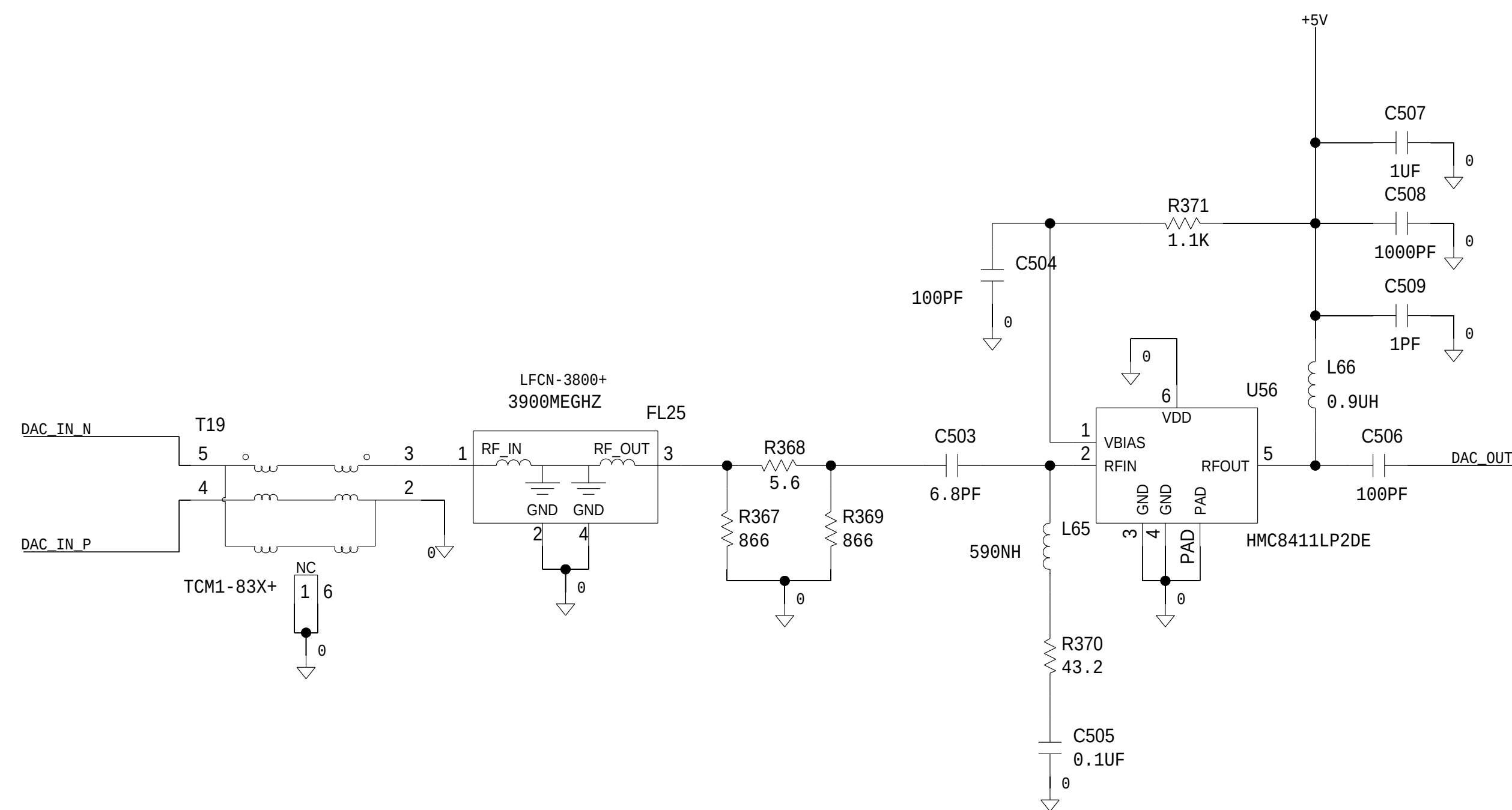






REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

The diagram shows an operational amplifier (op-amp) configured as a voltage follower. The non-inverting input (+) is connected to a signal source labeled "DAC_IN P". The inverting input (-) is connected to the output of the op-amp, which is labeled "DAC_OUT". The op-amp is powered by a +5V supply and ground. The output of the op-amp is also connected to a load resistor and a switch labeled "OUT".



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QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9081, ADQUADMxFE1EBZ_BRD, 2nd Rx Nyquist

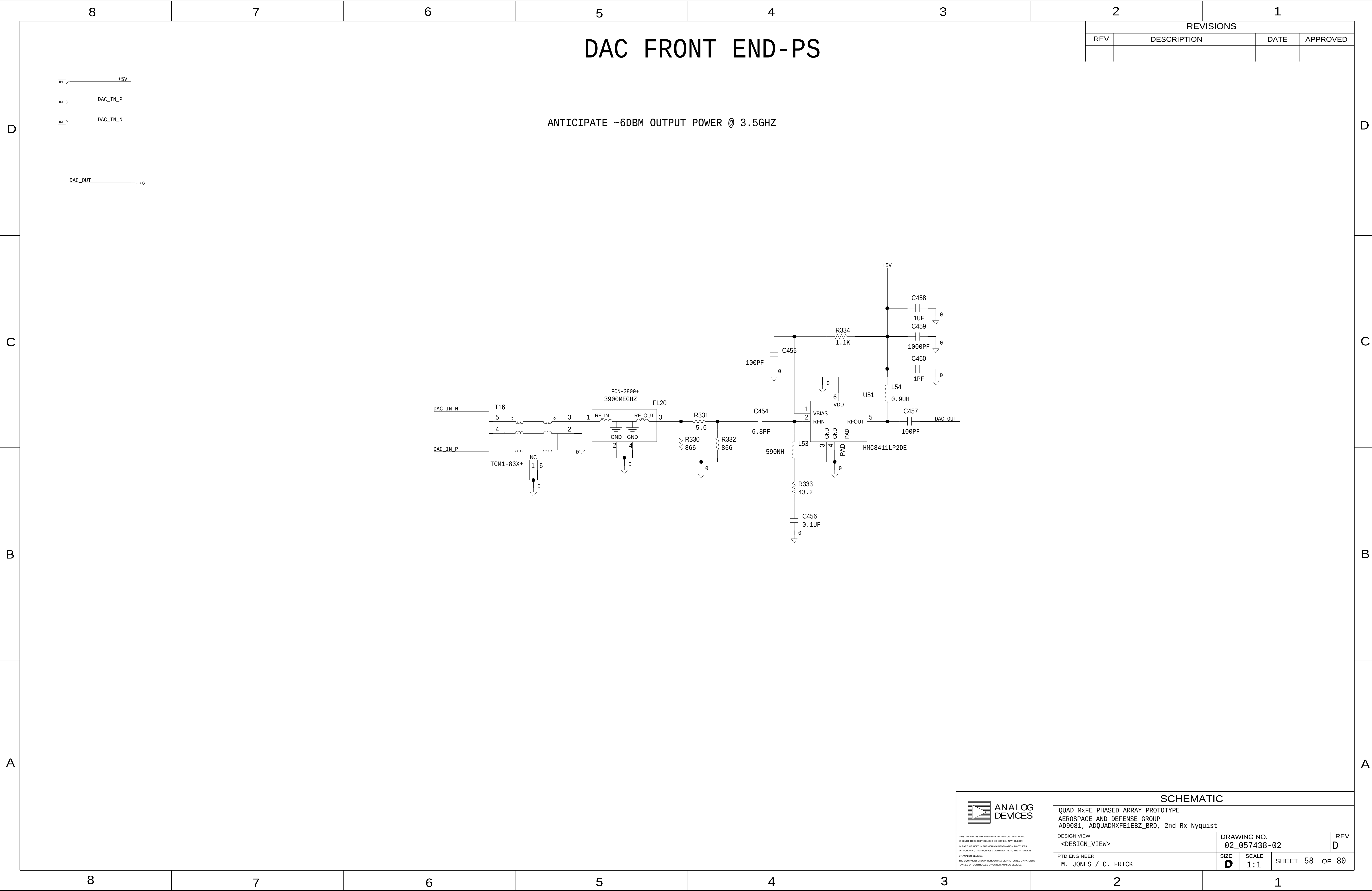
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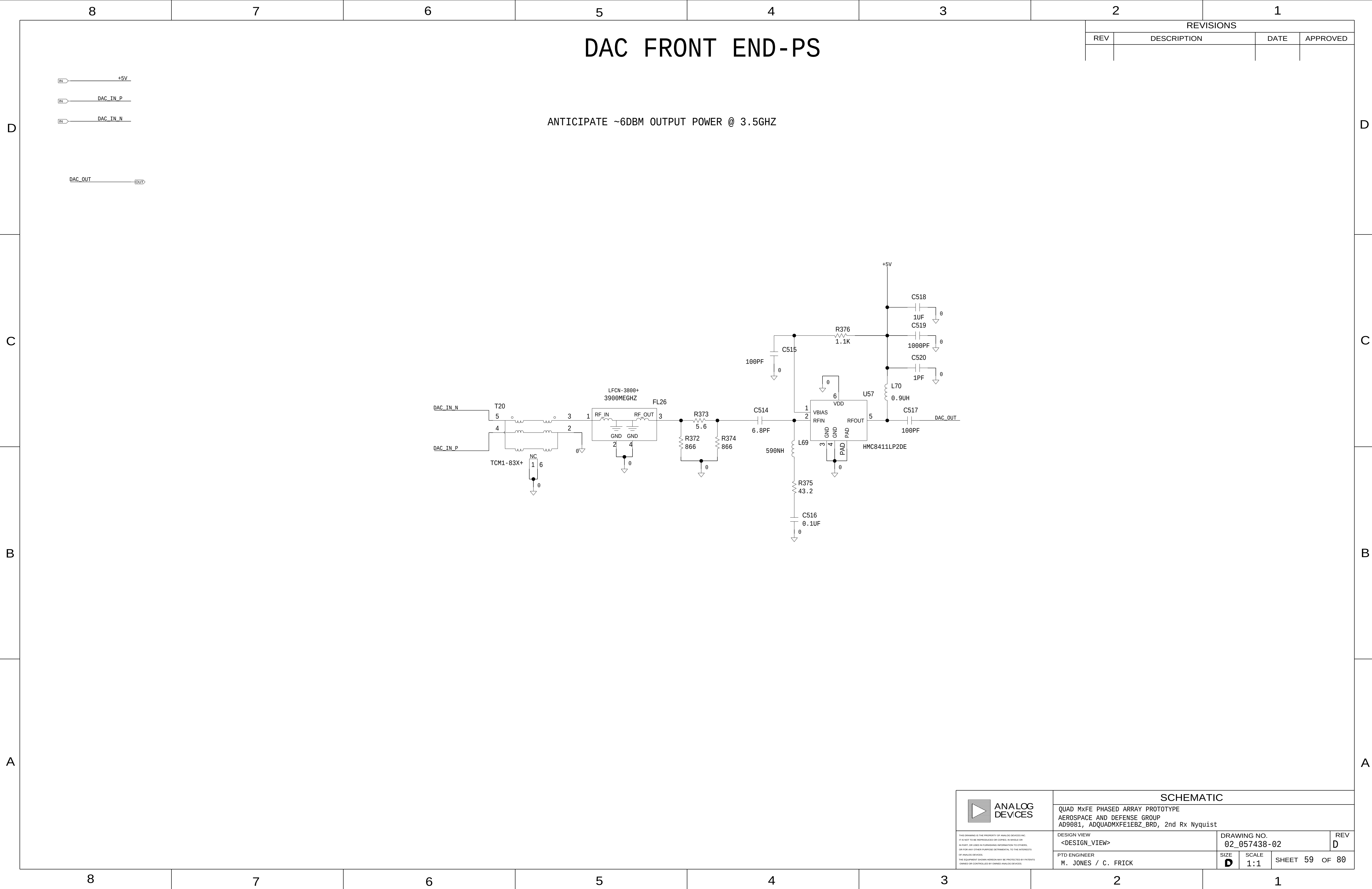
PTD ENGINEER
M. JONES / C. FRICK

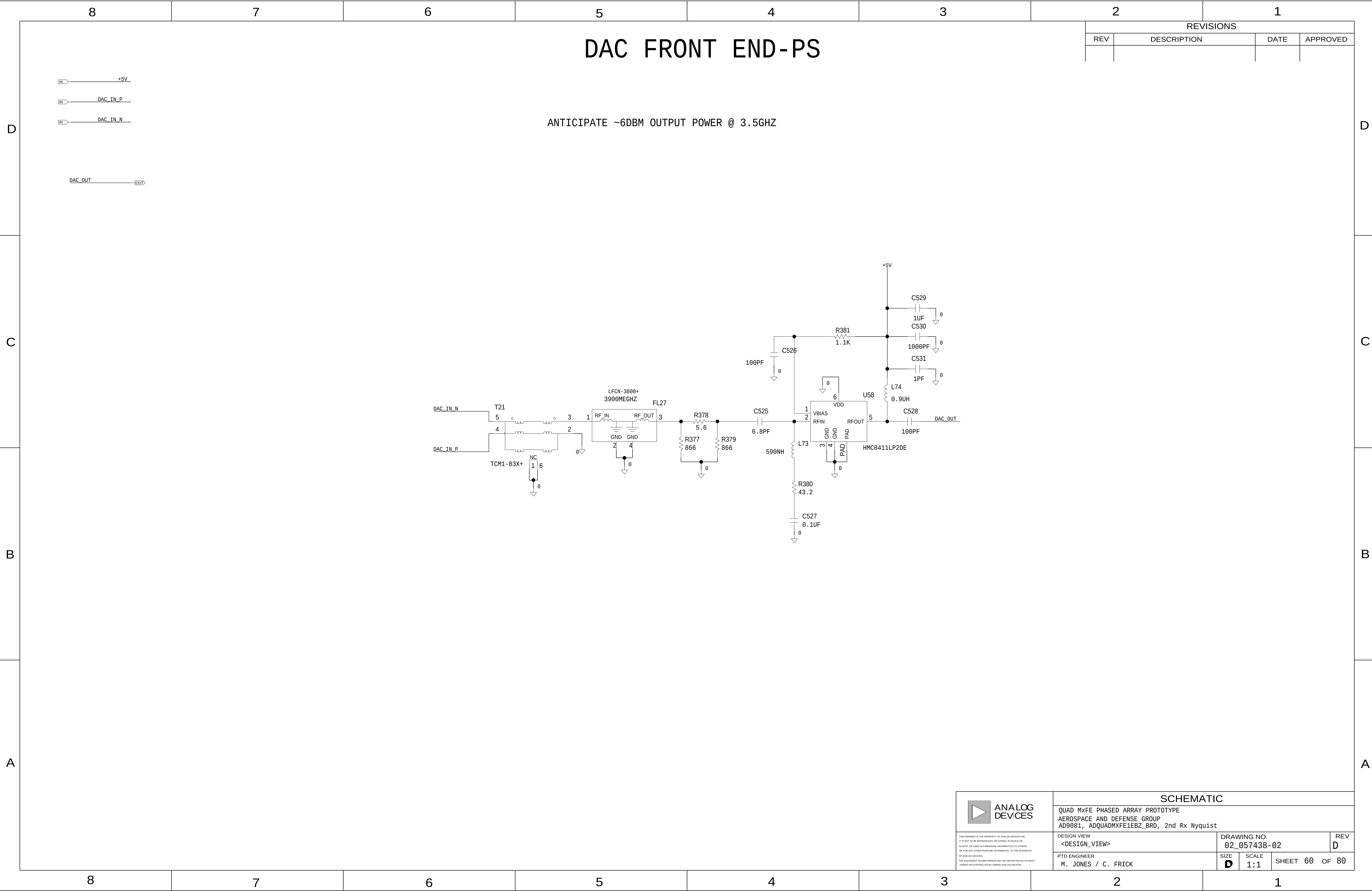
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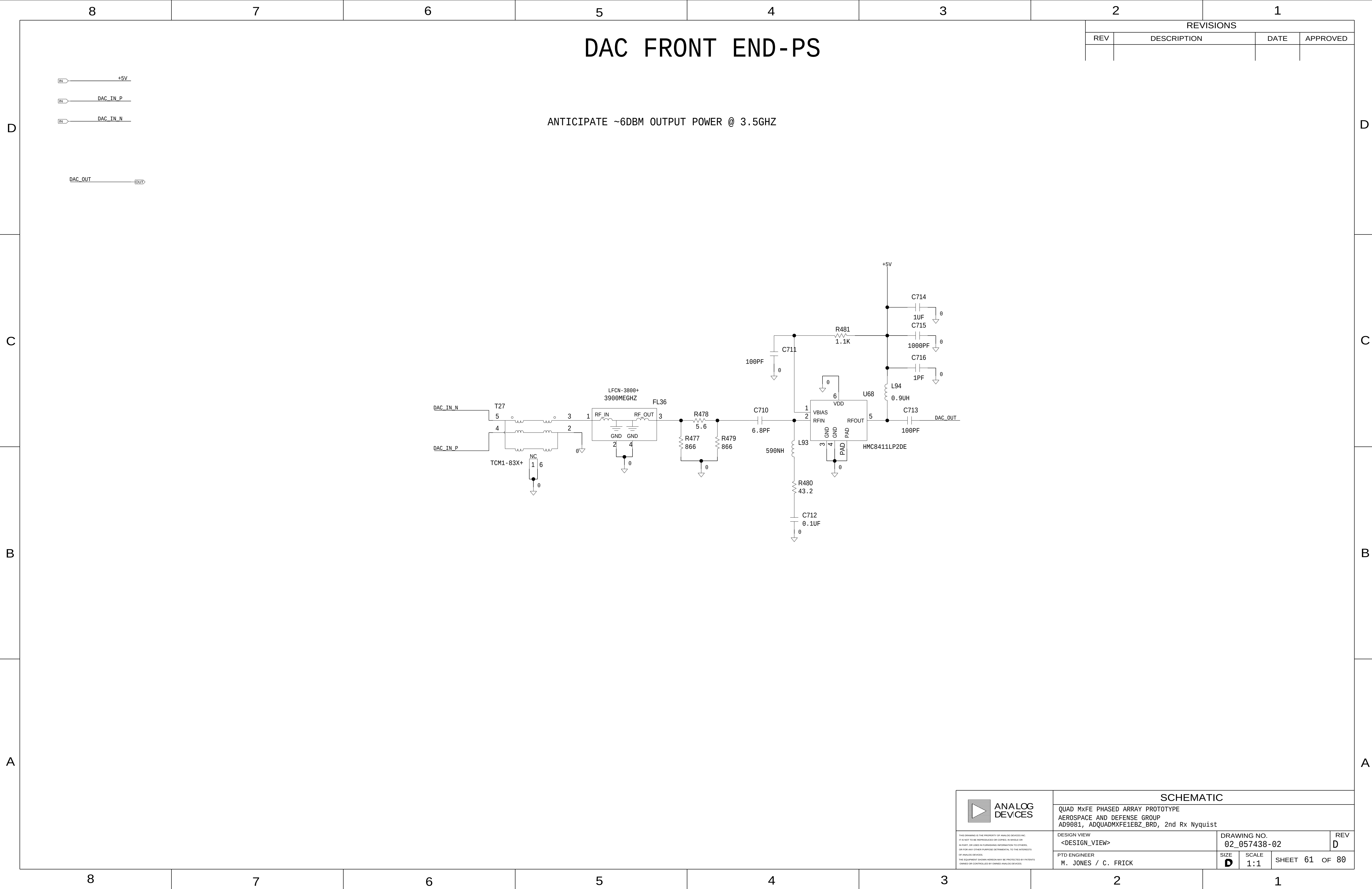
SIZE D	SCALE 1:1	SHEET 57 OF 80
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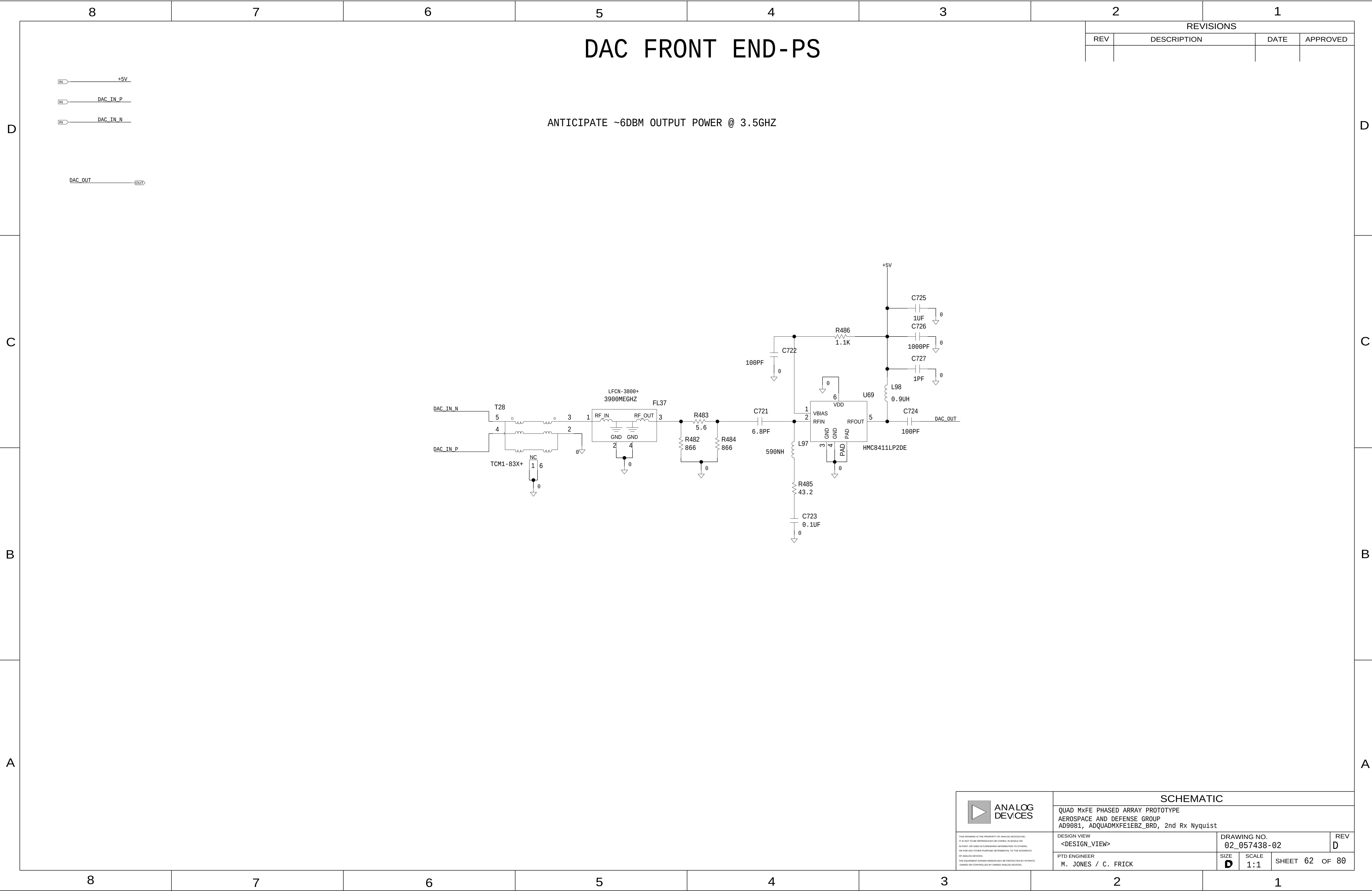
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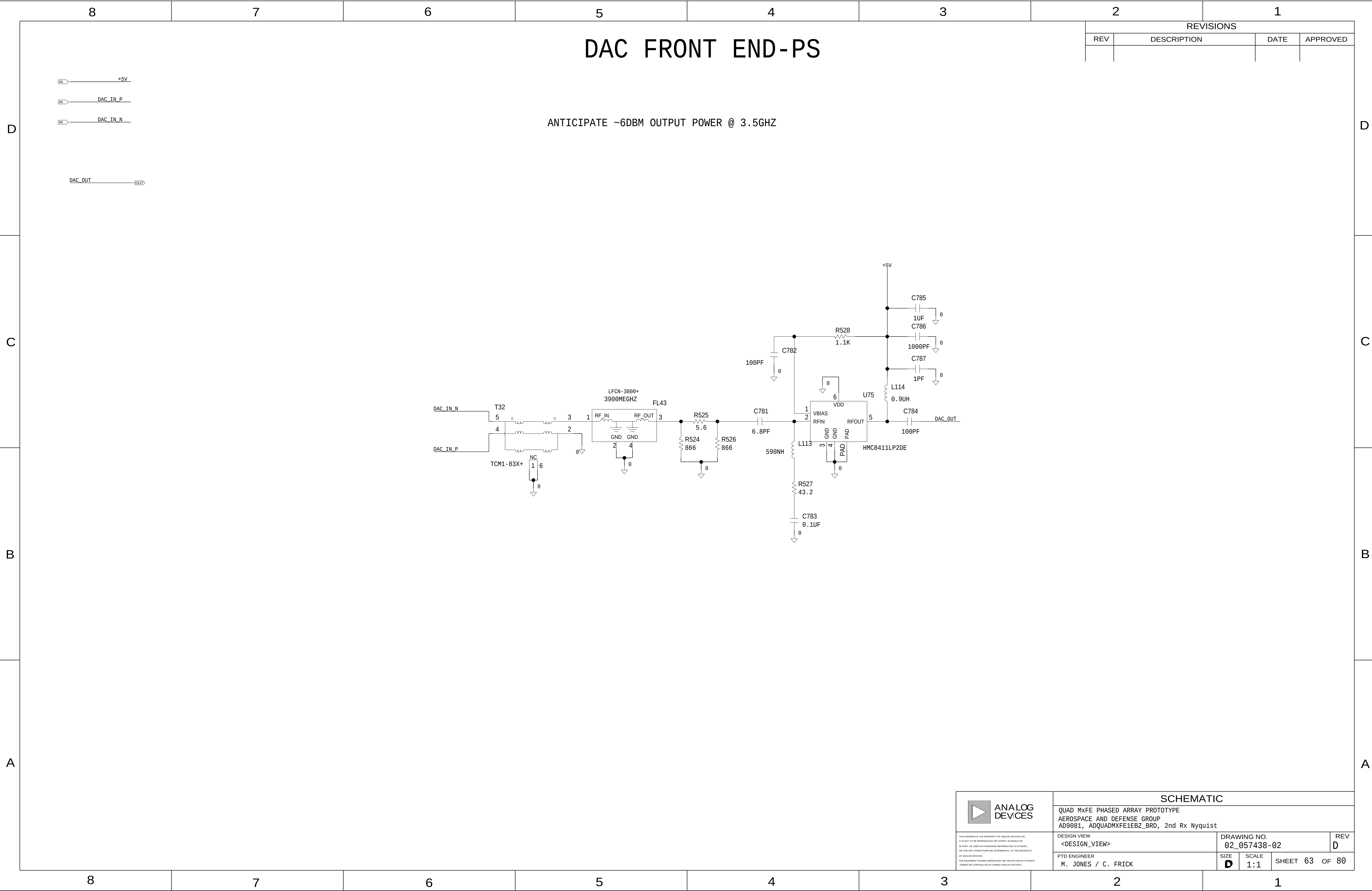






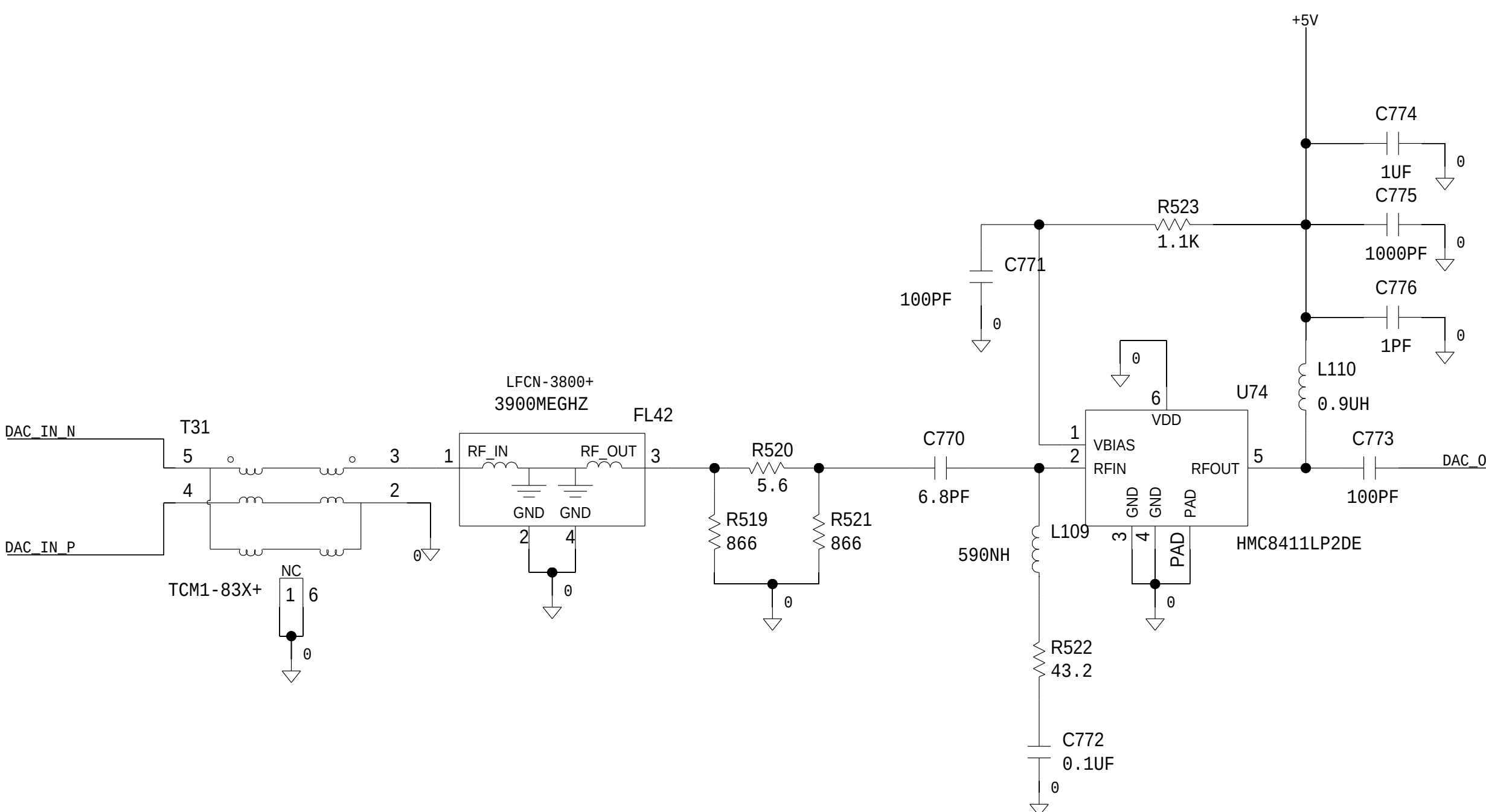






DAC FRONT END-PS

ANTICIPATE ~6DBM OUTPUT POWER @ 3.5GH.



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ADC FRONT END

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

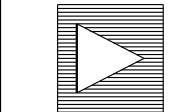
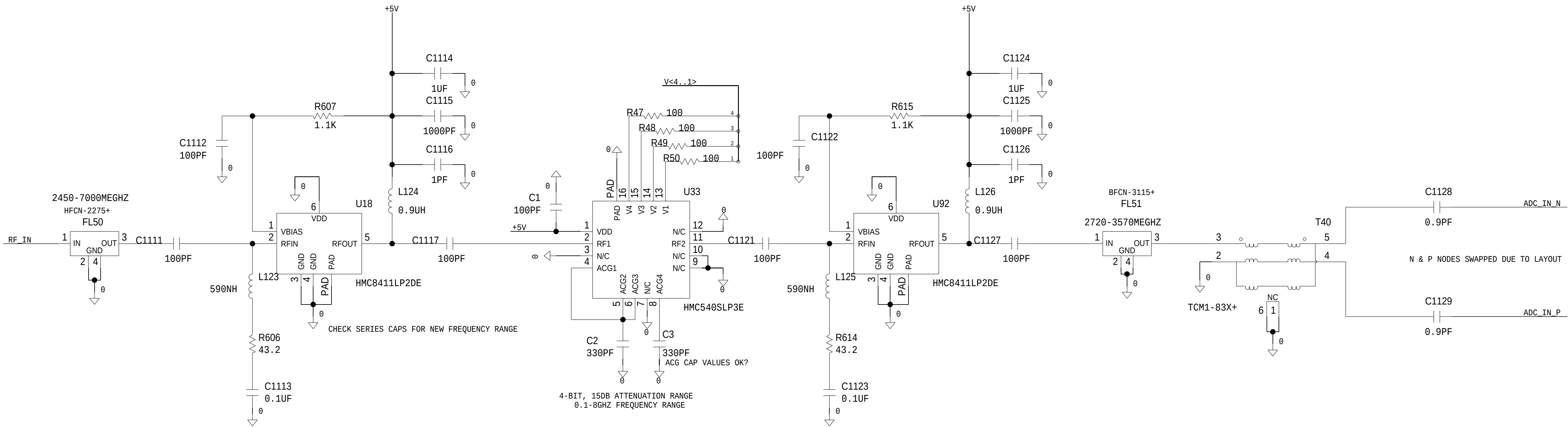
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IN +5V

IN RF_IN

ADC_IN_P OUT

ADC_IN_N OUT

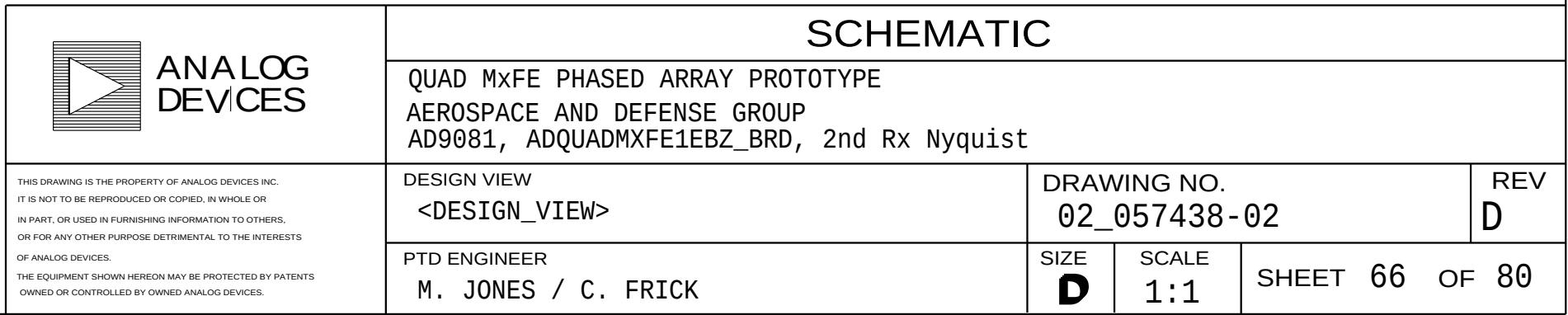


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SCHEMATIC				
QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9081, ADQUADMxFE1EBZ_BRD, 2nd Rx Nyquist				
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_057438-02		REV D	
PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 65 OF 80	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



ADC FRONT END

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

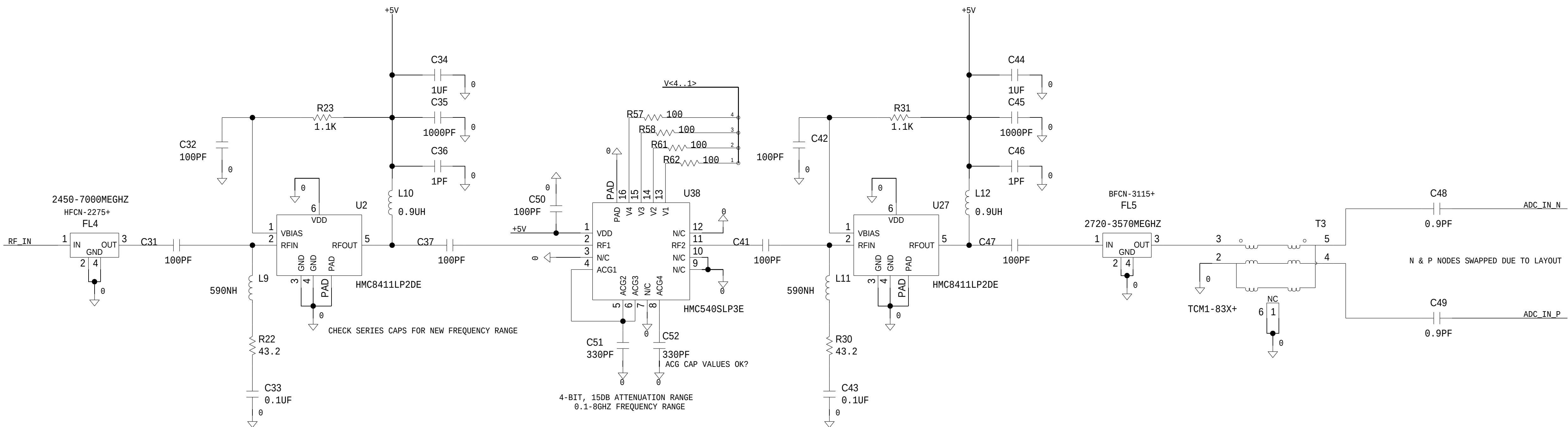
IN V<4...1>

IN +5V

IN RF_IN

ADC_IN_P OUT

ADC_IN_N OUT



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		DESIGN VIEW <DESIGN_VIEW>		DRAWING NO. 02_057438-02	
		PTD ENGINEER M. JONES / C. FRICK		SIZE D	SCALE 1:1
				SHEET 67	OF 80

ADC FRONT END

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

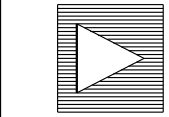
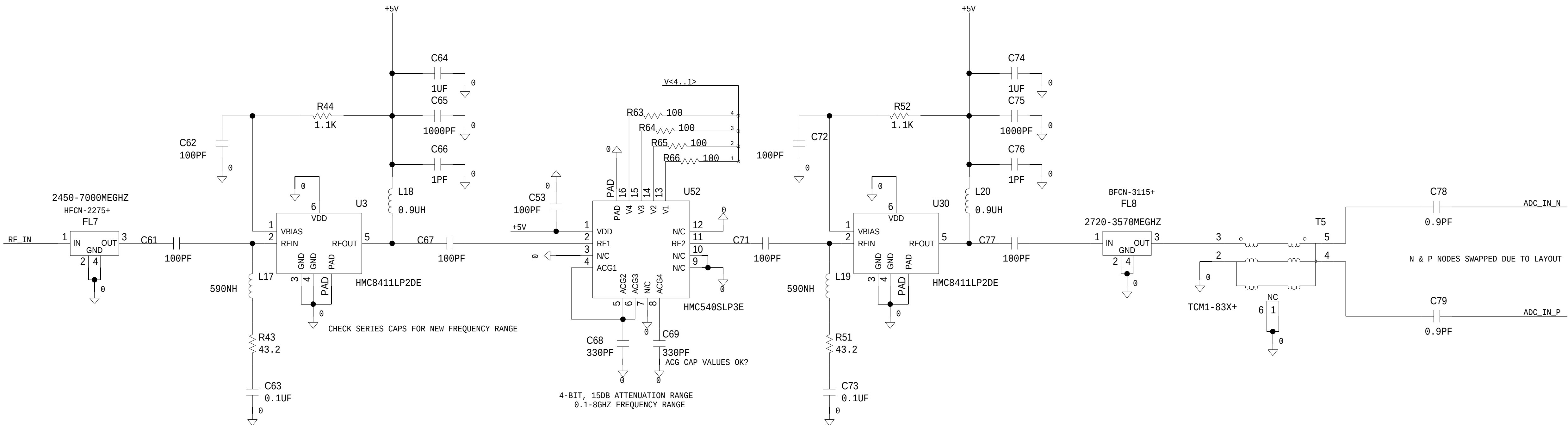
IN V<4...1>

IN +5V

IN RF_IN

ADC_IN_P OUT

ADC_IN_N OUT



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SCHEMATIC				
QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9081, ADQUADMxFE1EBZ_BRD, 2nd Rx Nyquist				
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_057438-02		REV D	
PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 68 OF 80	

ADC FRONT END

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

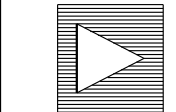
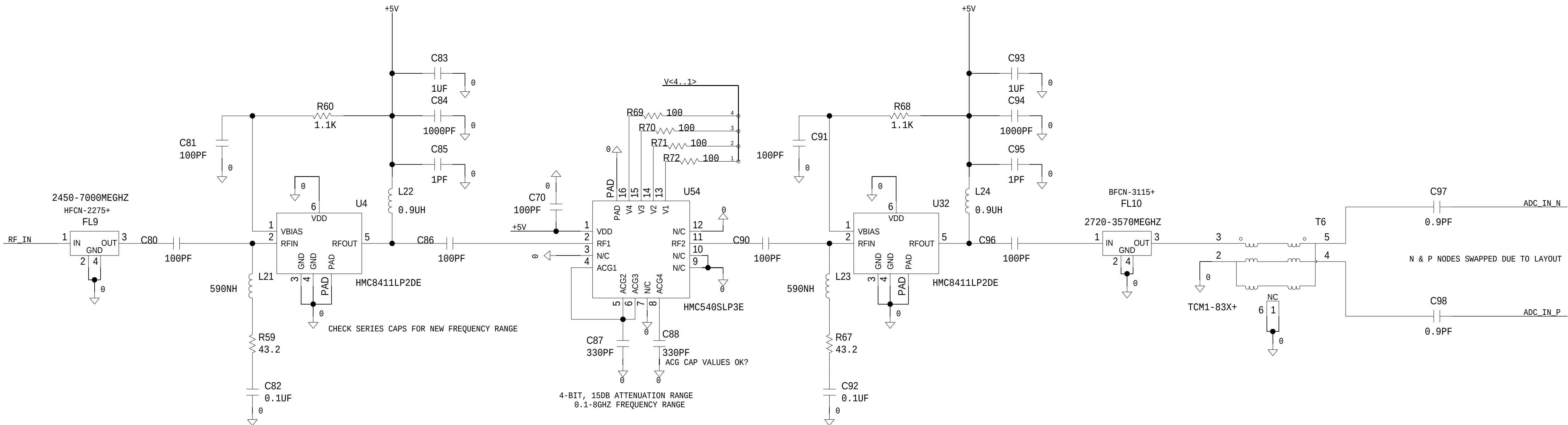
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IN +5V

IN RF_IN

ADC_IN_P OUT

ADC_IN_N OUT



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SCHEMATIC				
QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9081, ADQUADMxFE1EBZ_BRD, 2nd Rx Nyquist				
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_057438-02		REV D	
PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 69 OF 80	

ADC FRONT END

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

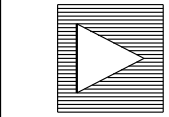
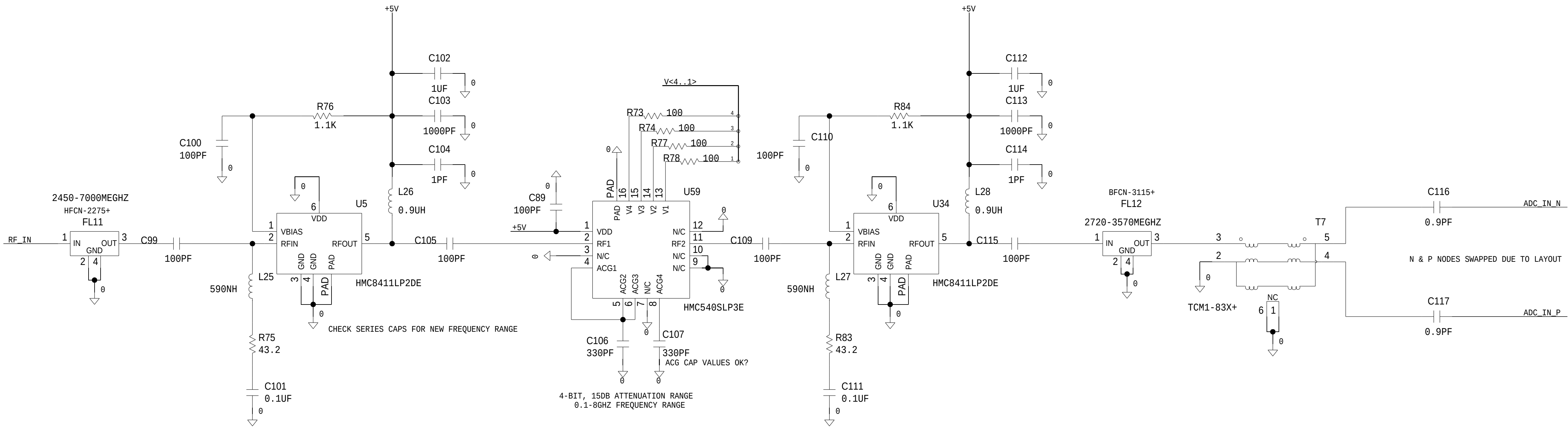
IN V<4...1>

IN +5V

IN RF_IN

ADC_IN_P OUT

ADC_IN_N OUT



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SCHEMATIC				
QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9081, ADQUADMxFE1EBZ_BRD, 2nd Rx Nyquist				
DESIGN VIEW <DESIGN_VIEW>			DRAWING NO. 02_057438-02	
PTD ENGINEER M. JONES / C. FRICK			SIZE D	SCALE 1:1
			SHEET 70 OF 80	

ADC FRONT END

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

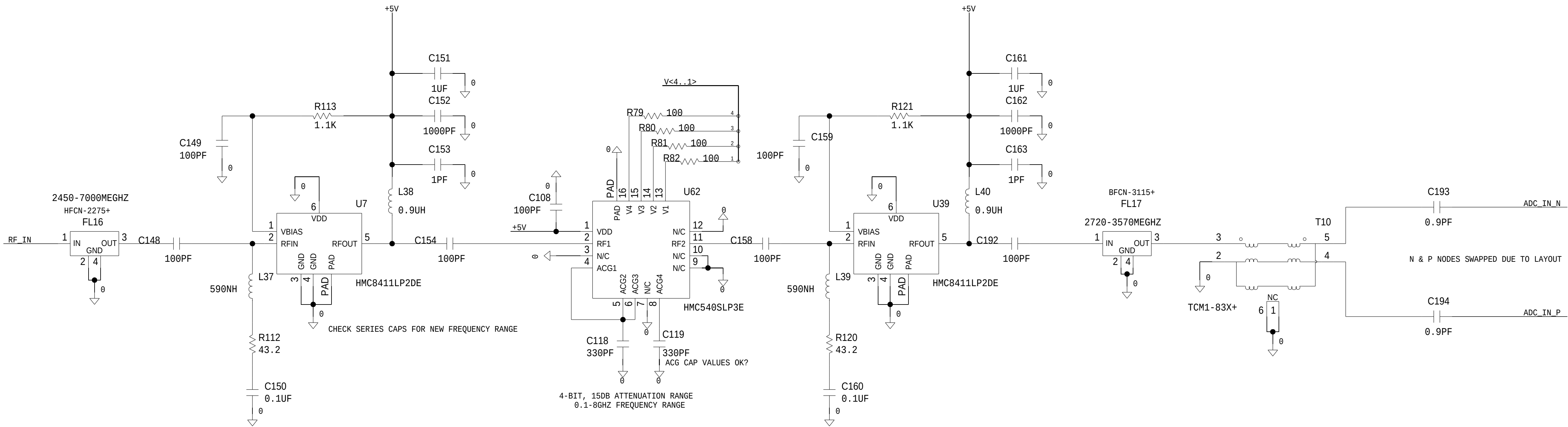
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IN +5V

IN RF_IN

ADC_IN_P OUT

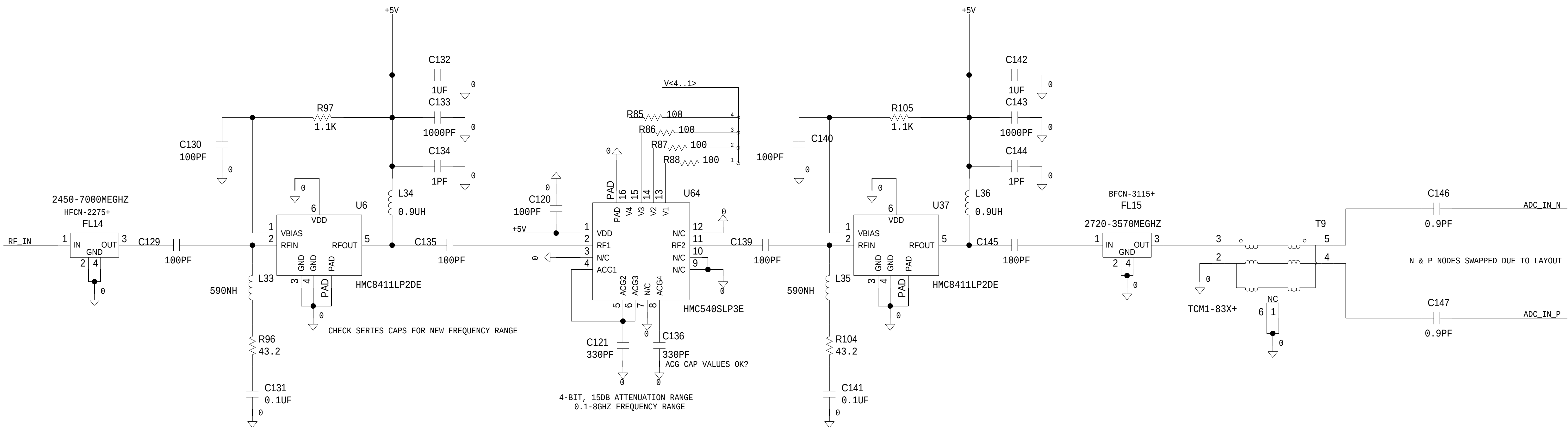
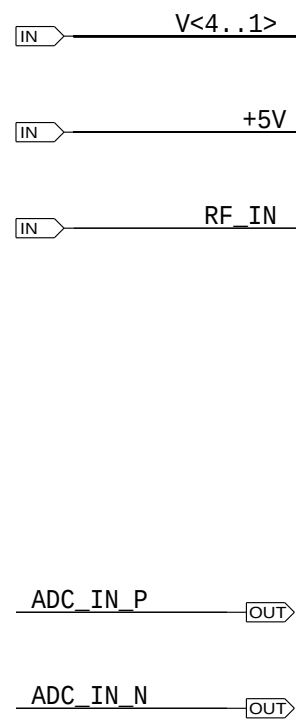
ADC_IN_N OUT



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		DESIGN VIEW <DESIGN_VIEW>		DRAWING NO. 02_057438-02	
		PTD ENGINEER M. JONES / C. FRICK		SIZE D	SCALE 1:1
				SHEET 71	OF 80

ADC FRONT END

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



ANALOG DEVICES

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9081, ADQUADMxFE1EBZ_BRD, 2nd Rx Nyquist

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
M. JONES / C. FRICK

SCHEMATIC

DRAWING NO.
02_057438-02

SIZE **D** SCALE 1:1 SHEET 72 OF 80

REV
D

ADC FRONT END-WEST

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

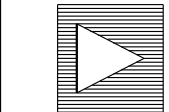
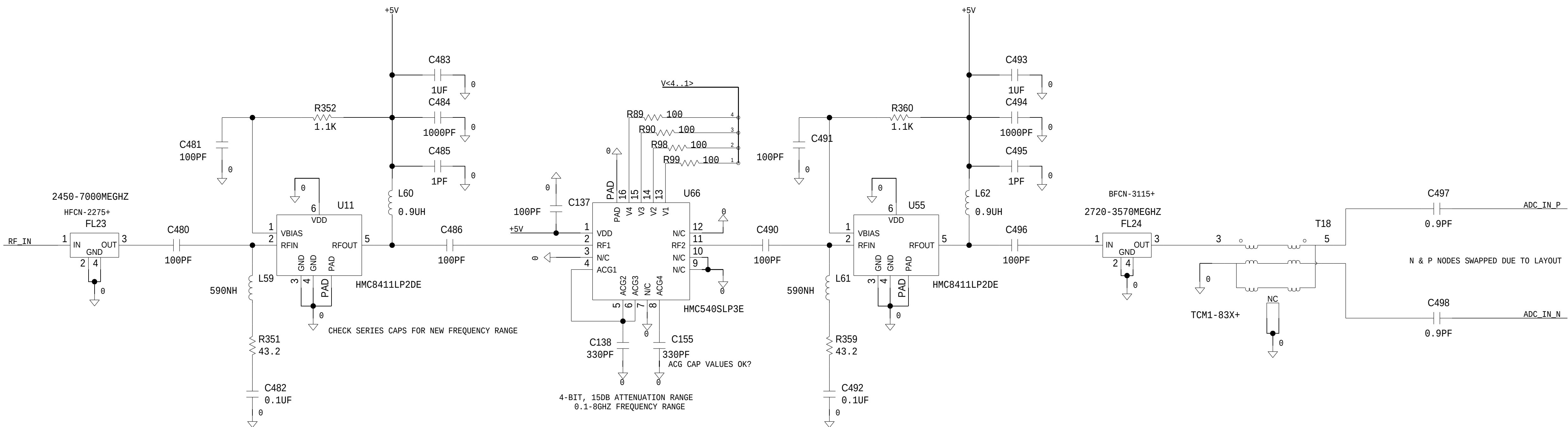
IN V<4...1>

IN +5V

IN RF_IN

ADC_IN_P OUT

ADC_IN_N OUT



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SCHEMATIC				
QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9081, ADQUADMxFE1EBZ_BRD, 2nd Rx Nyquist				
DESIGN VIEW <DESIGN_VIEW>			DRAWING NO. 02_057438-02	
PTD ENGINEER M. JONES / C. FRICK			SIZE D	SCALE 1:1
			SHEET 73 OF 80	
			REV D	

ADC FRONT END-WEST

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

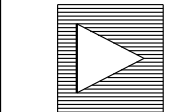
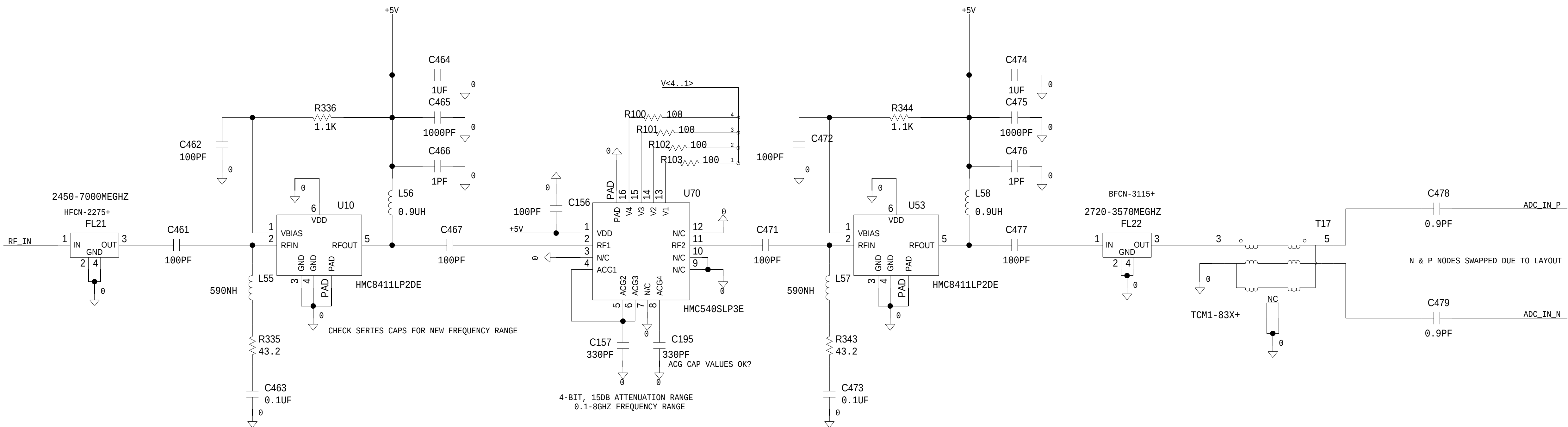
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IN +5V

IN RF_IN

ADC_IN_P OUT

ADC_IN_N OUT



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SCHEMATIC

QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9081, ADQUADMxFE1EBZ_BRD, 2nd Rx Nyquist

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
M. JONES / C. FRICK

DRAWING NO.
02_057438-02

SIZE
D

SCALE
1:1

SHEET 74 OF 80

REV
D

ADC FRONT END-WEST

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

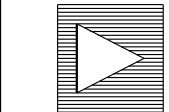
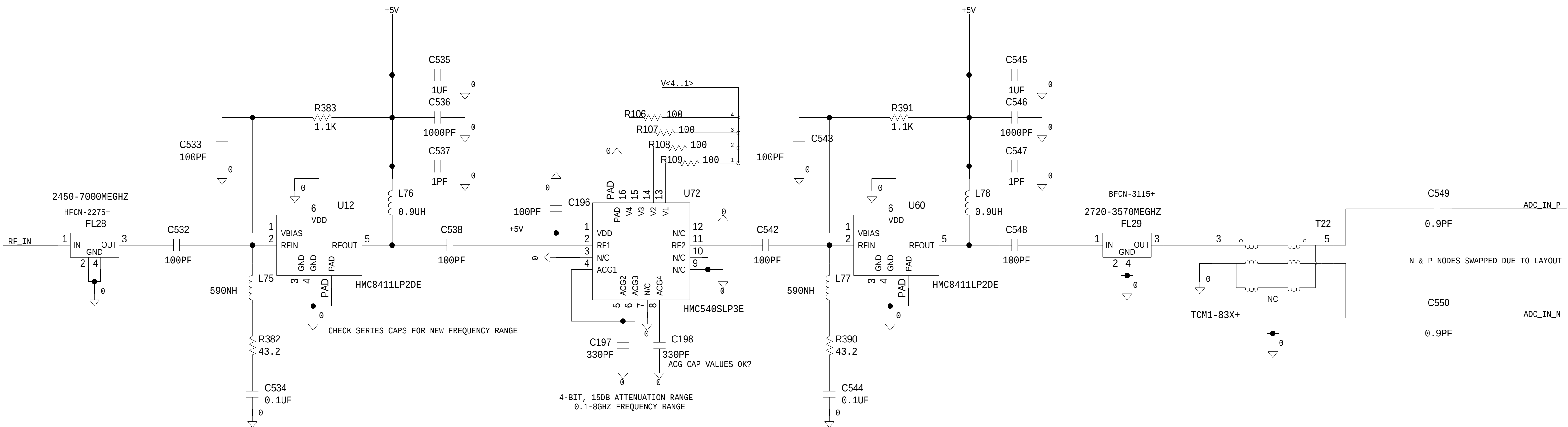
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IN +5V

IN RF_IN

ADC_IN_P OUT

ADC_IN_N OUT

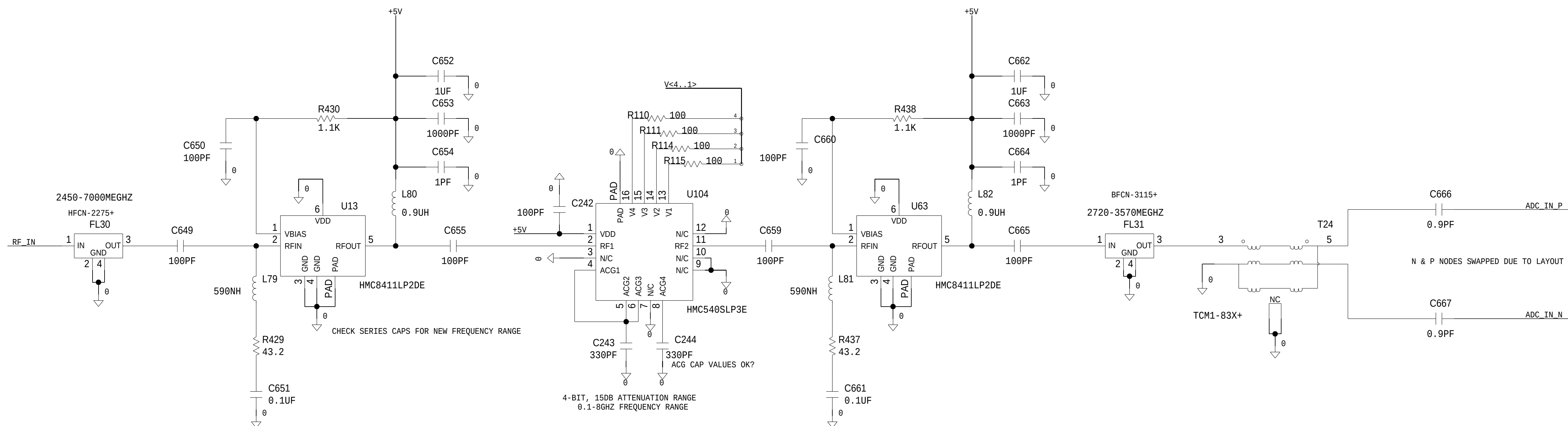
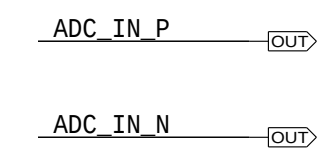


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SCHEMATIC				
QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9081, ADQUADMxFE1EBZ_BRD, 2nd Rx Nyquist				
DESIGN VIEW <DESIGN_VIEW>			DRAWING NO. 02_057438-02	
PTD ENGINEER M. JONES / C. FRICK			SIZE D	SCALE 1:1
			SHEET 75 OF 80	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



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QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9081, ADQUADMxFE1EBZ_BRD, 2nd Rx Nyquist

DESIGN VIEW	D
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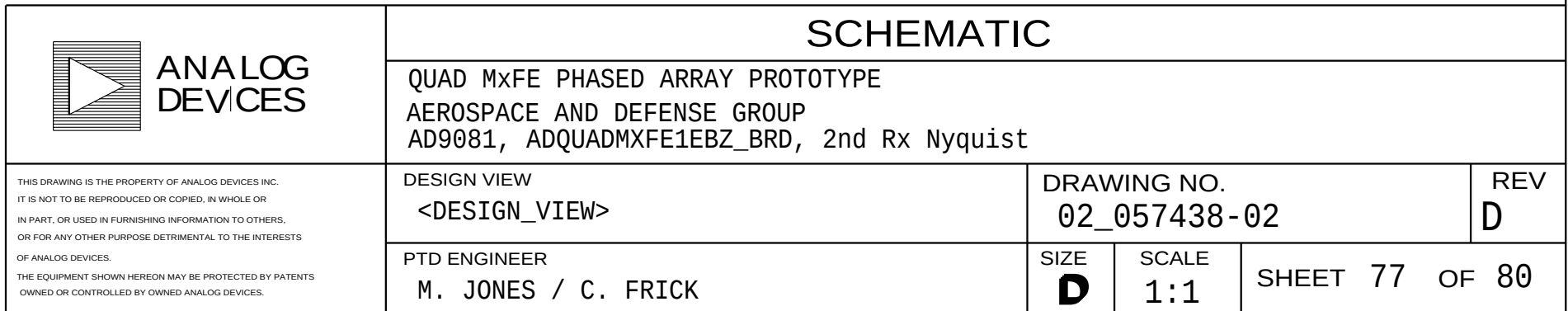
PTD ENGINEER
M. JONES / C. FRICK

DRAWING NO.
02 057438-02

SIZE D	SCALE 1:1	SHEET 76 OF 80
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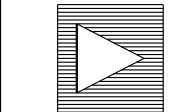
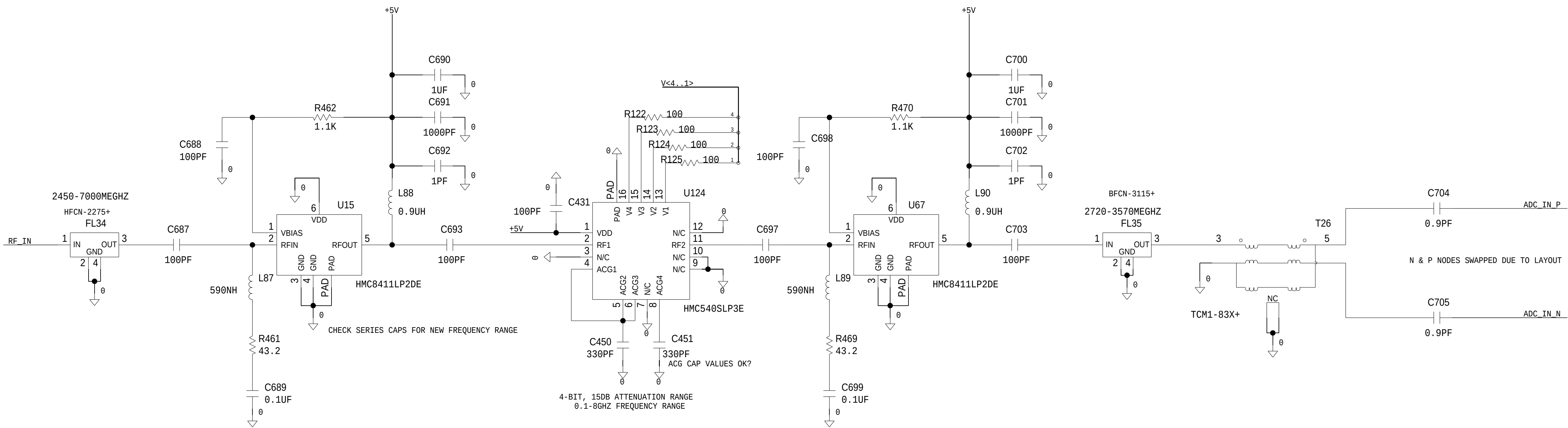
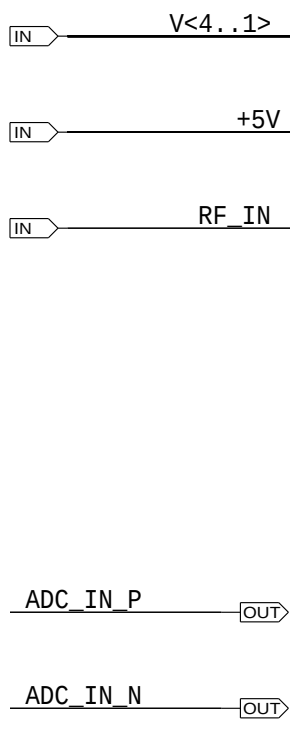
REV
D

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



ADC FRONT END-WEST

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



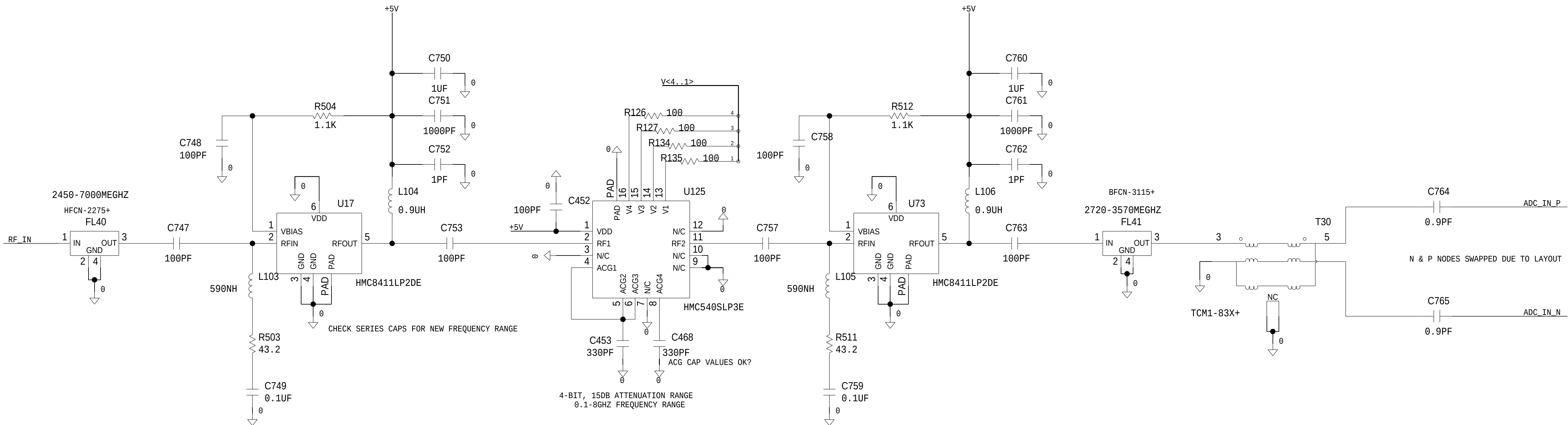
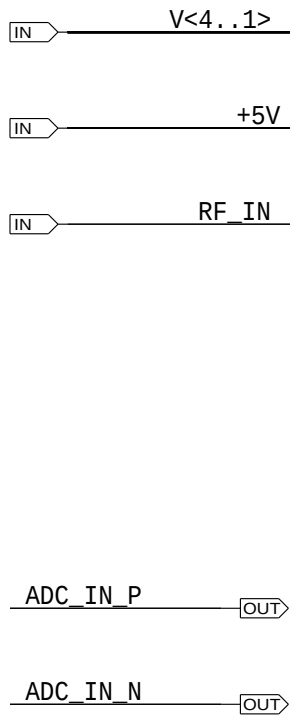
ANALOG
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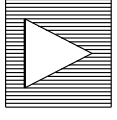
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SCHEMATIC				
QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9081, ADQUADMxFE1EBZ_BRD, 2nd Rx Nyquist				
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_057438-02		REV D	
PTD ENGINEER M. JONES / C. FRICK	SIZE D	SCALE 1:1	SHEET 78 OF 80	

ADC FRONT END-WEST

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



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SCHEMATIC
QUAD MxFE PHASED ARRAY PROTOTYPE
AEROSPACE AND DEFENSE GROUP
AD9081, ADQUADMxFE1EBZ_BRD, 2nd Rx Nyquist

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
M. JONES / C. FRICK

DRAWING NO.
02_057438-02

SIZE
D

REV
D

SCALE
1:1

SHEET 79 OF 80

ADC FRONT END-WEST

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

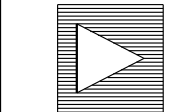
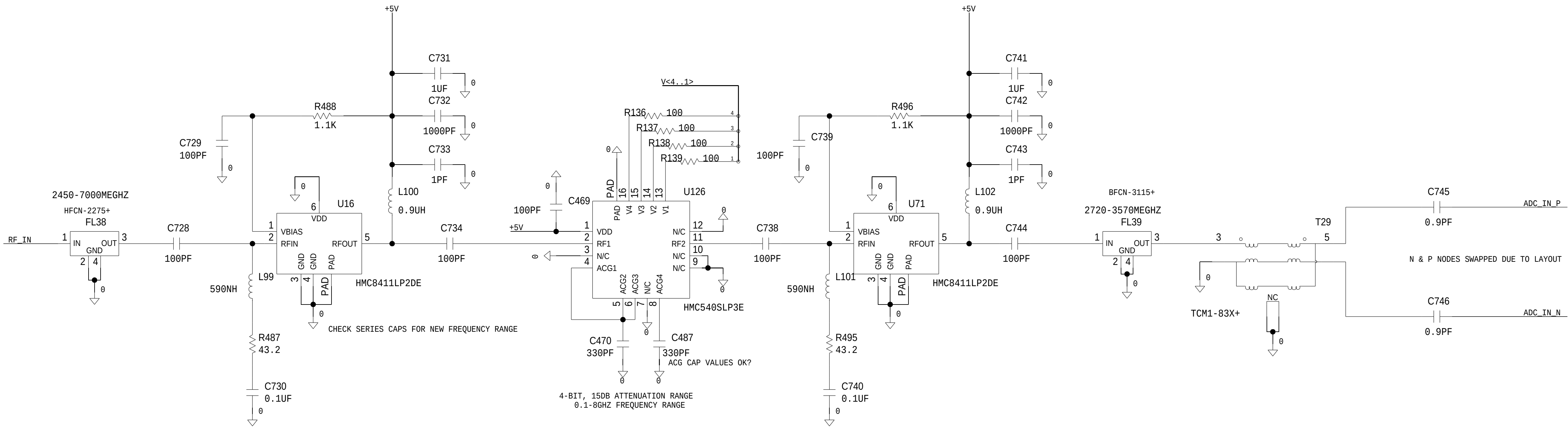
IN V<4...1>

IN +5V

IN RF_IN

ADC_IN_P OUT

ADC_IN_N OUT



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SCHEMATIC				
QUAD MxFE PHASED ARRAY PROTOTYPE AEROSPACE AND DEFENSE GROUP AD9081, ADQUADMxFE1EBZ_BRD, 2nd Rx Nyquist				
DESIGN VIEW <DESIGN_VIEW>			DRAWING NO. 02_057438-02	
PTD ENGINEER M. JONES / C. FRICK			SIZE D	SCALE 1:1
			SHEET 80	OF 80