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EDGE PLATING NOT ALLOWED IN CENTER CONDUCTOR
AND GAP AREA. EDGE PLATING SHOULD BE IN LINE
WITH TOP ETCH.

EDGE PLATING AND PCB ETCH ON RF CONDUCTOR
TRACE SHOULD BE FLUSHED $\pm .002"$. NO BUMPS.

DETAIL A

4 LAYER STACKUP

DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	PLATED	QTY	TOLERANCE/NOTES
•	8.0	PLATED	460	DIA MAX / SEE NOTE 18
•	8.01	PLATED	10	DIA MAX / SEE NOTE 15
•	14.0	PLATED	48	DIA MAX / SEE NOTE 18

		PRIMARY SILKSCREEN
		PRIMARY SOLDER MASK
NOMINAL		PRIMARY SIDE (LAYER 1)
FINISHED	ROGERS 4003C 8MILS	L2_GND PLANE (LAYER 2)
BOARD	ISOLA 370HR	L3_GND PLANE (LAYER 3)
THICKNESS	ISOLA 370HR	SECONDARY SIDE (LAYER 4)
0.062"		SECONDARY SOLDER MASK
+/- 10%		

CLIP BACK THE CENTER CONDUCTOR WITHIN 5 MILS FROM THE EDGE OF THE BOARD.

PLATED AREA
2 PLACES


DETAIL A

2

REQUIREMENTS:

1. REFER TO IPC-6010 SERIES (LATEST REV.), CLASS 2 FOR FABRICATION UNLESS OTHERWISE SPECIFIED.
2. ACCEPTABILITY PER ANALOG DEVICES, INC. SPECIFICATION TST00115, (LATEST REVISION.)
3. MODIFICATIONS TO THE ARTWORK ARE NOT ALLOWED WITHOUT WRITTEN AUTHORIZATION.
4. HOLE PATTERN TOLERANCES FOR UNDIMENSIONED HOLES SHALL BE A DIAMETER OF 0.005 INCHES FROM THEIR TRUE POSITION.
5. PLATED HOLE WALL THICKNESS SHALL NOT BE LESS THAN 0.001 INCH MINIMUM AVERAGE, WITH NO READING LESS THAN .0008 BY CROSS SECTION.
6. HOLE DIAMETERS APPLY AFTER PLATING.
7. FINISHED CONDUCTOR WIDTHS SHALL NOT BE REDUCED FROM THE NOMINAL INDICATED ON THE MASTER PATTERN, BY MORE THAN THE CONDUCTOR THICKNESS.
8. MINIMUM DESIGN LINE WIDTH IS 8 MILS.
9. MINIMUM DESIGN SPACING IS 7 MILS.
- ~~10. NON-FUNCTIONAL PAD REMOVAL FROM INNER SIGNAL LAYERS MAY BE PERFORMED AFTER CUSTOMER APPROVAL.~~
11. IF PAD SIZES PROVIDED ARE NOT LARGE ENOUGH TO MAINTAIN ANNULAR RING REQUIREMENT, MFGR. MAY REQUEST APPROVAL TO TEAR DROP PADS TO MAINTAIN ANNULAR RING. (AT PAD TO TRACE INTERSECTION ONLY AND ELECTRICAL INTEGRITY MUST BE MAINTAINED.)
12. THIEVING MAY BE ADDED TO COMPENSATE FOR LOW COPPER DENSITY AREAS ON THIS DESIGN ONLY AFTER REVIEW AND APPROVAL FROM THE CUSTOMER:
 - A. THIEVING TO CARD EDGE, FIDUCIALS, NON-PLATED THROUGH HOLES, ALL OTHER FEATURES TO BE 0.200 INCH MINIMUM.
 - B. THERE SHALL BE NO THIEVING IN ANY AREAS FREE OF SOLDER MASK OR INTERNAL COPPER PLANES.
13. MFGR. TO LEGIBLY ETCH OR STAMP/SCREEN WITH PERMANENT NON-CONDUCTIVE INK ON SECONDARY SIDE IN A CLEAR AREA UNLESS OTHERWISE INDICATED;
 - ~~A. U.L. CODE FLAMMABILITY RATING~~
 - B. DATE CODE (STAMP).
 - C. LOT NUMBER
 - D. MFGR LOGO
 - E. SUCCESSFUL ELECTRICAL TEST.
14. REPAIRS PER IPC-7711/21 (LATEST REV.) ARE ALLOWED.
15. INDICATED VIAS FILLED WITH NON-CONDUCTIVE EPOXY AND PLATED OVER. FLUSH TO .003" BELOW SUFACE BOTH SIDES PRIOR TO FINAL PLATING.
16. CRITICAL LINE WIDTH = 16 MILS +/- 1 MILS ADJUST PROCESS TO ACHIEVE WIDTH
17. BOARD TO HAVE EDGE PLATING AT CONNECTOR EDGE. ALL 4 METAL LAYERS MUST CONNECT.
18. THRU VIAS FILLED WITH NON-CONDUCTIVE EPOXY AND PLATED OVER

PRIMARY SIDE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES			APPROVAL		DATE		 ANALOG DEVICES		WWM DIVISION 804 WOBURN STREET WILMINGTON, MA 01887			
TOLERANCES			TEMPLATE ENGINEER N/A		N/A							
DECIMALS FRACTIONS ANGLES .XX --.010 --1/32 -- 2 .XXX --.005 .XXXX --.0050			HARDWARE SERVICES M.VALE		17 JUN21		TITLE FABRICATION ADL8107 CUSTOMER EVALUATION Z					
MATERIAL			HARDWARE SYSTEMS N/A		N/A							
			TEST ENGINEER N/A		N/A							
			COMPONENT ENGINEER M.YAN		17 JUN21							
			TEST PROCESS N/A		N/A							
FINISH			HARDWARE RELEASE K.JABATAN		17 JUN21		SIZE FSCM NO DRAWING NUMBER REV C 24355 09-068109 A					
			DESIGNER S.NODADO		17 JUN21							
			PTD ENGINEER P.COCHANGCO		17 JUN21							
DO NOT SCALE DWG			CHECKER N/A		N/A		SCALE 1/1			SHEET 1 OF 1		

ANALOG
DEVICES

WWM
DIVISION
804 WOBURN STREET
WILMINGTON, MA 01887

TITLE FABRICATION
ADL8107
CUSTOMER EVALUATION Z

SIZE

FSCM NO

DRAWING NUMBER

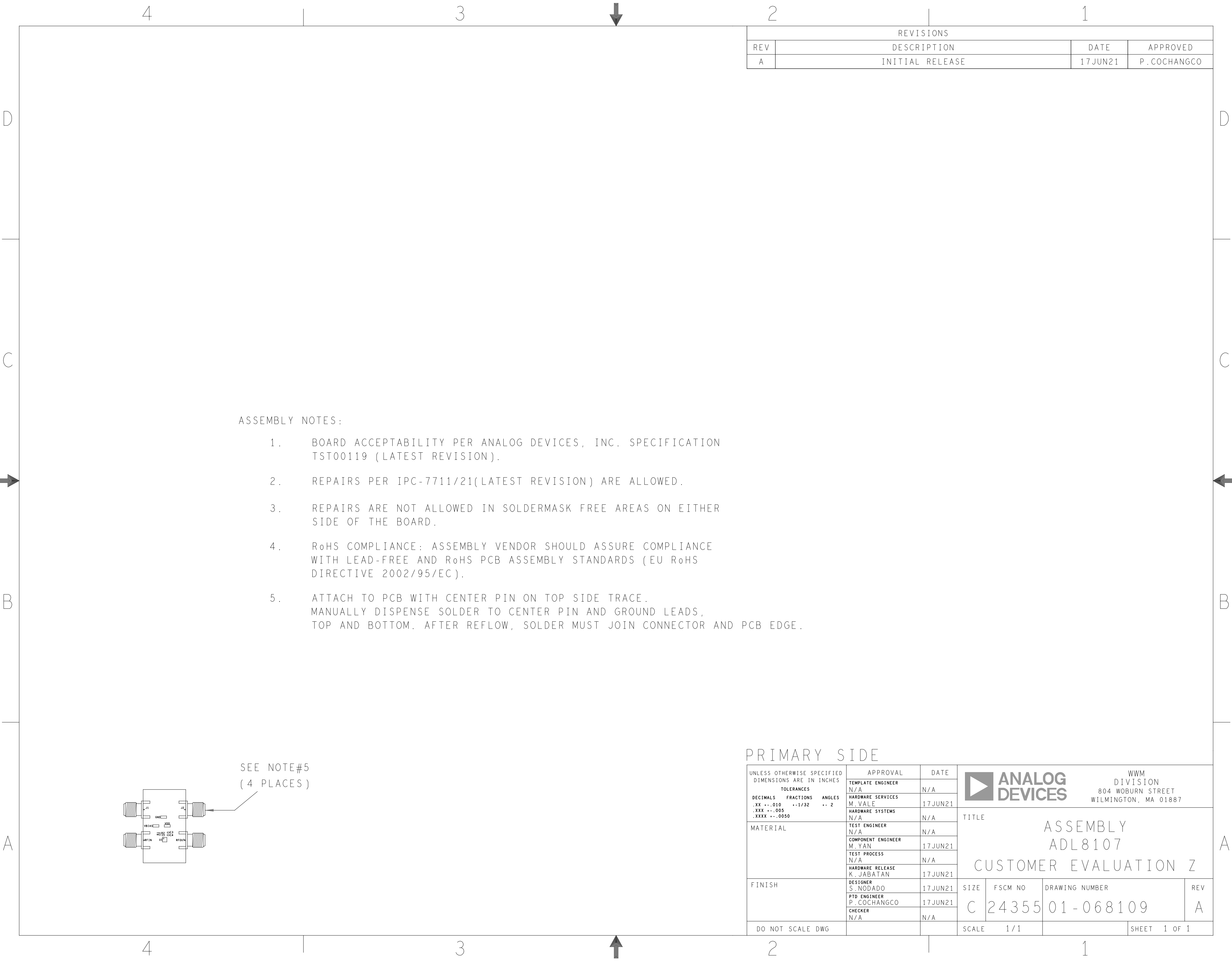
REV

SCAL

1 / 1

SHEE

SHEET 1 OF 1




ASSEMBLY NOTES:

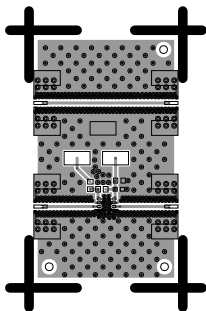
- 1. BOARD ACCEPTABILITY PER ANALOG DEVICES, INC. SPECIFICATION TST00119 (LATEST REVISION).
- 2. REPAIRS PER IPC-7711/21(LATEST REVISION) ARE ALLOWED.
- 3. REPAIRS ARE NOT ALLOWED IN SOLDERMASK FREE AREAS ON EITHER SIDE OF THE BOARD.
- 4. RoHS COMPLIANCE: ASSEMBLY VENDOR SHOULD ASSURE COMPLIANCE WITH LEAD-FREE AND RoHS PCB ASSEMBLY STANDARDS (EU RoHS DIRECTIVE 2002/95/EC).
- 5. ATTACH TO PCB WITH CENTER PIN ON TOP SIDE TRACE. MANUALLY DISPENSE SOLDER TO CENTER PIN AND GROUND LEADS, TOP AND BOTTOM. AFTER REFLOW, SOLDER MUST JOIN CONNECTOR AND PCB EDGE.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	17JUN21	P.COCHANGCO

PRIMARY SIDE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES			APPROVAL		DATE		<div><div></div><div>ANALOG DEVICES</div></div> <div>WWM DIVISION 804 WOBURN STREET WILMINGTON, MA 01887</div>							
TOLERANCES			TEMPLATE ENGINEER N/A		N/A									
DECIMALS FRACTIONS ANGLES .XX -.010 --1/32 -- 2 .XXX -.005 .XXXX -.0050			HARDWARE SERVICES M.VALE		17JUN21									
			HARDWARE SYSTEMS N/A		N/A									
MATERIAL			TEST ENGINEER N/A		N/A		TITLE ASSEMBLY ADL8107 CUSTOMER EVALUATION Z							
			COMPONENT ENGINEER M.YAN		17JUN21									
			TEST PROCESS N/A		N/A									
			HARDWARE RELEASE K.JABATAN		17JUN21									
FINISH			DESIGNER S.NODADO		17JUN21		SIZE C		FSCM NO 24355		DRAWING NUMBER 01-068109		REV A	
			PTD ENGINEER P.COCHANGCO		17JUN21									
			CHECKER N/A		N/A									
DO NOT SCALE DWG							SCALE		1 / 1				SHEET 1 OF 1	

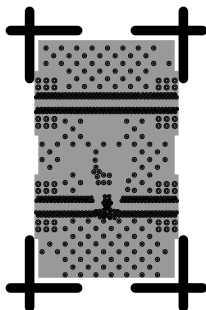
L1 PRIMARY
08-068109-01
REV A



L2 GND

08-068109-06

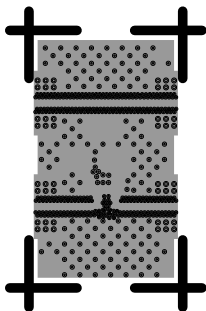
REV A



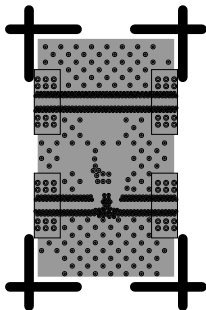
L3 GND

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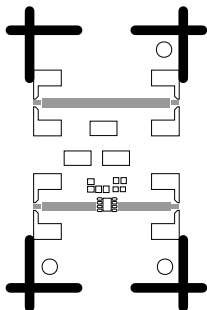
REV A



L4 SECONDARY
08-068109-02
REV A



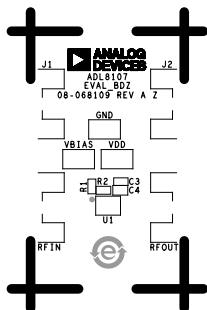
SOLDERMASK PRIMARY
08-068109-04
REV A



SILKSCREEN PRIMARY

08-068109-03

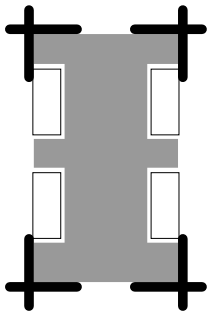
REV A



SOLDERMASK SECONDARY

08-068109-05

REV A



PASTEMASK PRIMARY

08-068109-08

REV A

