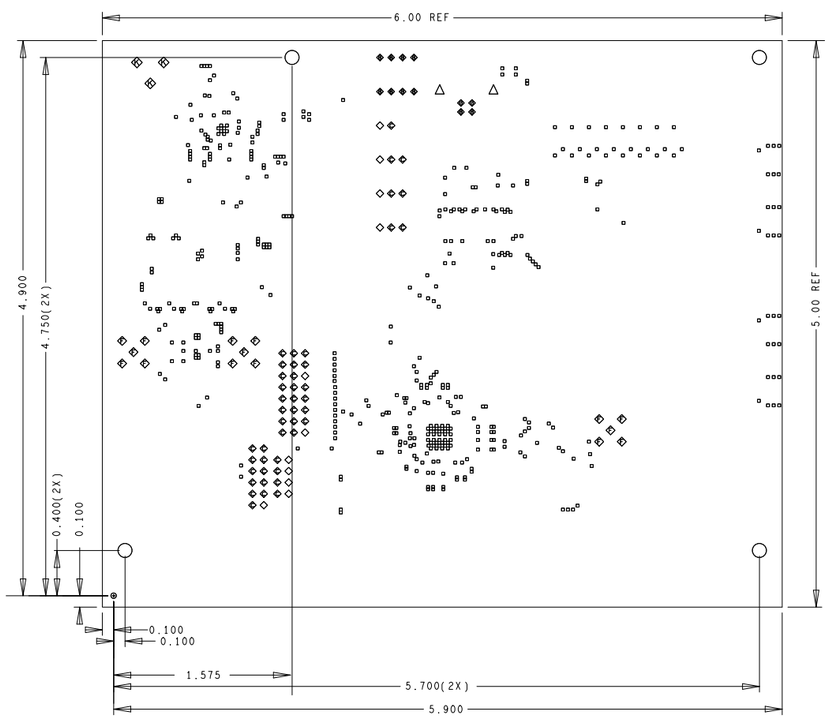
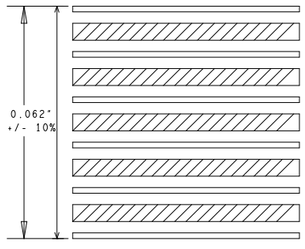
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE		





TOP LAYER 1.5 oz cu. FINISHED
FR4-106 0.0062"
LAYER 02 1 oz cu.
FR4-106 0.003"
LAYER 03 1 oz CU.
FR4-106 0.0336"CORE FILLER
LAYER 04 1 oz cu.
FR4-106 0.003"
LAYER 05 1 oz cu.
FR4-106 0.0062"
BOTTOM LAYER 1.5 oz cu. FINISHED

DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILS			
FIGURE	SIZE	PLATED	QTY
▫	8.0	PLATED	472
⊕	13.0	PLATED	1
	16.0	PLATED	32
◈	40.0	PLATED	12
◇	45.0	PLATED	11
◈	45.0	PLATED	44
◈	60.0	PLATED	15
◈	75.0	PLATED	3
△	90.0	PLATED	2
◯	125.0	NON-PLATED	4
		TOTAL HOLES:	596

PCB INFORMATION:

Board Size: Refer to Drill drawing/dimension drawing
Drill Table: Refer to Drill drawing/dimension drawing
Number of Holes: 596
Number of Layers: 6
Artwork Format: Gerber 274X 2.5 Absloute Leading Zero Suppressed
NC DrillFormat: Excellon 2.5 Absloute Leading Zero Suppressed
Electrical Test: All cards to be tested for open and shorts
ICP-D-356 netlsir provided.
Surface Finish: (indicate choice with an X)

__X__ Alternate Silver Immersion Plating

Soldermask: Liquid Photo-Imageable, BLUE, Gloss

Silkscreen: White Epoxy base ink

Other Marking: PCB and (customer supplied) impedance test coupon to be marked with:
- Fabricator's name or logo
- date code showing calendar year and week (YY/WW)
- PCB part number on test coupon for traceability

CONTROLLED IMPEDANCE:

Target Impedance: Stripline 50 Ohms +/- 10% Diffrential Pair 100 Ohms +/-10%
Data supplied with desired final trace width.
Adjustment for etchback to be done by PCB fabricator.
Finished trace width: 0.010" +-/- 0.001" Stripline 0.00475" +/- 0.001"
Trace Location: Layer L01 (Top) Referenced to L02.

OTHER NOTES:

1. Unless otherwise noted, fabrication methods shall comply with ANSI/IPC standards
2. Any change to artworks must be approved in writing.
3. Tear-dropping permitted by PCB Fabricator to improve reliability.
4. Data is nominal and may be adjusted to compensate for etch tolerances.
5. Inside radii, inside notches, slots, cut-offs, unless otherwise specified, to be .062R +/-2 degrees.
6. Information in drill file takes preference if conflicting drill information exists.
7. All holes are finished holes sizes. Hole diameter and location tolerance to be +/- 0.003" unless otherwise specified.
8. All 0.125" tooling holes are non-plated with tolerance of +0.002" / -0.000" unless otherwise stated.
9. Via drill size may be reduced if required to prevent break-out.
10. Minimum copper plating in holes to be .001"
11. Solder mask thickness shall not exceed height of exposed pads including surface finish.
12. Solder mask overlap is permitted on via lands
13. Solder mask overlap shall not exceed .001" on circular lands other than vias.
14. No solder mask overlap permitted on SMD lands, unless otherwise state

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS FRACTIONS ANGLES
.XX +-.010 +-1/32 +/-2
.XXX +-.005

ANALOG DEVICES
TMIC DIVISION
831 WOBURN STREET
WILMINGTON, MA 01887

APPROVAL	DATE
DRAWN BY R.L.O.	02/13/2009
DESIGNED	
CHECKED	
APPROVED	
MFG ENGINEER	

TITLE FABRICATION DRAWING
AD9547CE01A CUSTOMER EVAL BOARD
AD9547/PCBZ

SIZE	FSCM NO	DRAWING NUMBER	REV
B		09-041732	A

DO NOT SCALE DWG | SCALE NONE | SHEET 1 OF 1