



FINISHED HOLES IN MILS				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	PLATED	QTY	TOLERANCE/NOTES
•	8.0	PLATED	64	
□	13.0	PLATED	1	
•	16.0	PLATED	84	
○	50.0	PLATED	4	
○	63.0	PLATED	1	
◇	125.0	NON-PLATED	4	

PCB INFORMATION:

Board Size: Drill Table: Refer FABRICATION DRAWING
Number of Holes: 158
Number of Layers: 4
Artwork Format: Gerber 274X 2.5 Absolute Leading Zero Suppressed
NC DrillFormat: Excellon 2.5 Absolute Leading Zero Suppressed
Electrical Test (opens and shorts) Required ICP-D-356 Neltist provided.
Surface Finish: (indicate choice with an X)
XX Standard (ENIG)- Electroless Ni (120-200u inch);Immersion Gold (3-8u inch)
____ Alternate (HASL) - Tin/Lead Plating
Soldermask: Liquid Photo-Imageable, BLUE, Gloss
Silkscreen: White Epoxy base ink
Other Marking: PCB to be marked with:
- Fabricator's name or logo
- date code showing calendar year and week (YY/WW)
- PCB part number on test coupon for traceability

CONTROLLED IMPEDANCE:

Target Impedance: 50 Ohms +/- 10% and 100 Ohms +/- 10%
Data supplied with desired final trace width.
Adjustment for etchback to be done by PCB fabricator.
IMPEDANCE CONTOLL: LAYER L01 REFERENCED TO LAYER L02
TRACE WIDTHS OF 0.0067 ARE 50 ohm SINGLE ENDED
TRACE WIDTHS OF 0.0045 ARE 100 ohm DIFFERENTIAL.

OTHER NOTES:

- Unless otherwise noted, fabrication methods shall comply with ANSI/IPC standards
- Any change to artworks must be approved in writing.
- Tear-dropping permitted by PCB Fabricator to improve reliability.
- Data is nominal and may be adjusted to compensate for etch tolerances.
- Inside radii, inside notches, slots, cut-offs, unless otherwise specified, to be .062R +/-2 degrees.
- Information in drill file takes preference if conflicting drill information exists.
- All holes are finished holes sizes. Hole diameter and location tolerance to be +/- 0.003" unless otherwise specified.
- All 0.125" tooling holes are non-plated with tolerance of +0.002" / -0.000" unless otherwise stated.
- Via drill size may be reduced if required to prevent break-out.
- Minimum copper plating in holes to be .001"
- Solder mask thickness shall not exceed height of exposed pads including surface finish.
- Solder mask overlap is permitted on via lands
- Solder mask overlap shall not exceed .001" on circular lands other than vias.
- No solder mask overlap permitted on SMD lands, unless otherwise state

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS FRACTIONS ANGLES
.XX +/- .010
.XXX +/- .005 +/- 1/32 +/- 2



ANALOG DEVICES
TMIC DIVISION
831 WOBURN STREET
WILMINGTON, MA 01887

APPROVAL	DATE
DRAWN BY R.L.O.	03/13/2009
DESIGNED	
CHECKED	
APPROVED	
MFG ENGINEER	

TITLE FABRICATION DRAWING			
SIZE C	FSCM NO	DRAWING NUMBER FAB-ADCLK946CE01	REV B
DO NOT SCALE DWG		SCALE NONE	SHEET 1 OF 1