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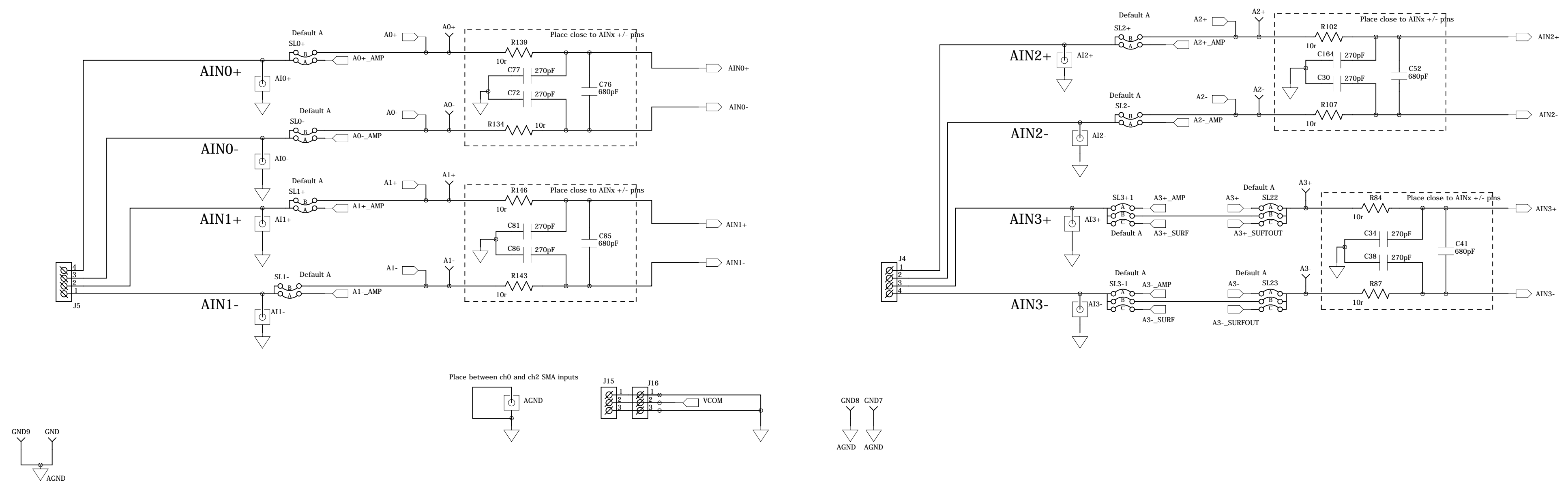
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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

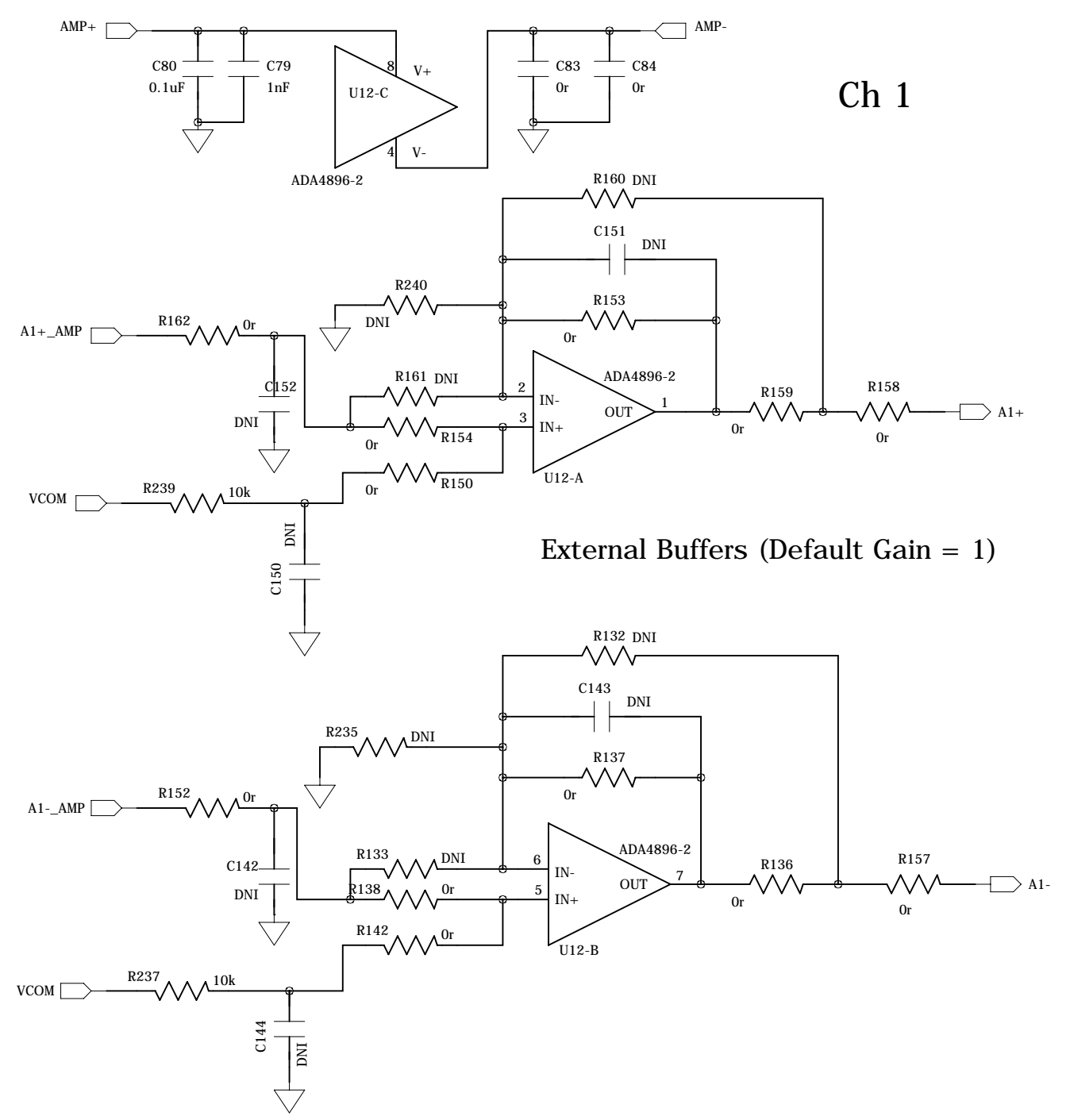
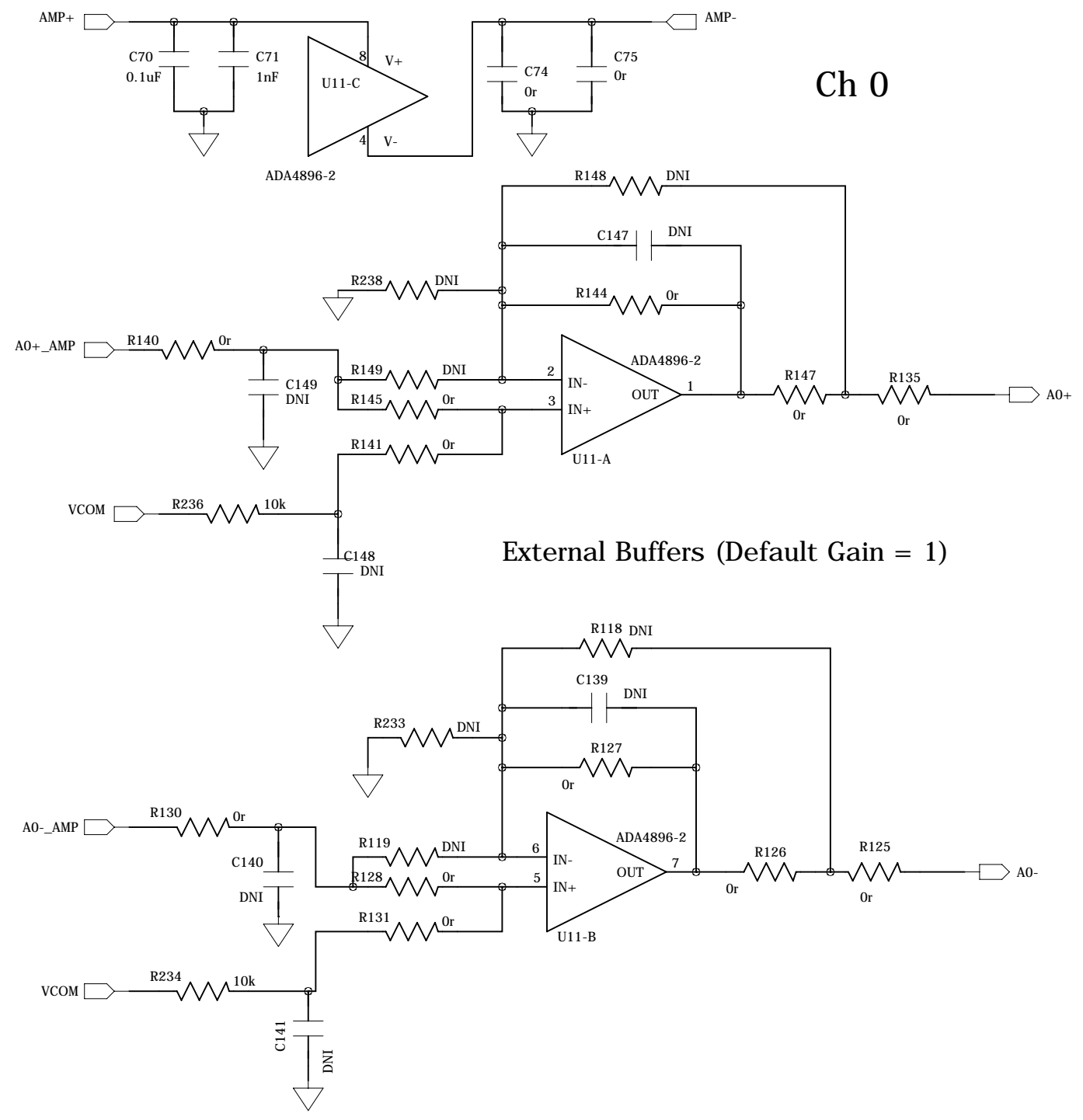
Analog Inputs

Solder Link Connections:
 A: Buffered input (Default)
 B: Direct to ADC Input pins
 C: Route through Amplifier Mezzanine Card (AMC) for Alternative Amplifier Evaluation (Ch 3 ONLY)



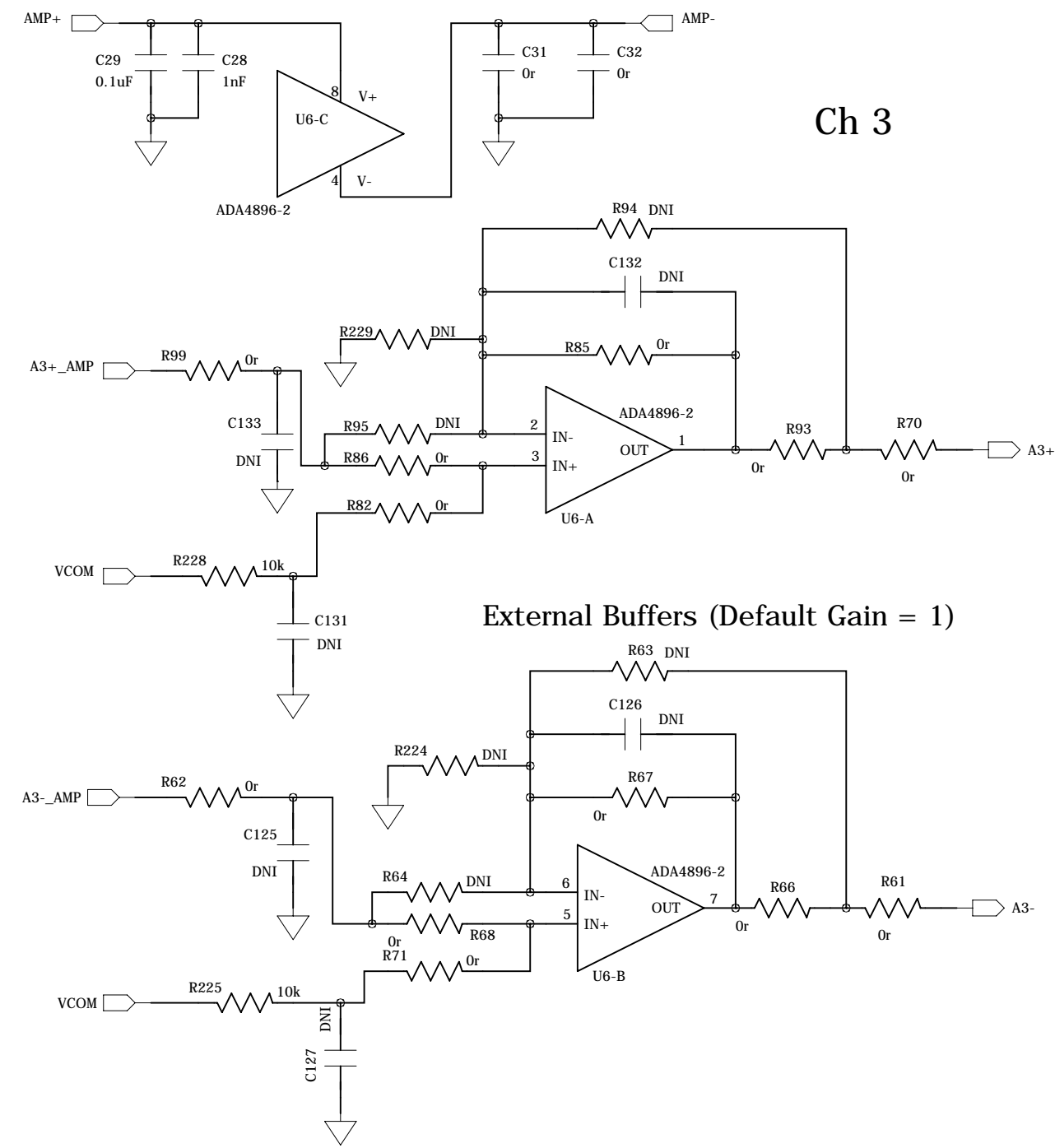
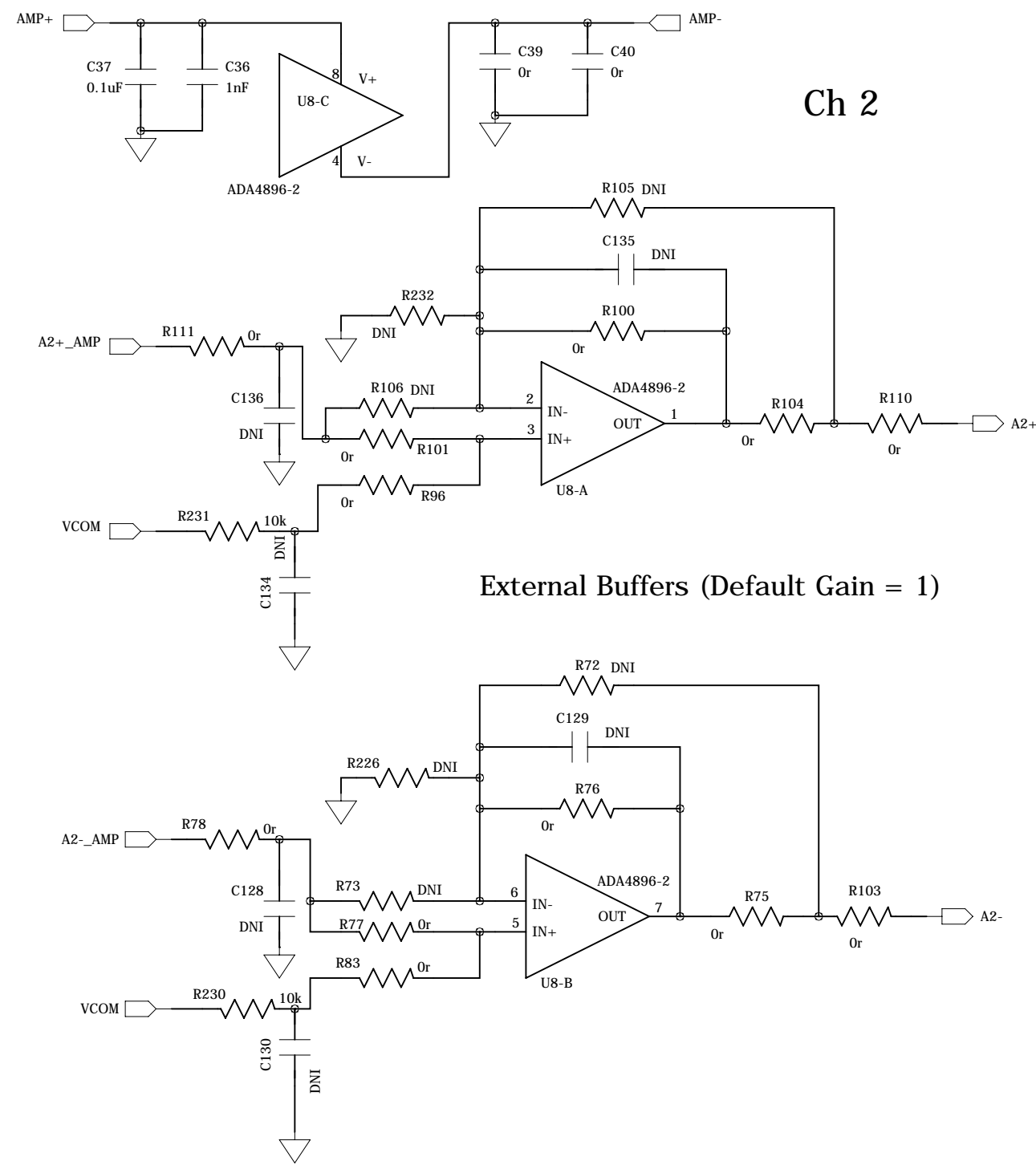
COMPANY:				Analog Devices			
TITLE:				EVAL-AD7768-4FMCZ			
DRAWN:	ROB FINNERTY	DATED:		CODE:	SIZE:	DRAWING NO:	REV:
CHECKED:	<Checked By>	DATED:		<Code>	A2	02-0	A
QUALITY CONTROL:	<QC By>	DATED:	<QC Date>				
RELEASED:	<Released By>	DATED:	<Release Date>				

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY:				Analog Devices			
TITLE:				EVAL-AD7768-4FMCZ			
DRAWN:	Rob Finnerty	DATED:	24/11/2014	CODE:	SIZE:	DRAWING NO:	REV:
CHECKED:	<Checked By>	DATED:	24/11/2014	<Code>	A2	02-0	A
QUALITY CONTROL:	<QC By>	DATED:	<QC Date>	SCALE: <Scale>		SHEET: 2 OF 7	
RELEASED:	<Released By>	DATED:	<Release Date>				

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



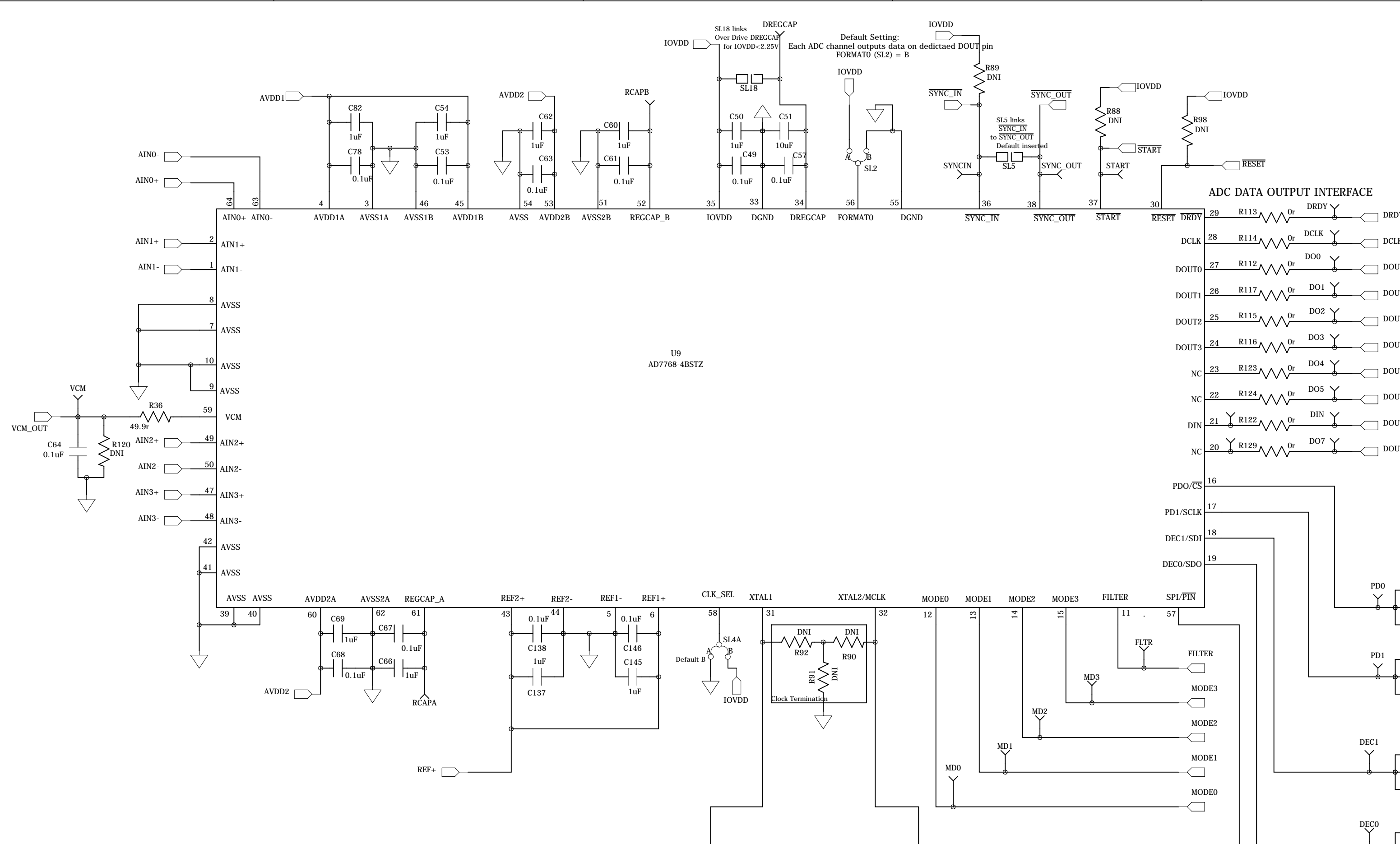
COMPANY: **Analog Devices**

TITLE: **EVAL-AD7768-4FMCZ**

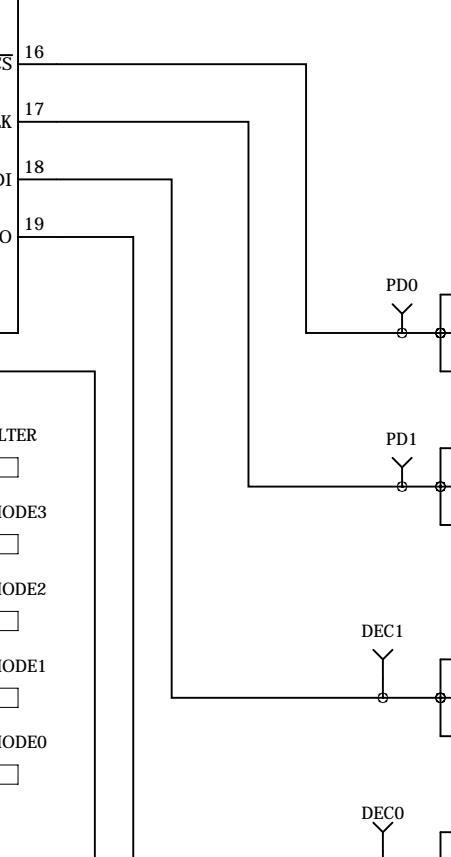
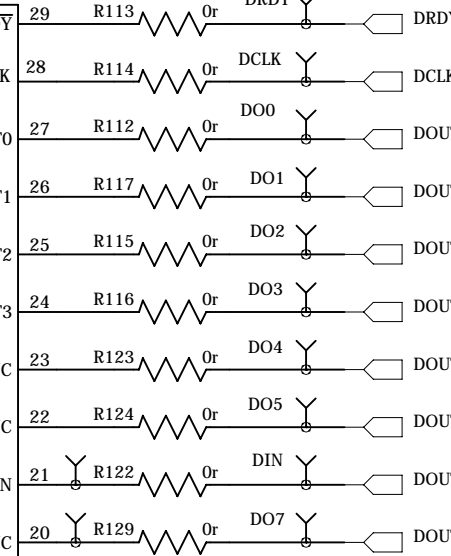
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CHECKED: <Checked By>	DATED: 24/11/2014
QUALITY CONTROL: <QC By>	DATED: <QC Date>
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<Code>	A2	02-0	A

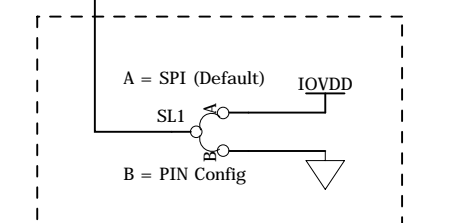
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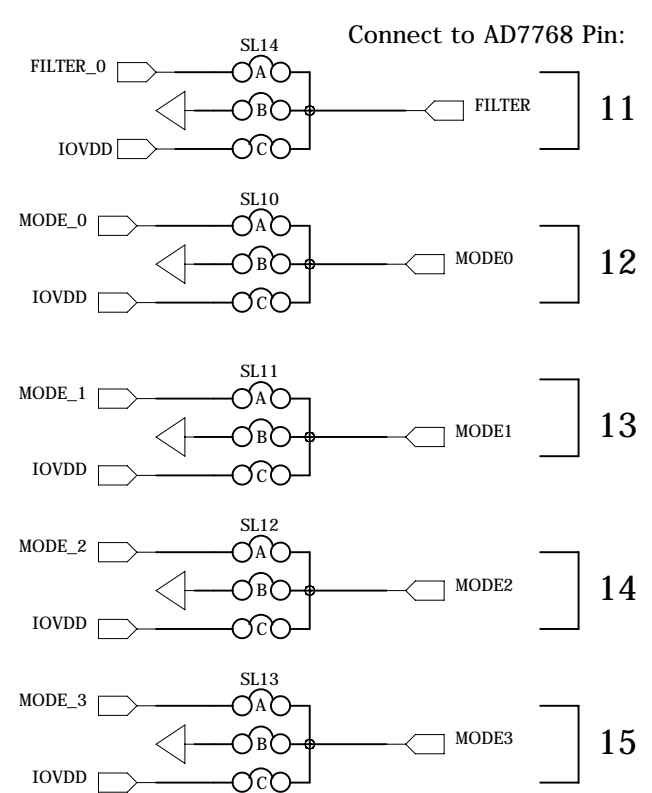
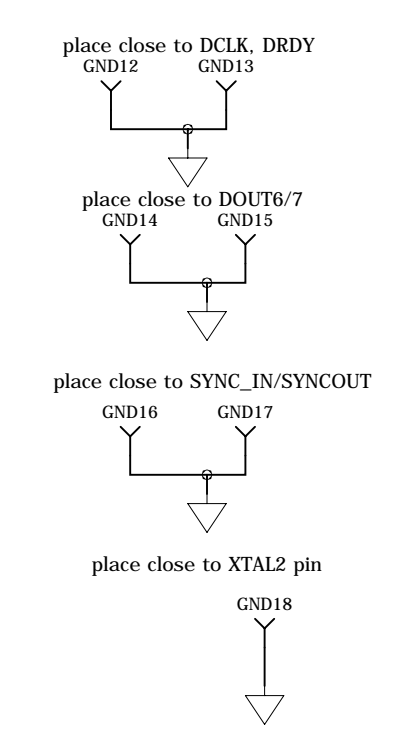
ADC DATA OUTPUT INTERFACE



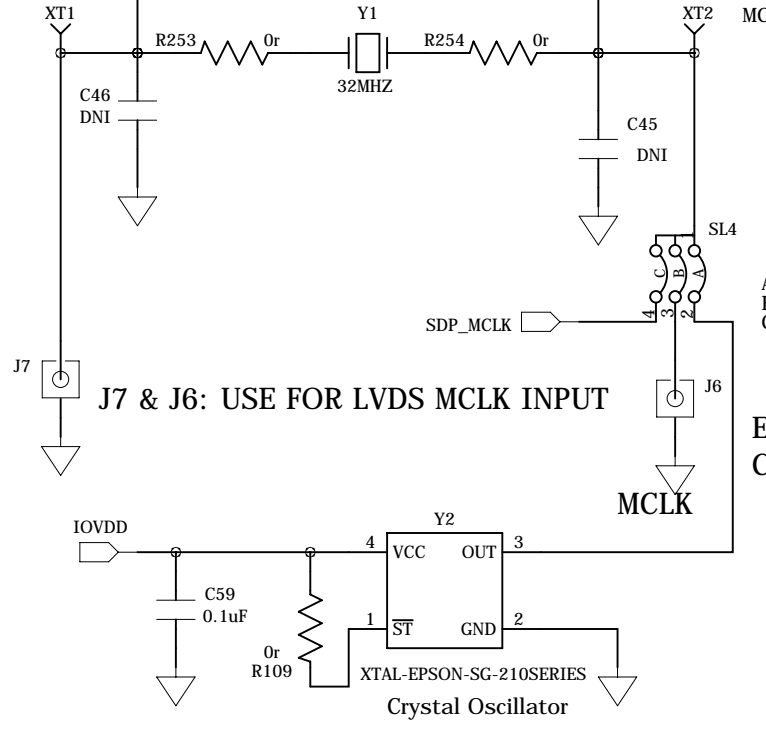
*FOR PIN CONTROL: SETTING TO B or C CONTROLS DEC RATE AND POWER DOWN FUNCTIONS



SL4 SETS AD7768 FOR PIN OR SPI CONTROL DEFAULTED TO SPI CONTROL



PIN Configuration: Mode and Filter Connections
 A = SDP GPIO Control
 B = GND: PIN CONFIG LOOKUP TABLE
 C = IOVDD: PIN CONFIG LOOKUP TABLE



A: Crystal Oscillator (Default)
 B: External CMOS/LVDS Clock
 C: MCLK from Blackfin TMR_A

J7 & J6: USE FOR LVDS MCLK INPUT
 EXT CMOS

DRAWN: Rob Finnerty	DATED: 24/11/2014
CHECKED: <Checked By>	DATED: 24/11/2014
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>

COMPANY: Analog Devices			
TITLE: EVAL-AD7768-4FMCZ			
CODE: <Code>	SIZE: A2	DRAWING NO: 02-0	REV: A
SCALE: <Scale>			SHEET: 4 OF 7

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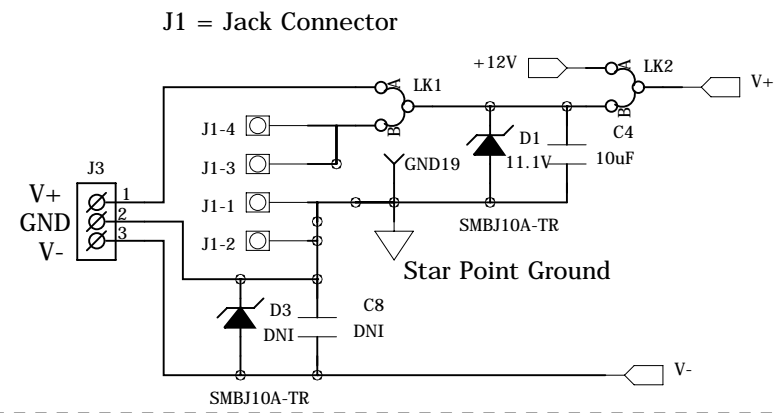
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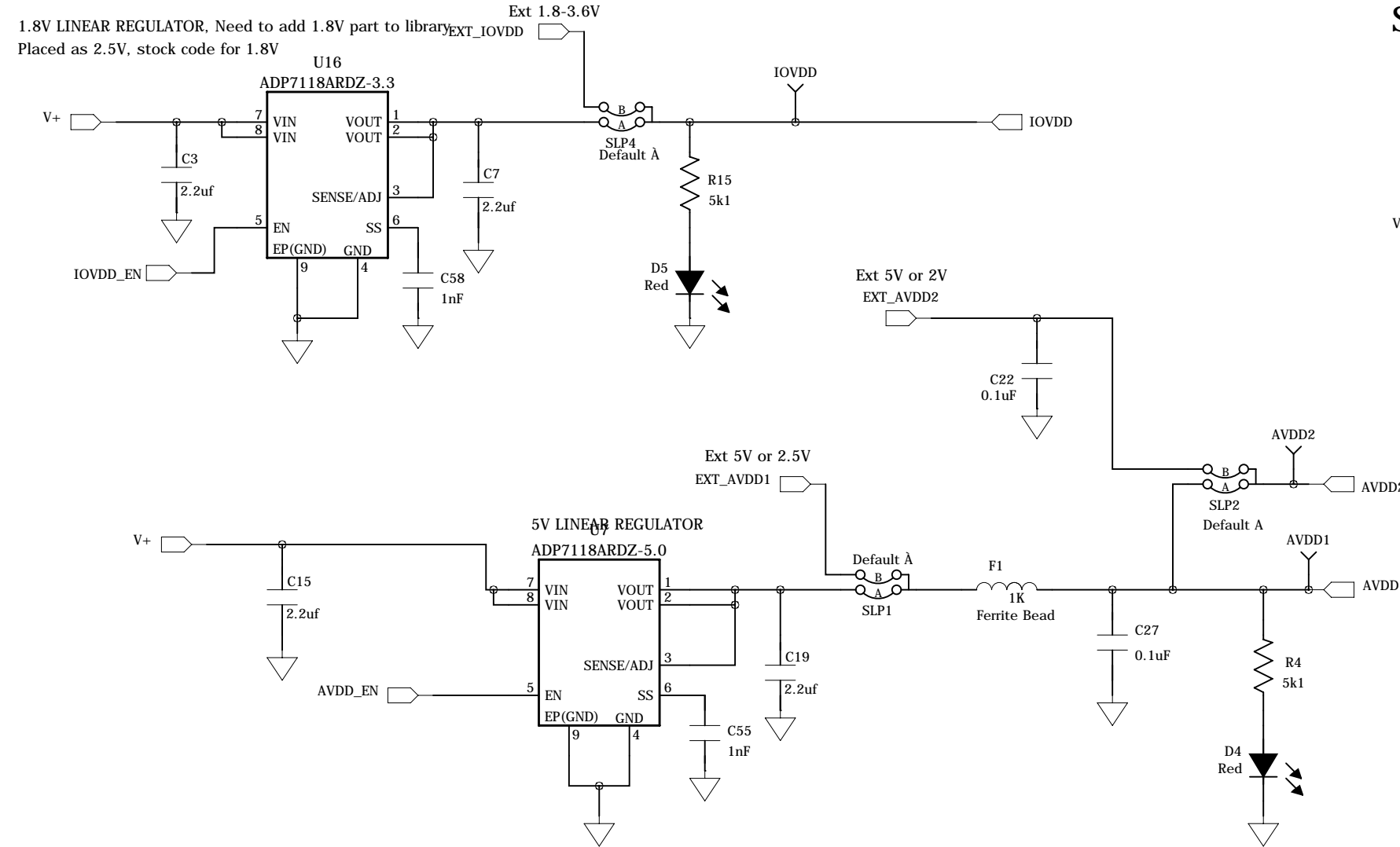
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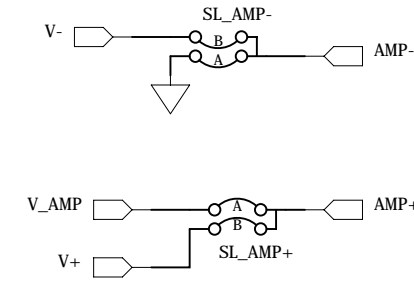
POWER SUPPLY : Jack or Bench Connection



5V, 1.8V Regulators

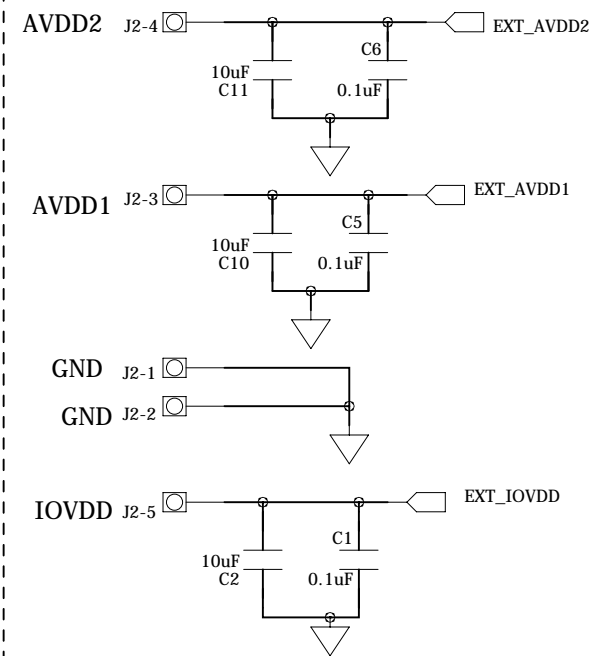


Select Amplifier Rails

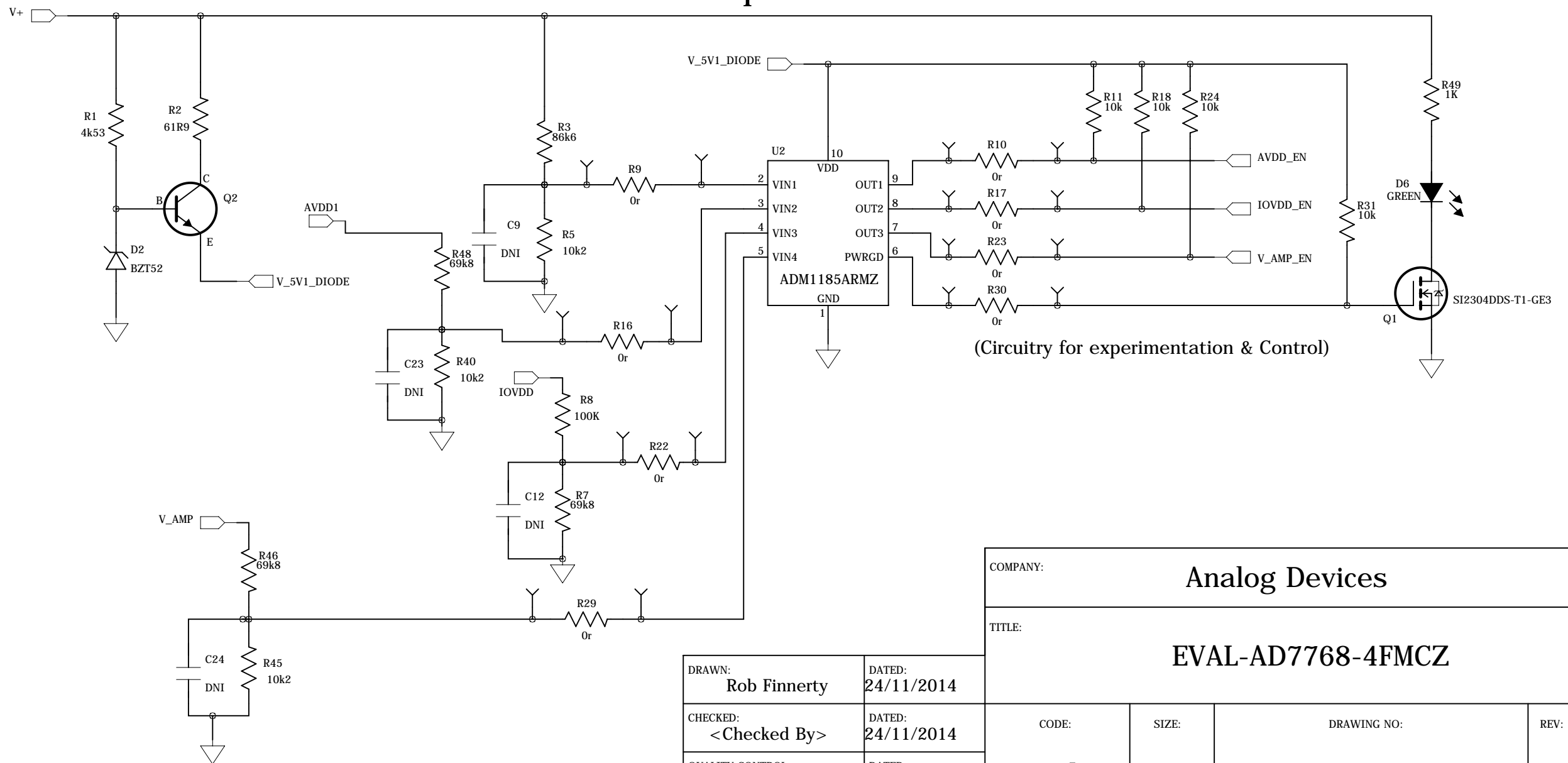


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LTR	ECO NO:	APPROVED:	DATE:

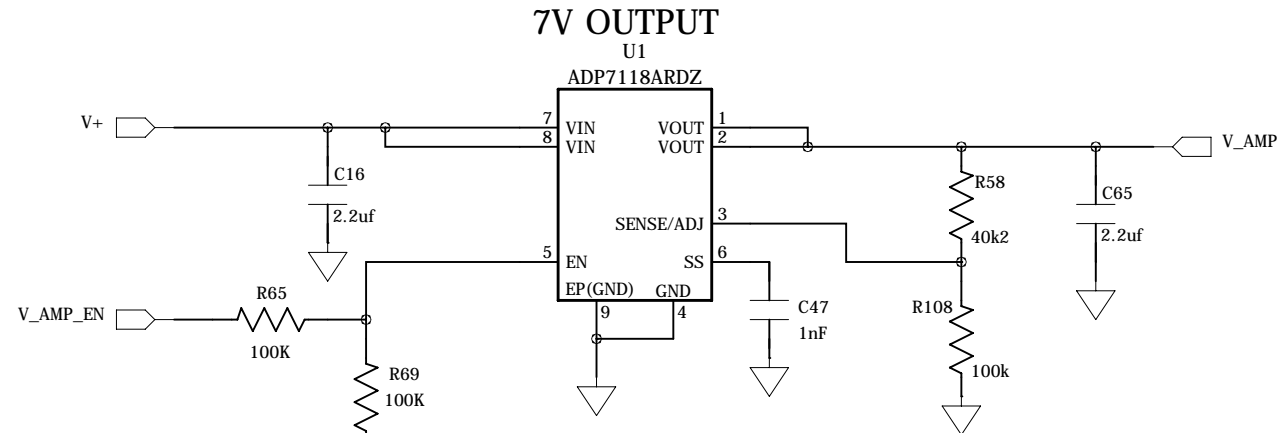
External supply: Stand-Alone Operation



Power Sequence Control



Amplifier and Reference Supply



COMPANY: Analog Devices			
TITLE: EVAL-AD7768-4FMCZ			
CODE: <Code>	SIZE: A2	DRAWING NO: 02-0	REV: A
SHEET: 5 OF 7			

DRAWN: Rob Finnerty	DATED: 24/11/2014
CHECKED: <Checked By>	DATED: 24/11/2014
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>

D

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B

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D

C

B

A

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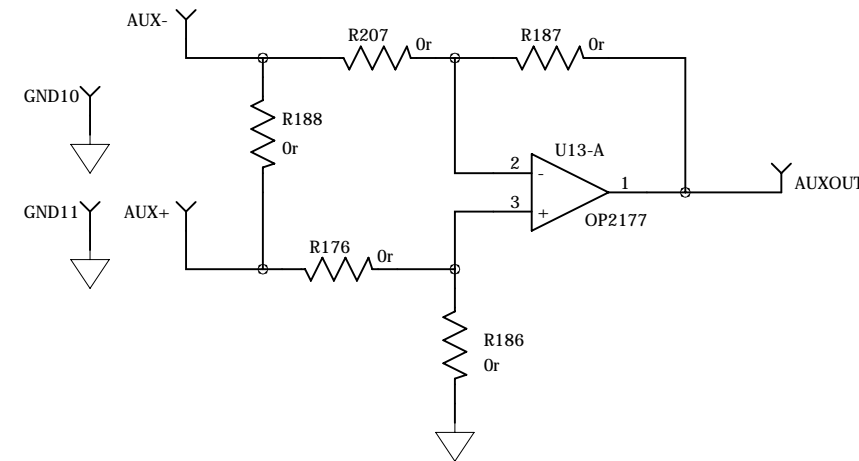
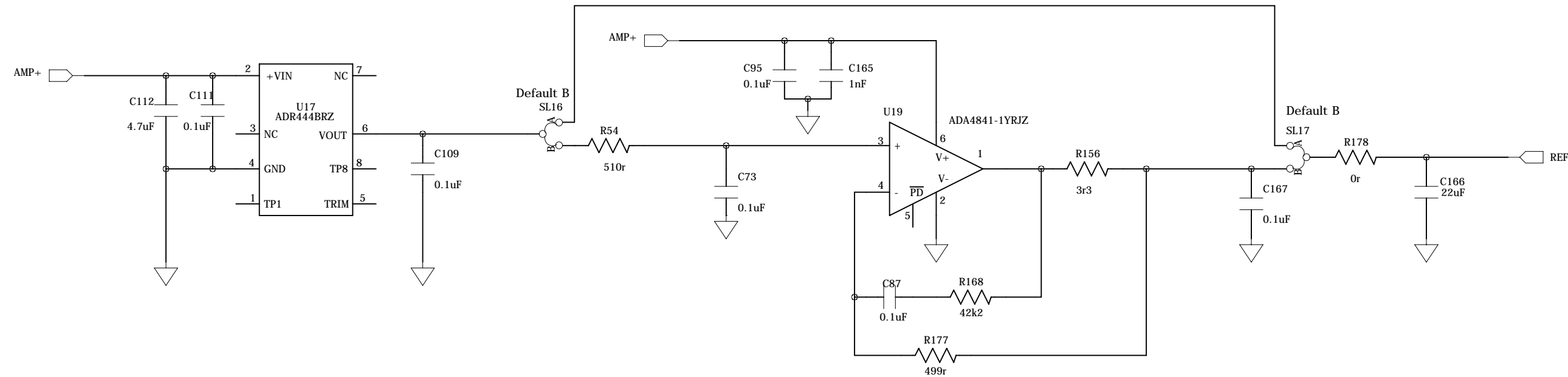
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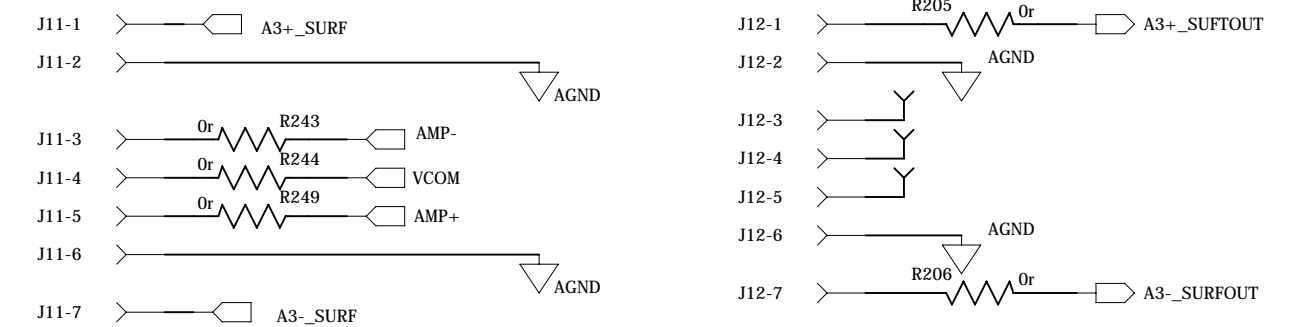
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Precision Voltage Reference

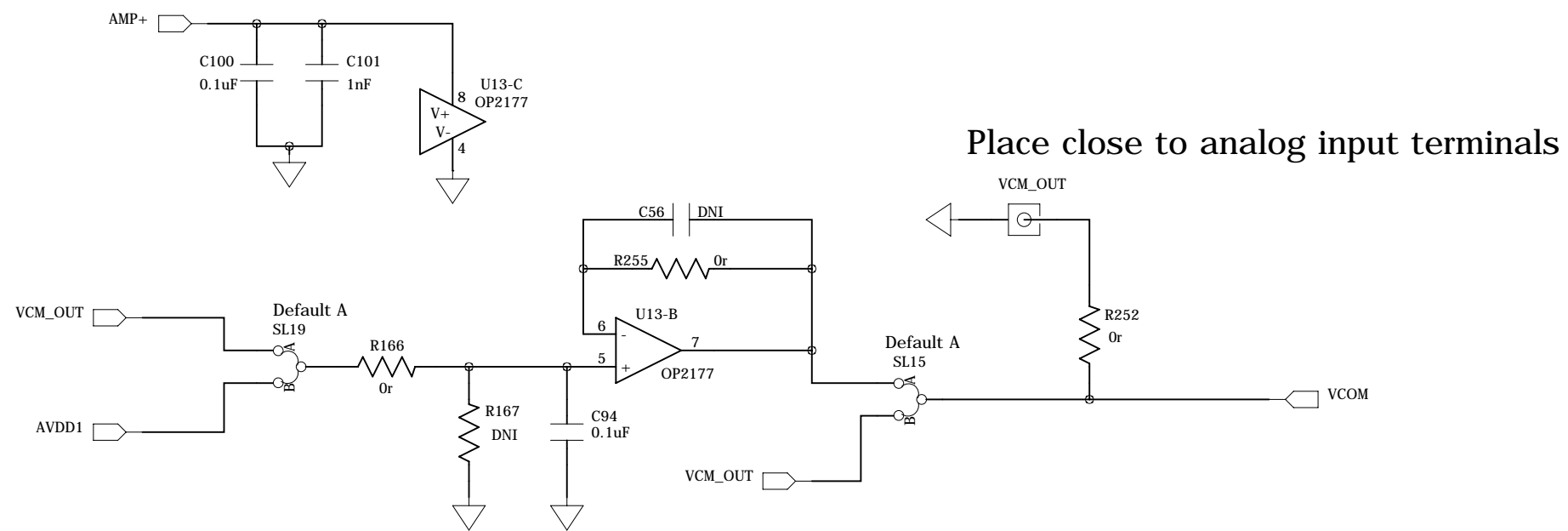
REFERENCE BUFFER ADA4841-1



OPTIONAL HEADER CONNECTOR (AMC for Ch3)



Creating VCOM - Common Mode for ADC Analog Inputs



Place close to analog input terminals

COMPANY: **Analog Devices**

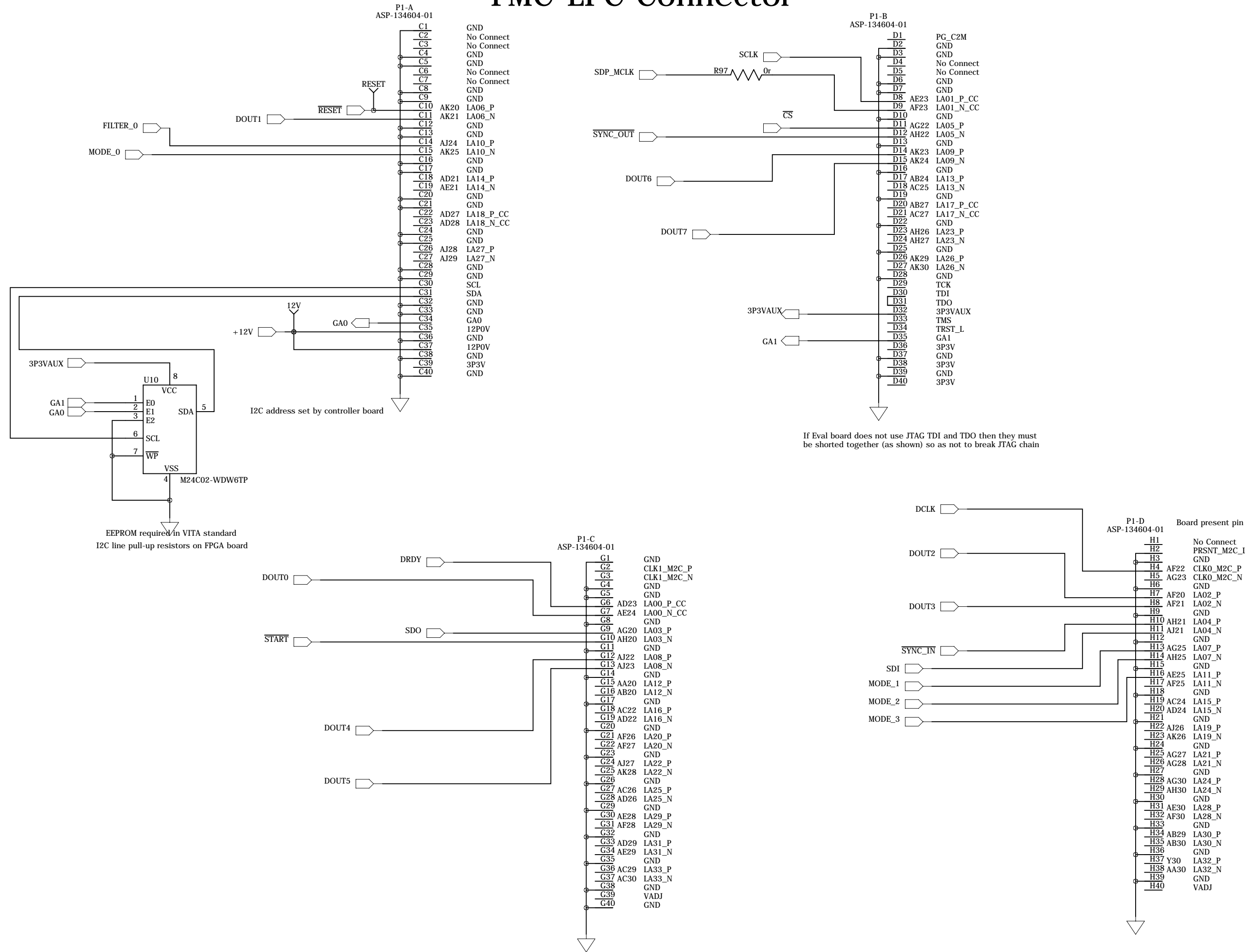
TITLE: **EVAL-AD7768-4FMCZ**

DRAWN: Rob Finnerty	DATED: 24/11/2014
CHECKED: <Checked By>	DATED: 24/11/2014
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>

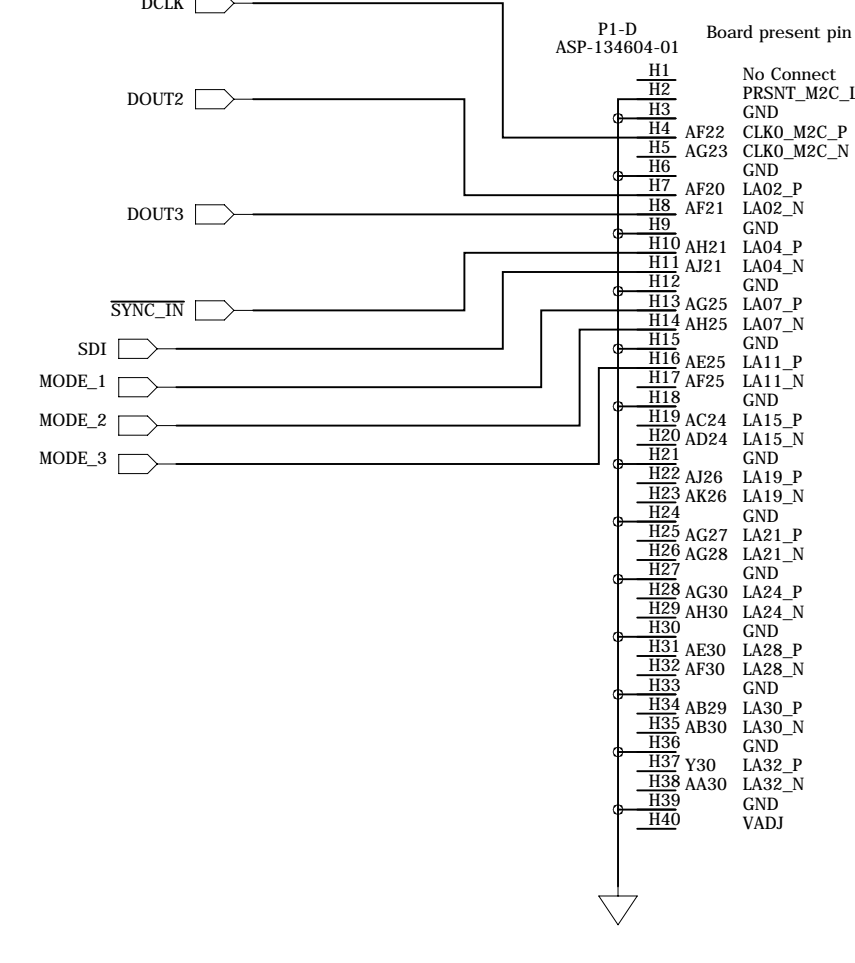
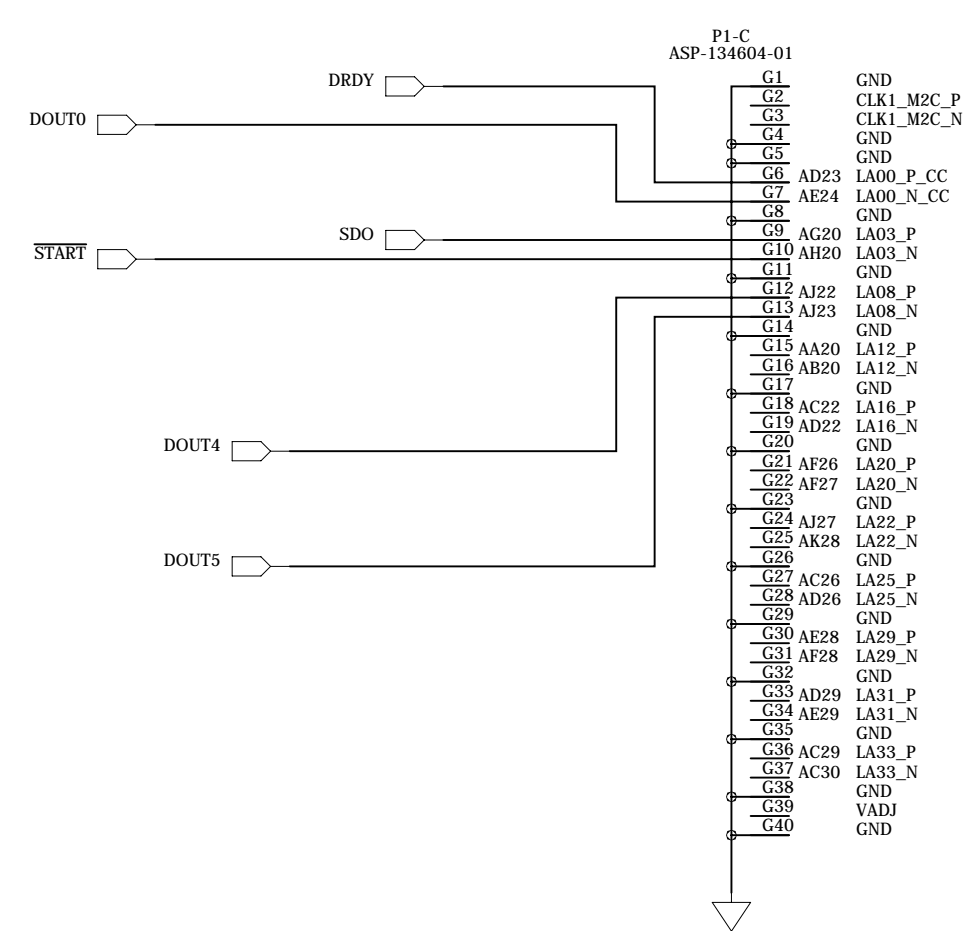
CODE:	SIZE:	DRAWING NO:	REV:
<Code>	A2	02-0	A

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

FMC-LPC Connector



EEPROM required in VITA standard I2C line pull-up resistors on FPGA board



COMPANY: Analog Devices			
TITLE: EVAL-AD7768-4FMCZ			
DRAWN: Rob Finnerty	DATED: 24/11/2014	CODE:	SIZE: A2
CHECKED: <Checked By>	DATED: 24/11/2014	DRAWING NO: 02-0	REV: A
QUALITY CONTROL: <QC By>	DATED: <QC Date>	SCALE: <Scale>	SHEET: 7 of 7
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