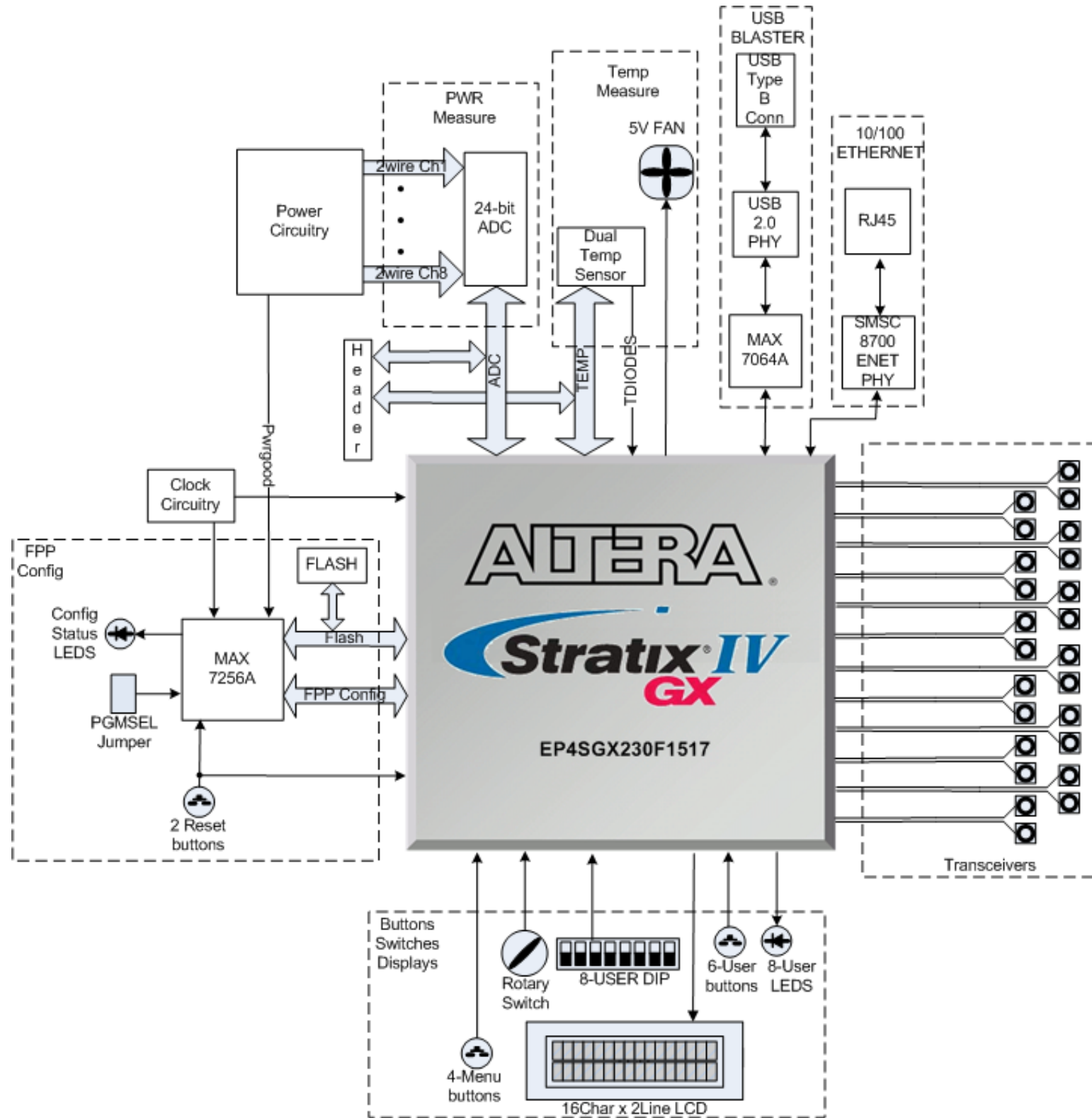


Stratix IVGX F1517 SI Evaluation Board Block Diagram

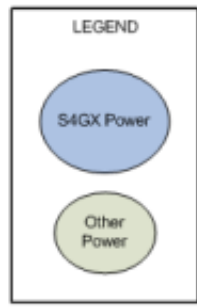
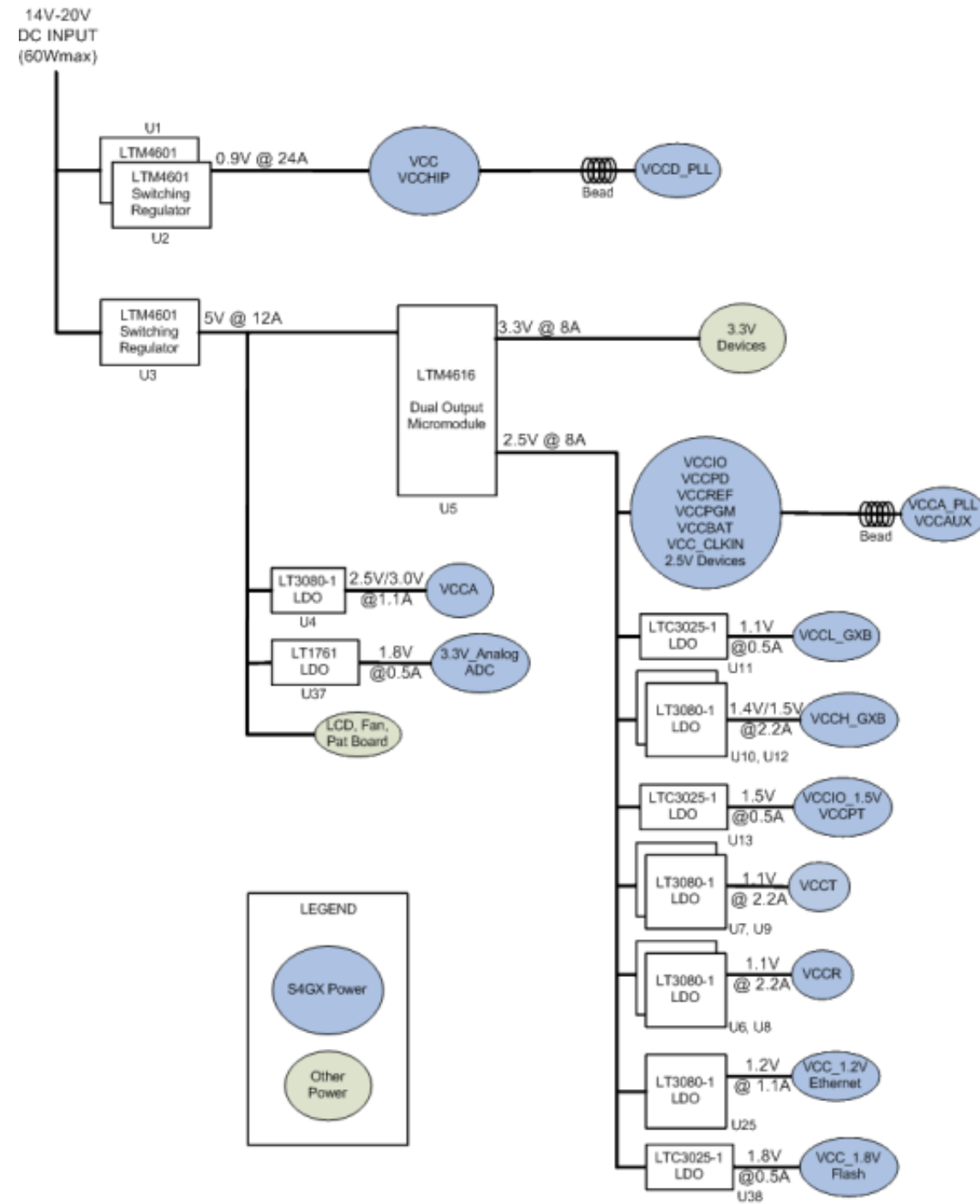


REV	DATE	PAGES	DESCRIPTION

PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Revision History
2	S4GX FPGA Package Top
3	Power 1
4	Power 2
5	Power 3
6	Power 4
7	Power 5
8	Power Measure
9	Temp Measure, PaT Header
10	USB Blaster
11	Global Clocks
12	Transceiver Clocks
13	MAX FPP Configuration
14	Flash
15	Button, Switches, LEDs
16	JTAG Chain
17	10/100 Ethernet
18	Transceiver Channels 1
19	Transceiver Channels 2
20	Stratix IVGX Configuration
21	Stratix IVGX Banks 1 & 2
22	Stratix IVGX Banks 3 & 4
23	Stratix IVGX Banks 5 & 6
24	Stratix IVGX Banks 7 & 8
25	Stratix IVGX Power
26	Decoupling 1
27	Decoupling 2



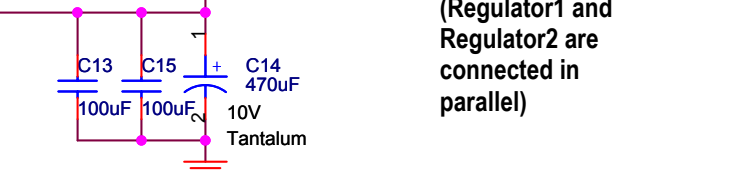
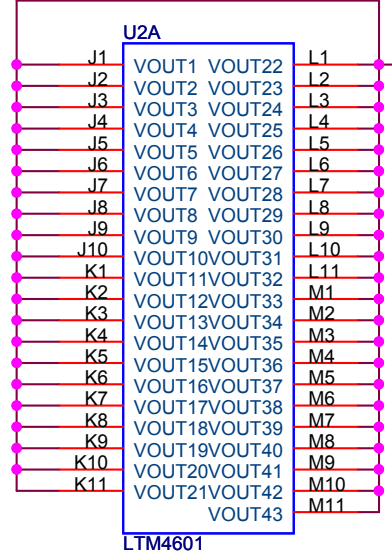
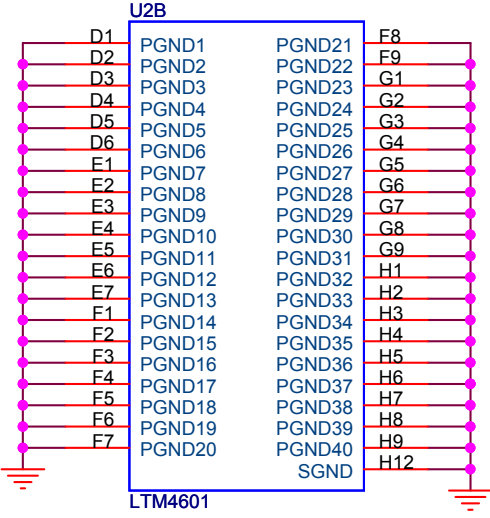
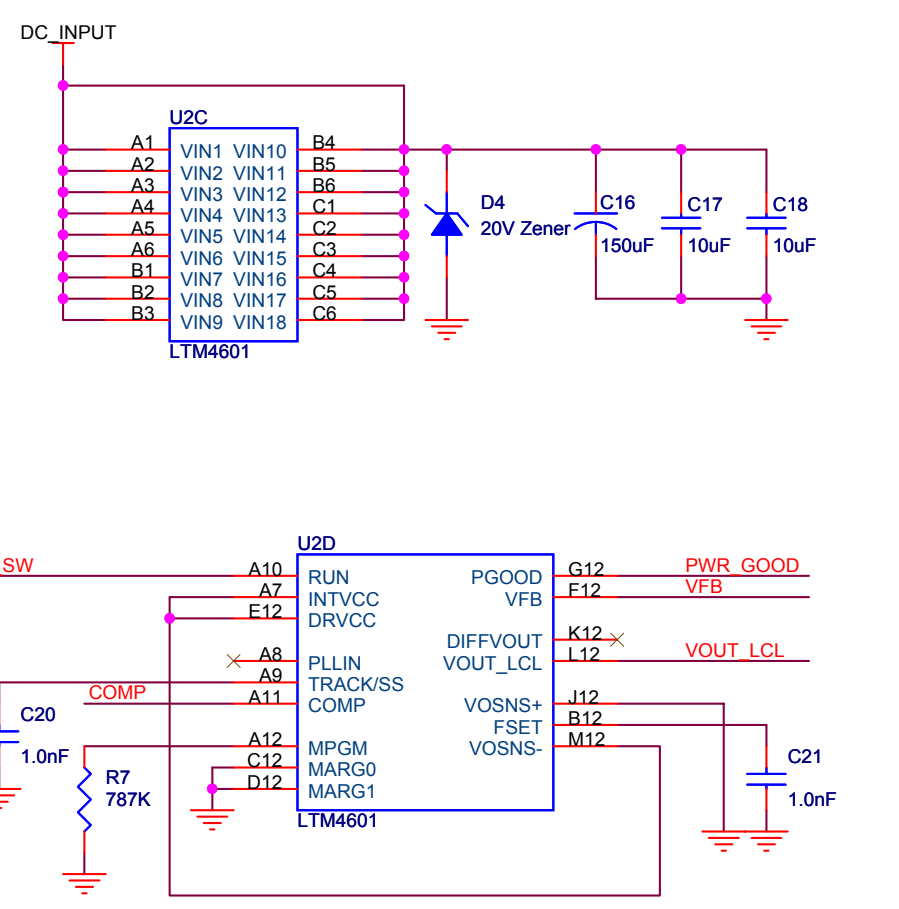
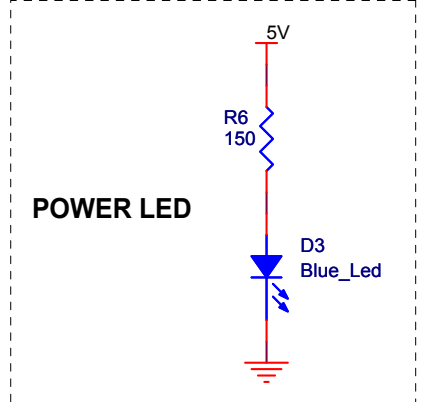
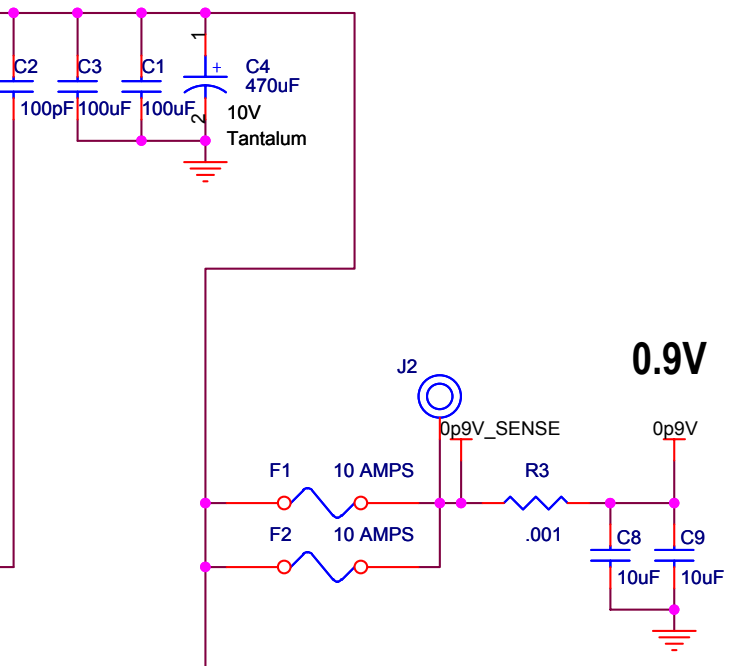
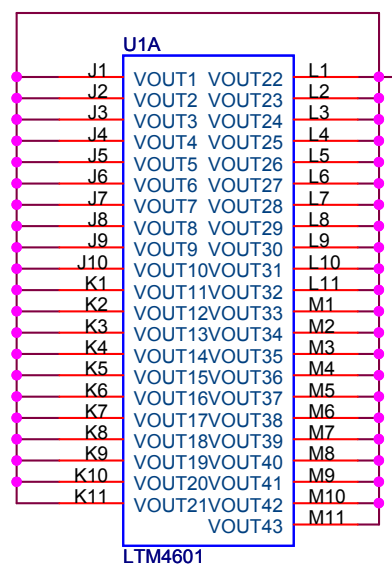
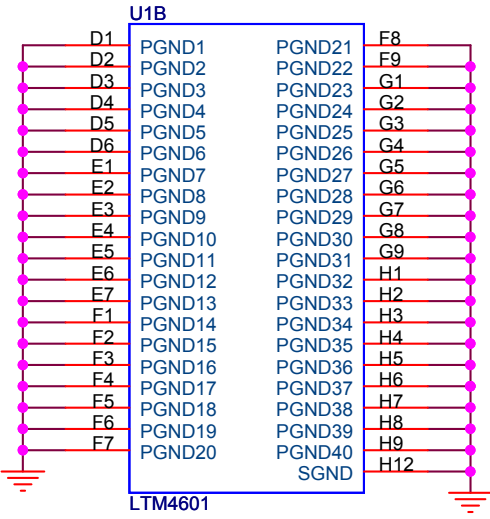
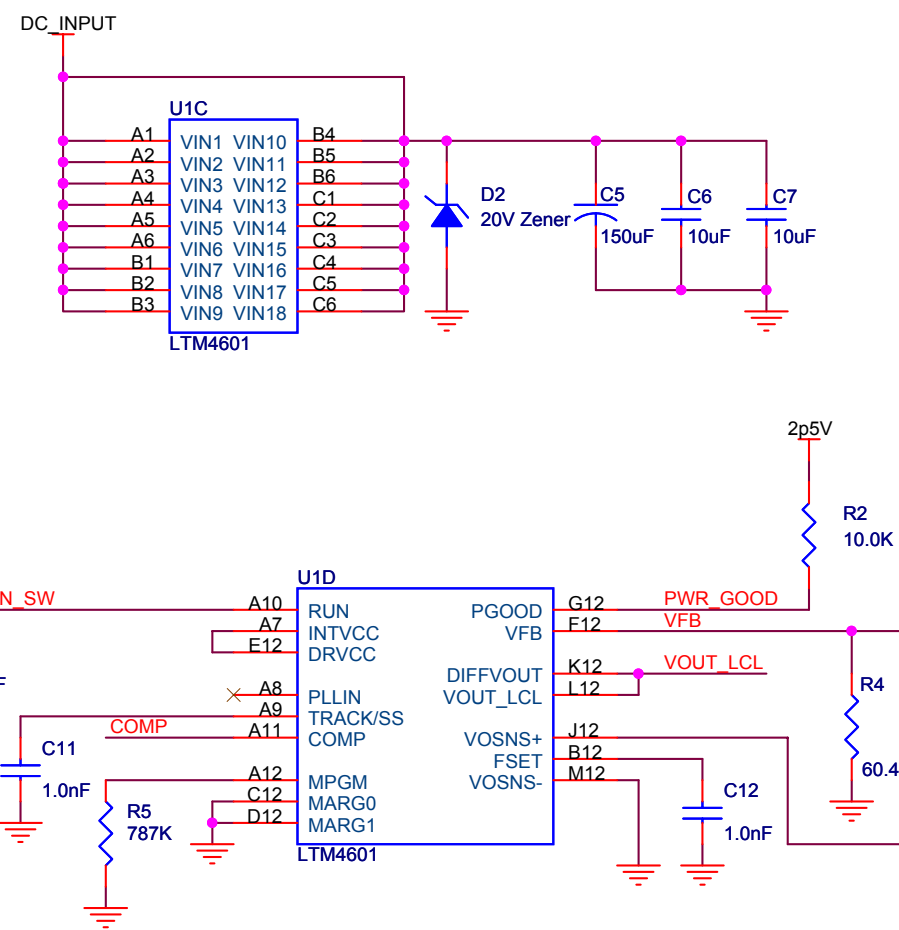
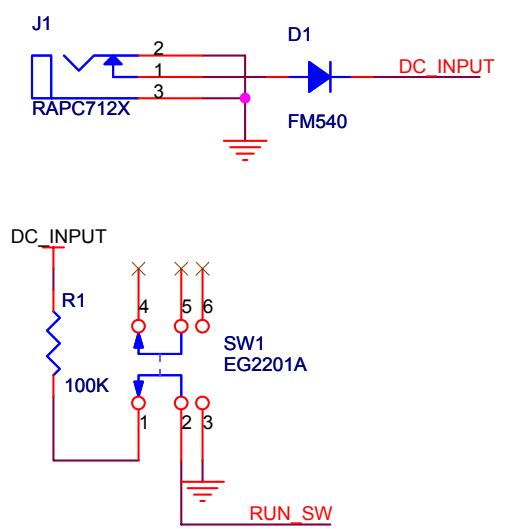
Power Tree



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Power 1

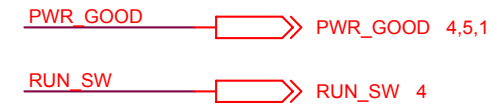
14V-20V DC INPUT



REGULATOR 1

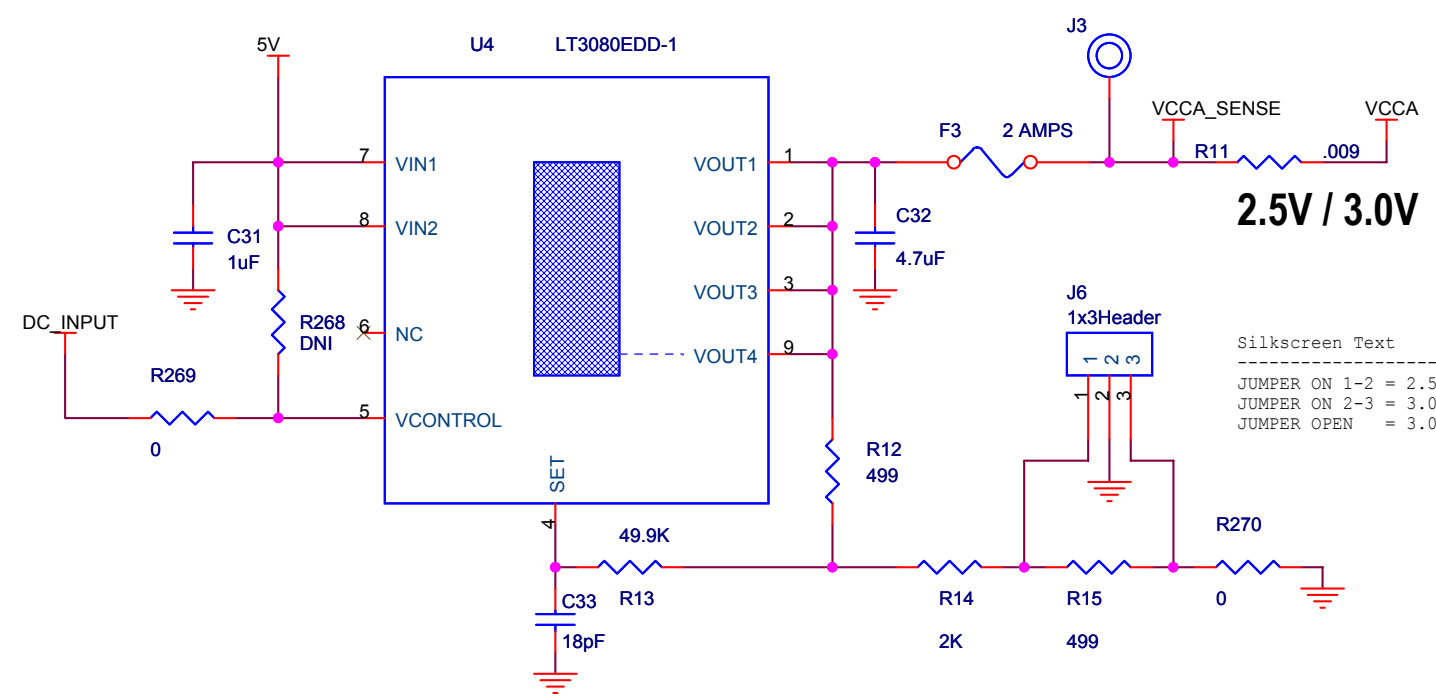
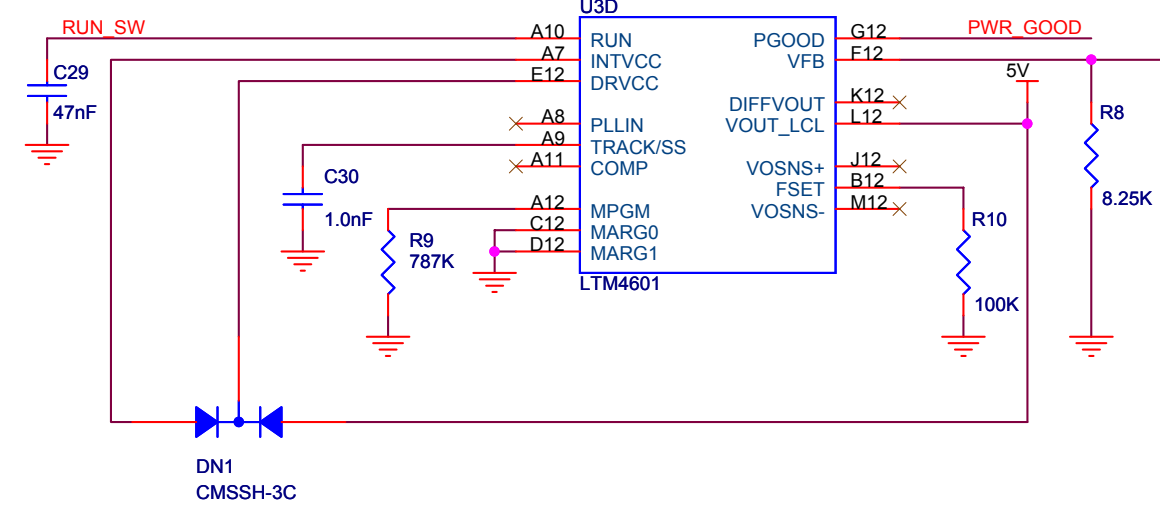
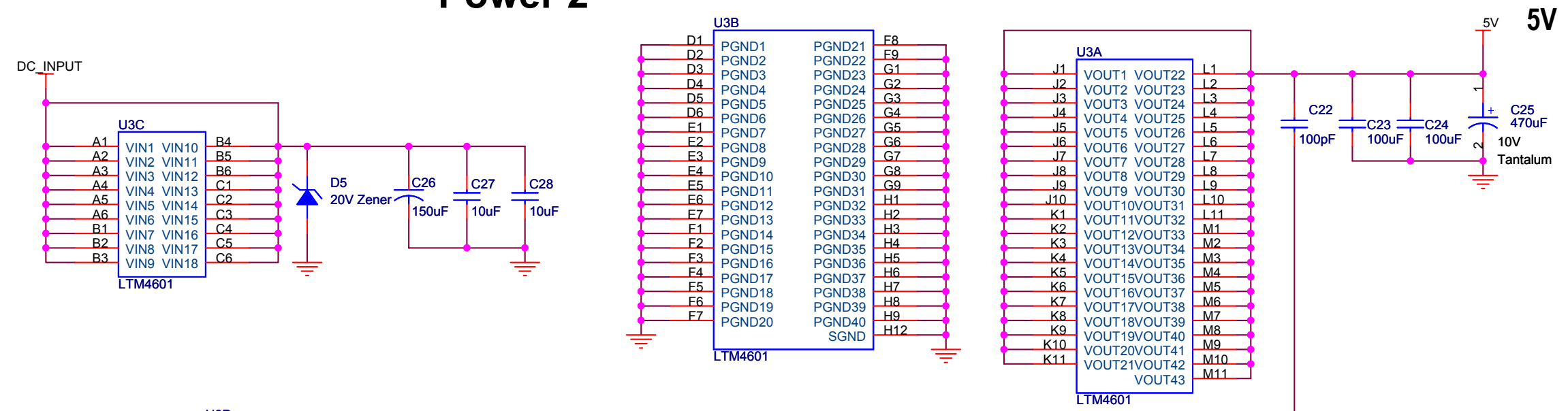
REGULATOR 2

(Regulator1 and Regulator2 are connected in parallel)



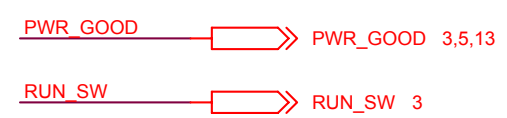
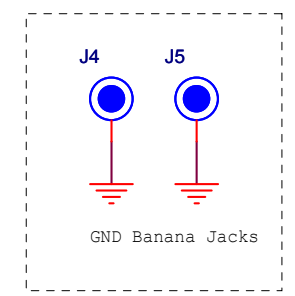
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Power 2



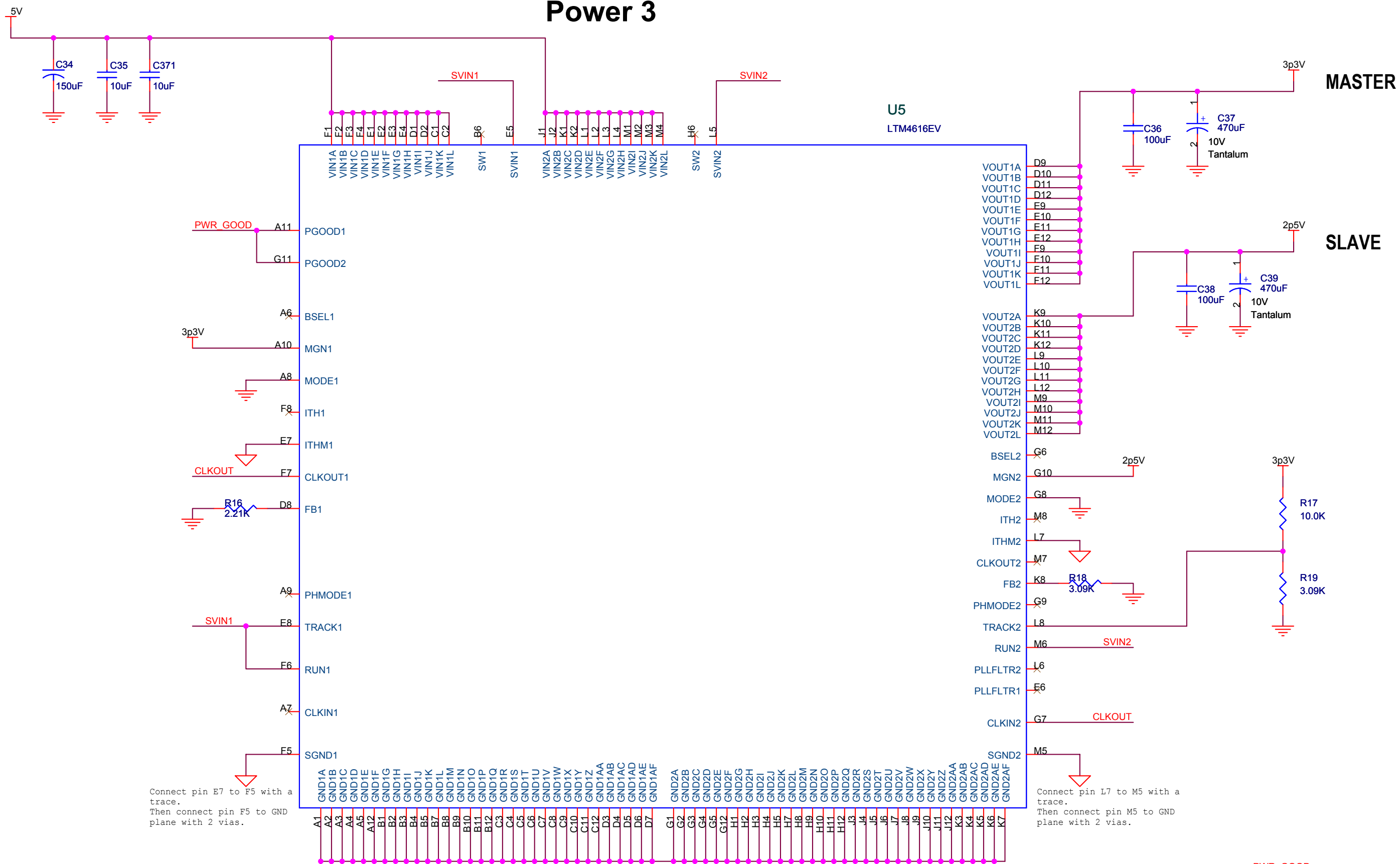
2.5V / 3.0V

Silkscreen Text
 JUMPER ON 1-2 = 2.5V
 JUMPER ON 2-3 = 3.0V
 JUMPER OPEN = 3.0V



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Power 3



Connect pin E7 to F5 with a trace.
Then connect pin F5 to GND plane with 2 vias.

Connect pin L7 to M5 with a trace.
Then connect pin M5 to GND plane with 2 vias.

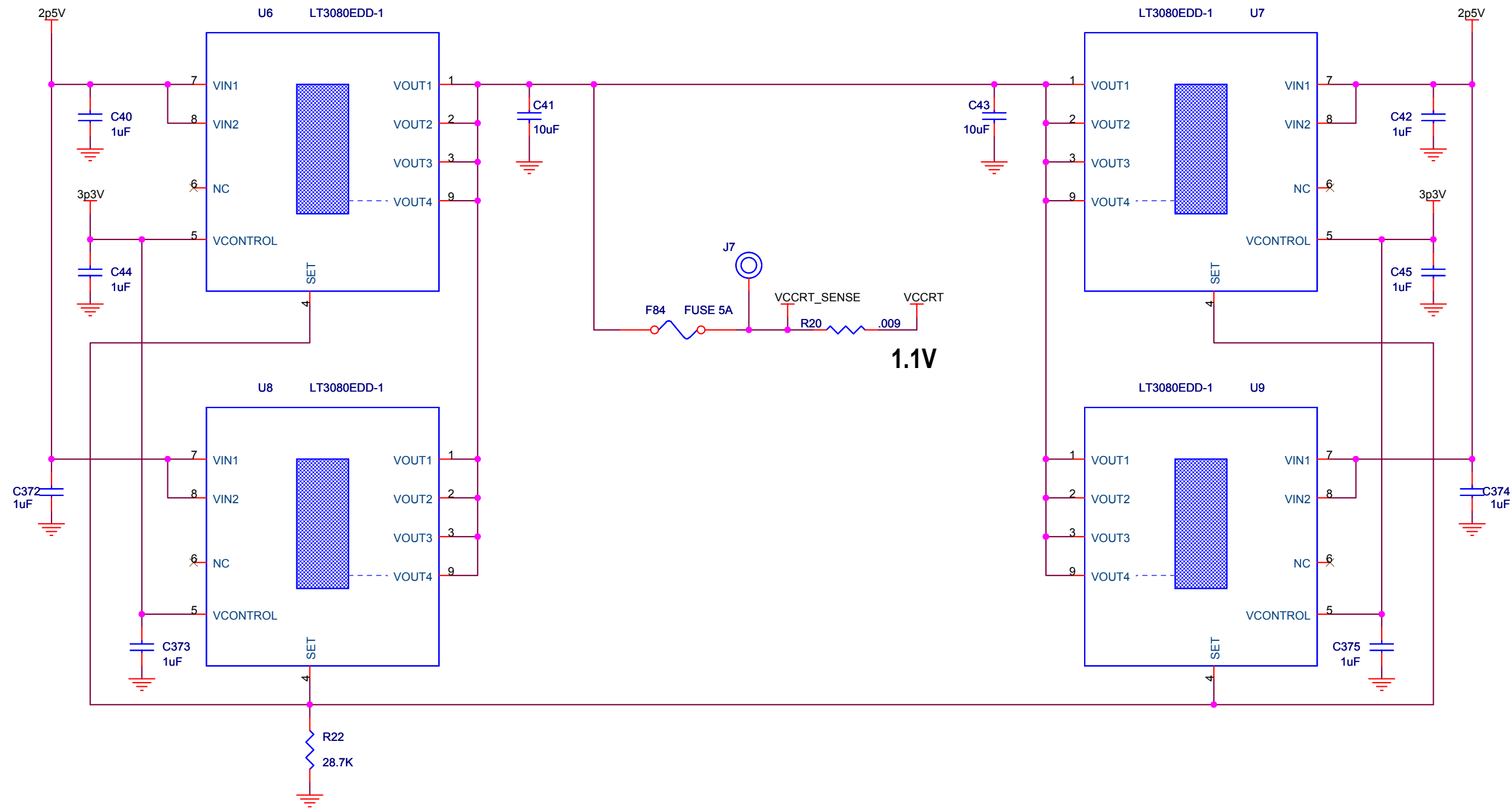
Refer to Datasheet for recommended layout

PWR_GOOD → PWR_GOOD 3,4,13



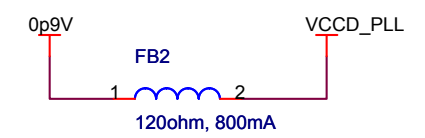
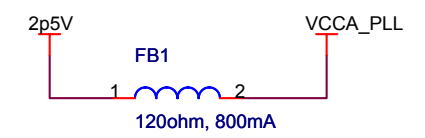
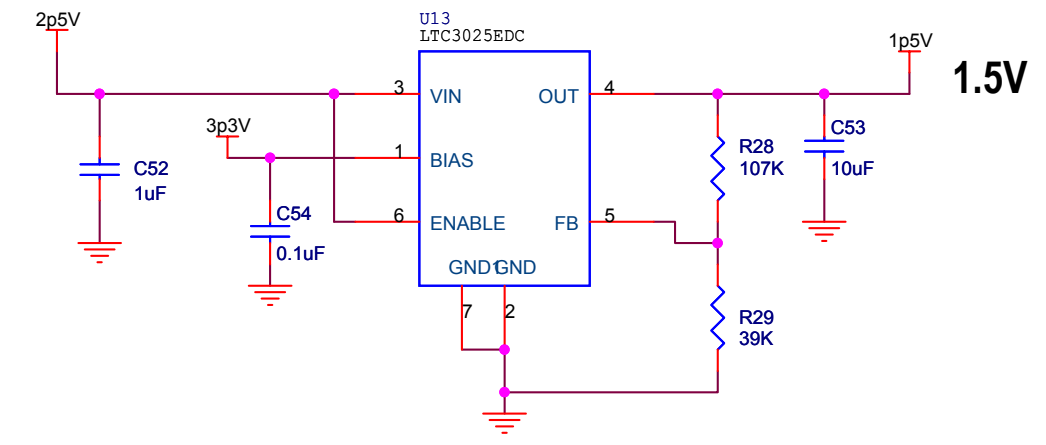
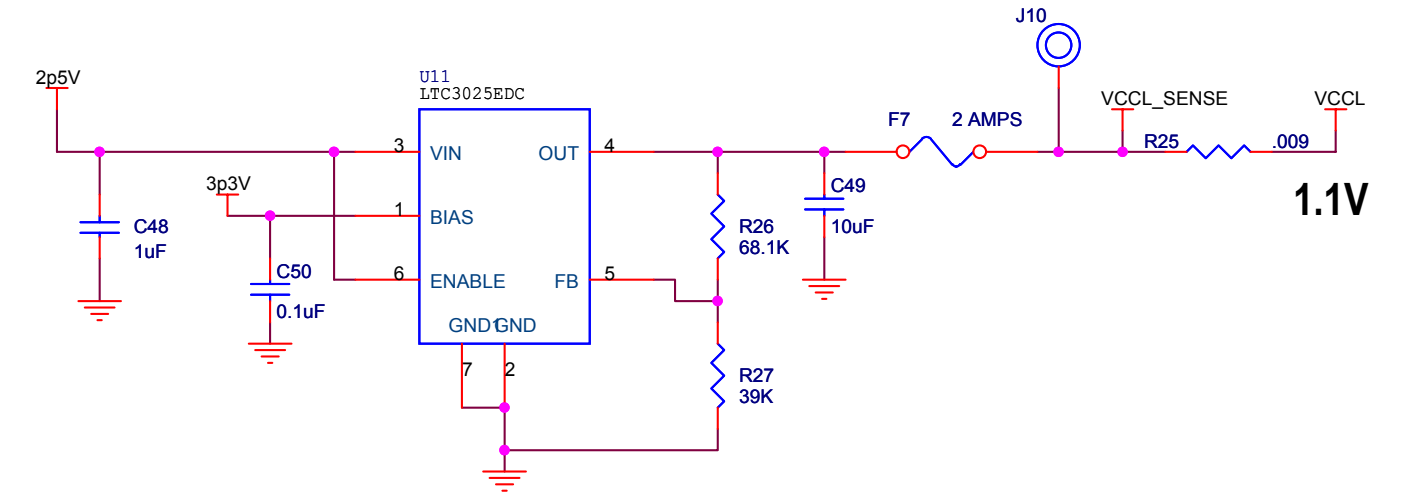
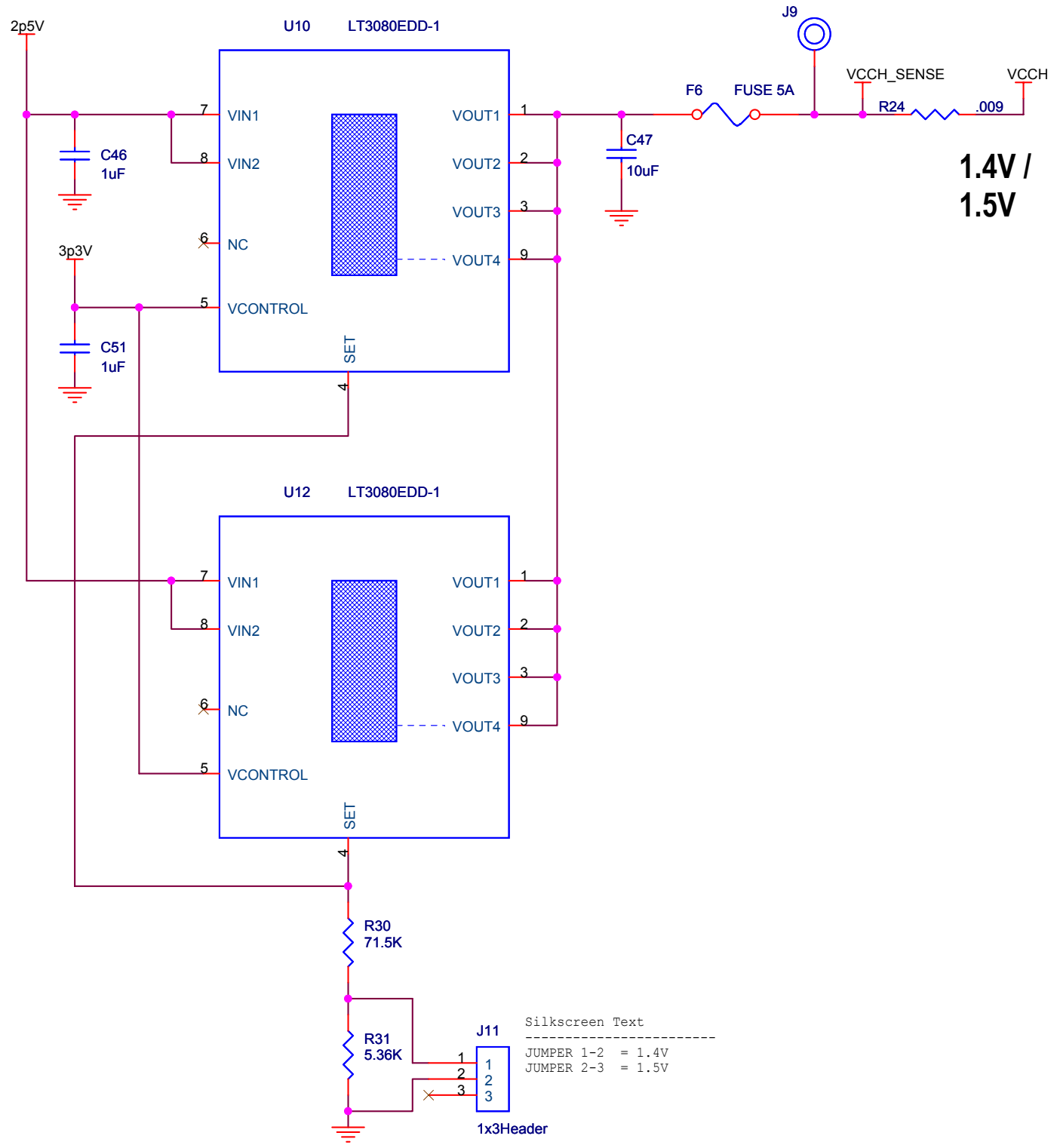
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Power 4



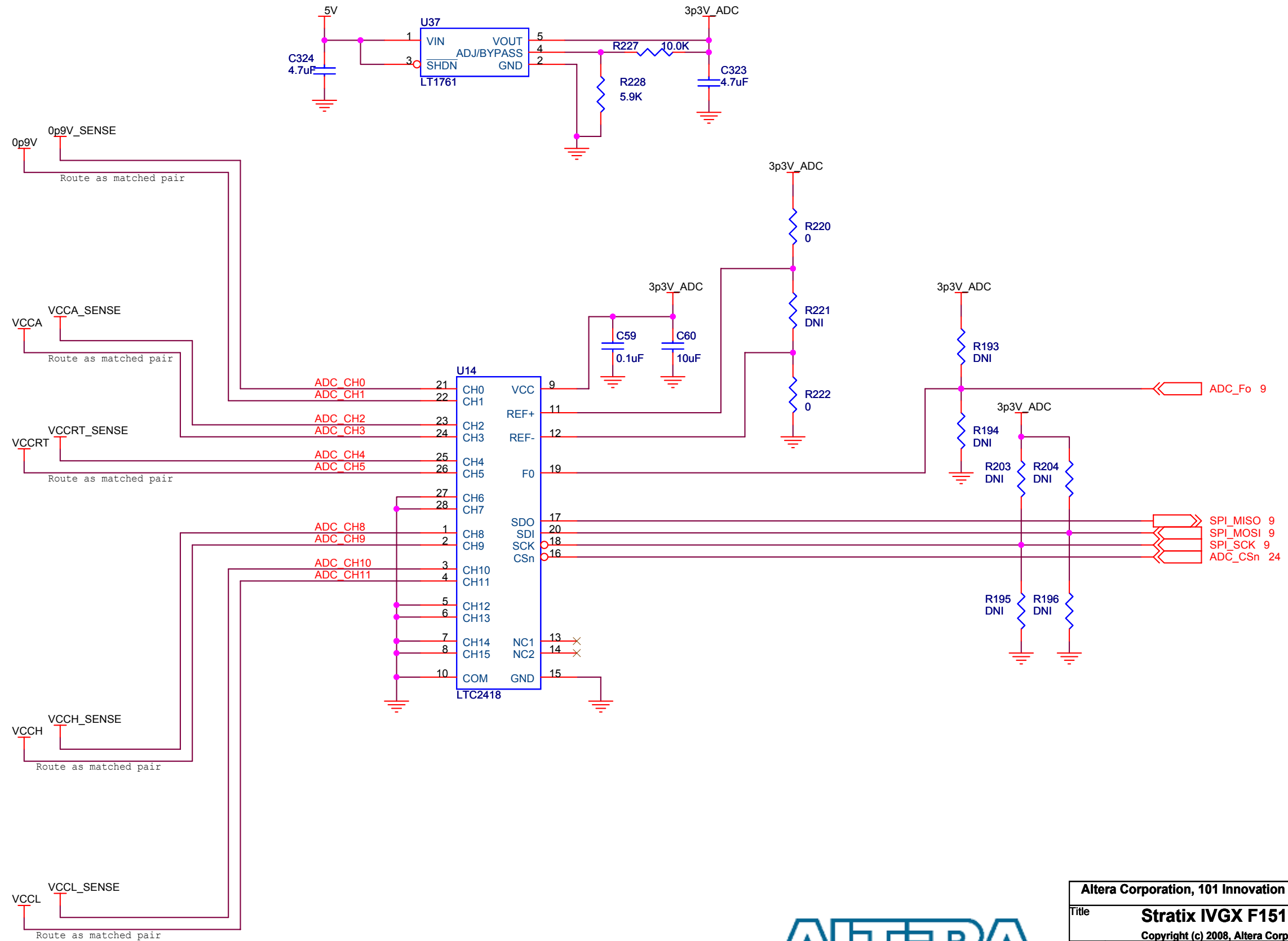
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Power 5



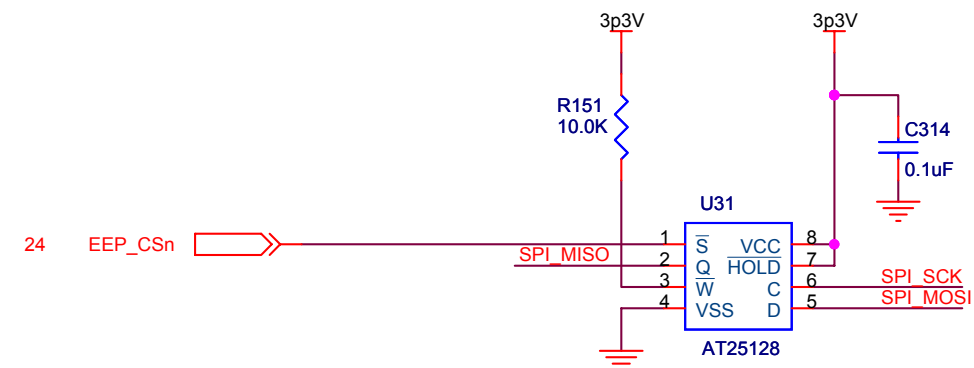
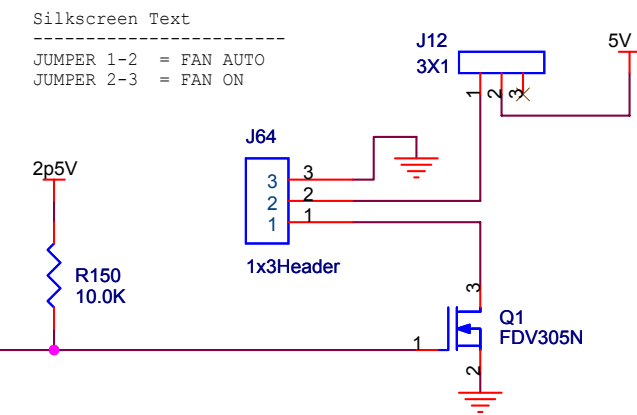
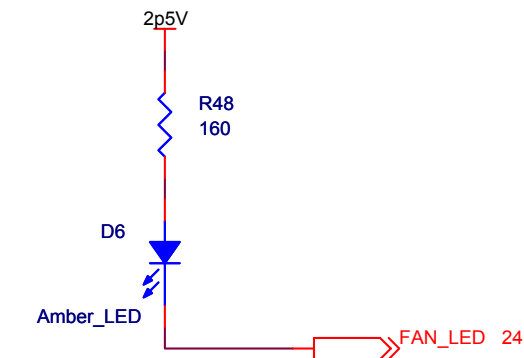
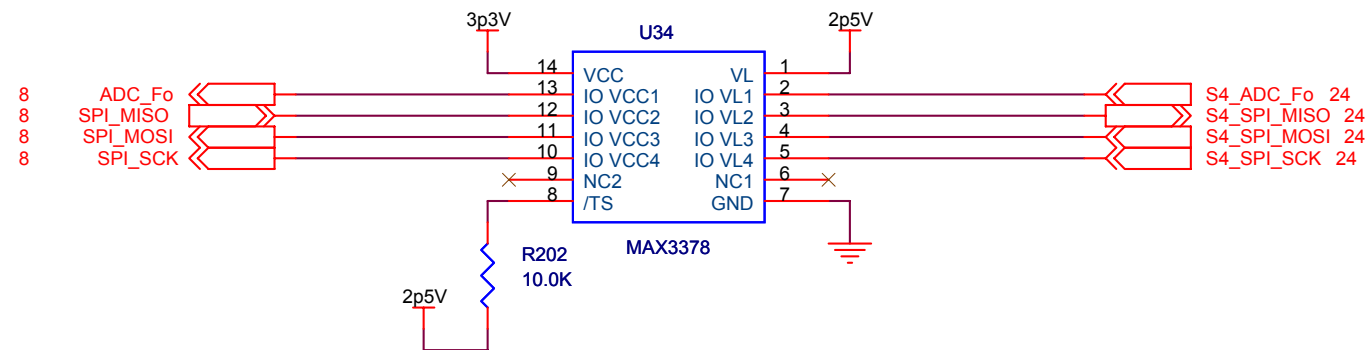
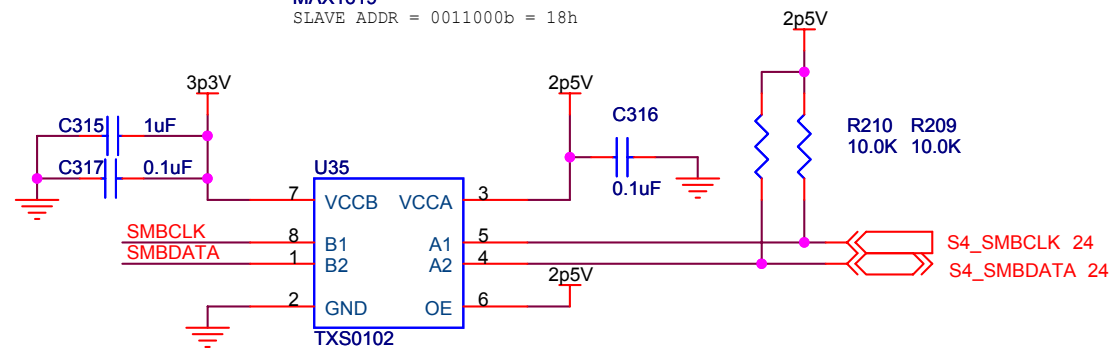
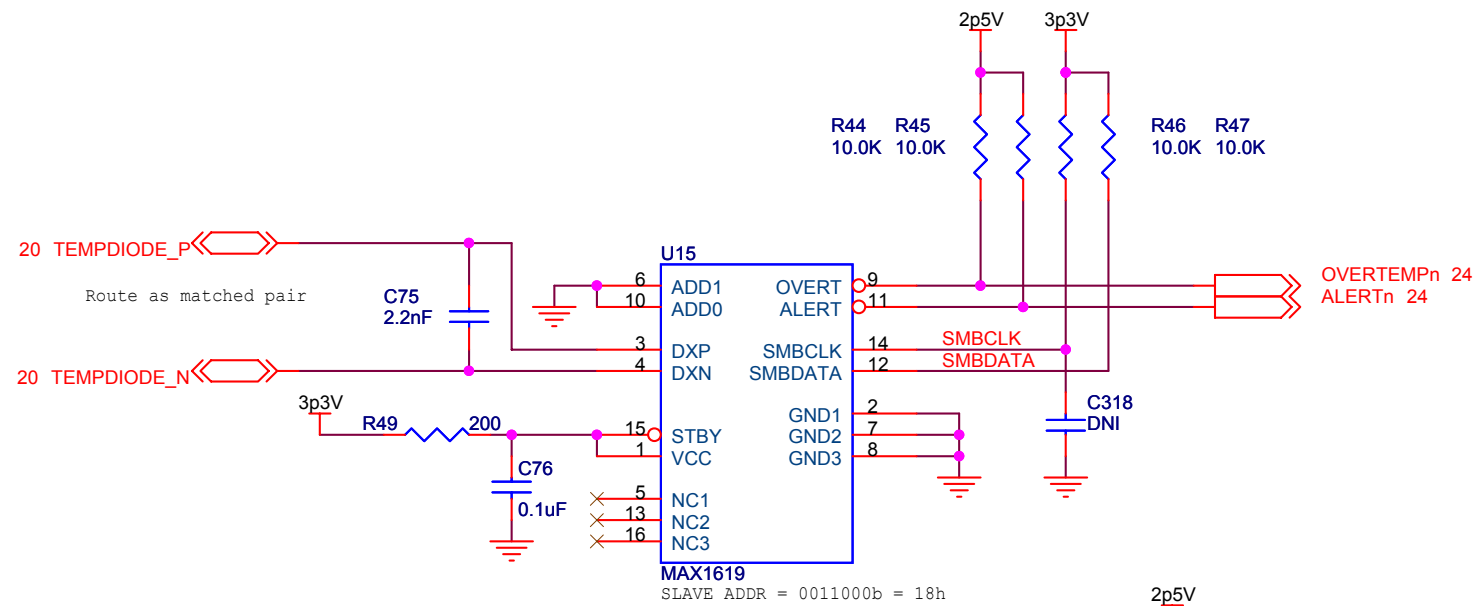
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Power Measure



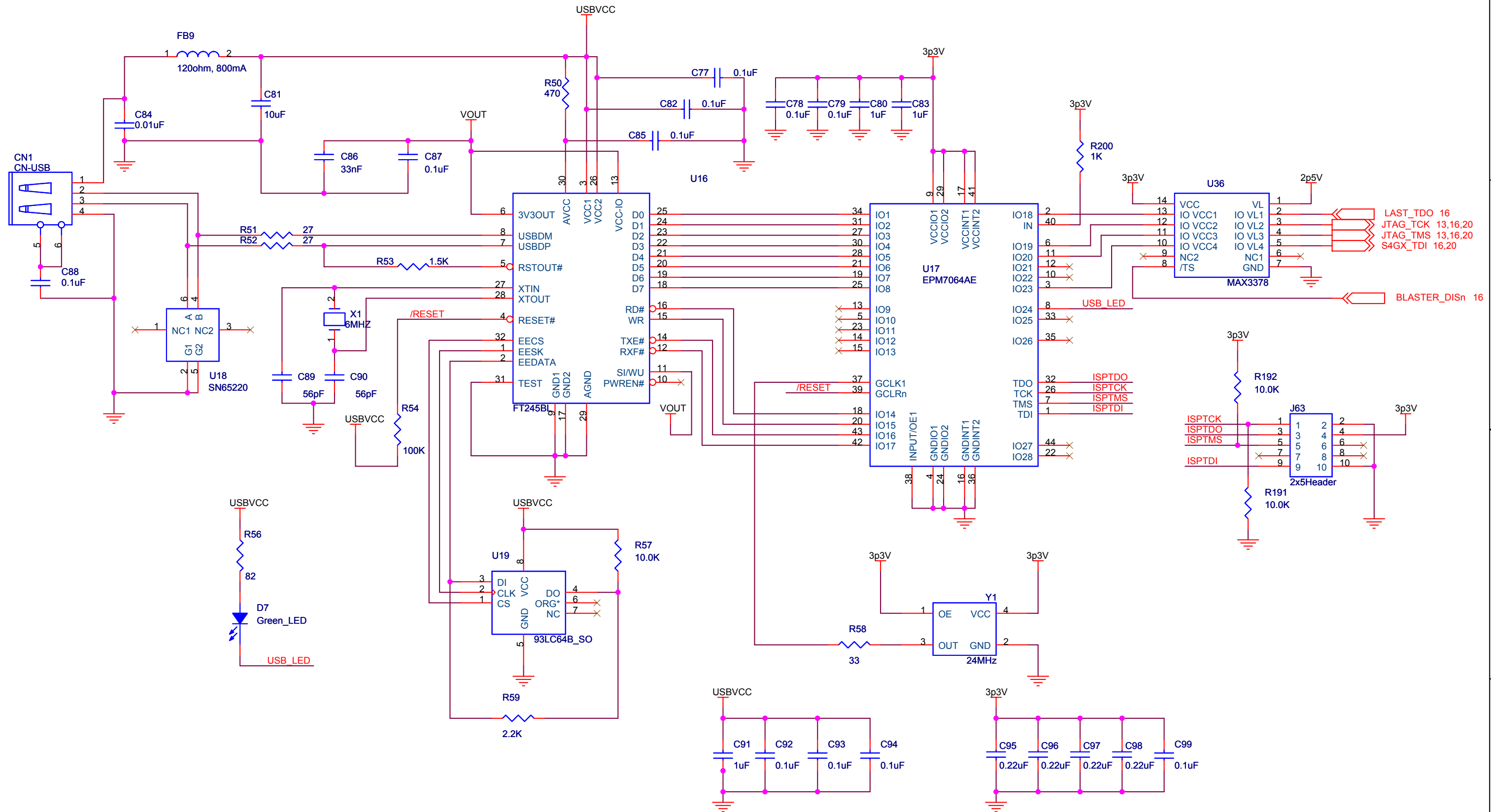
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Temperature Measure



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USB BLASTER



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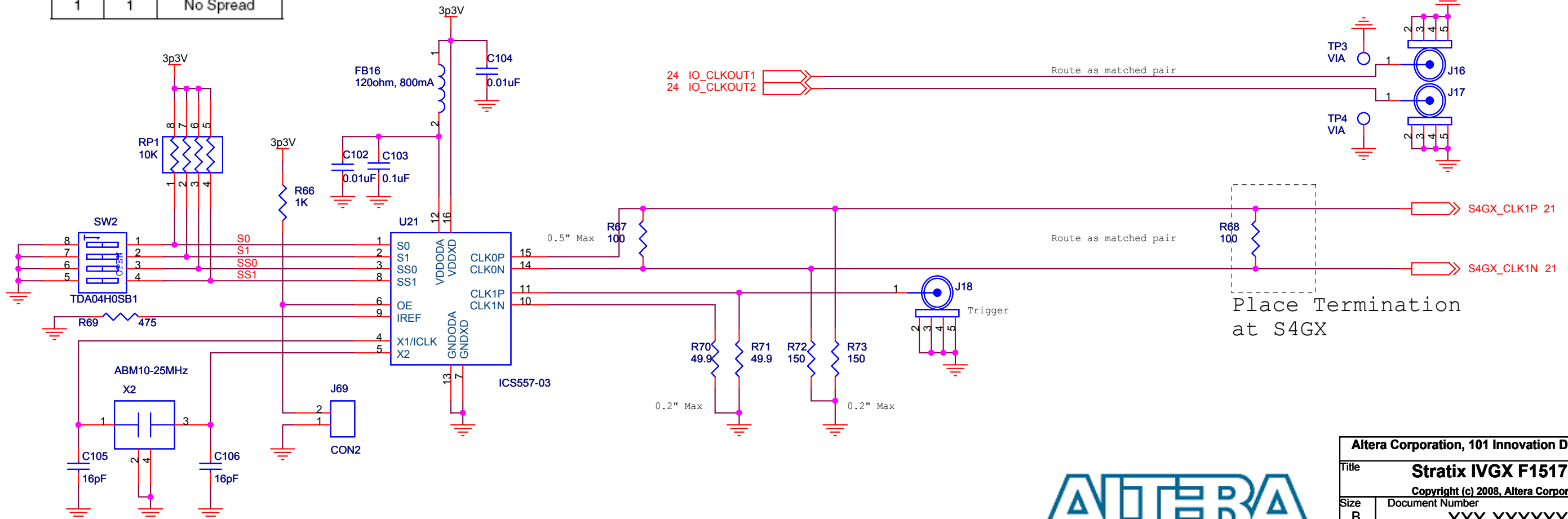
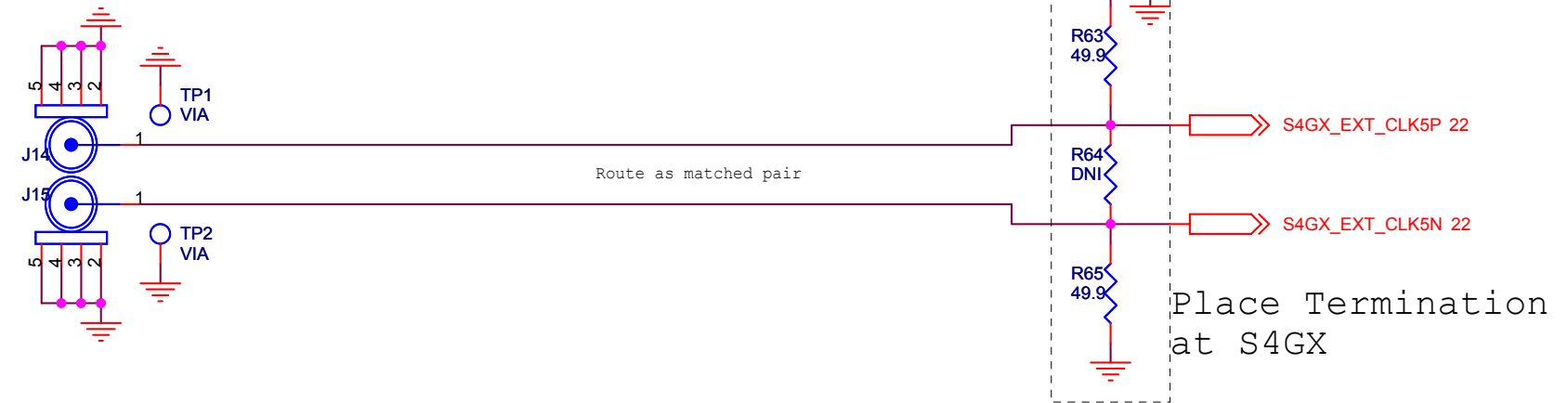
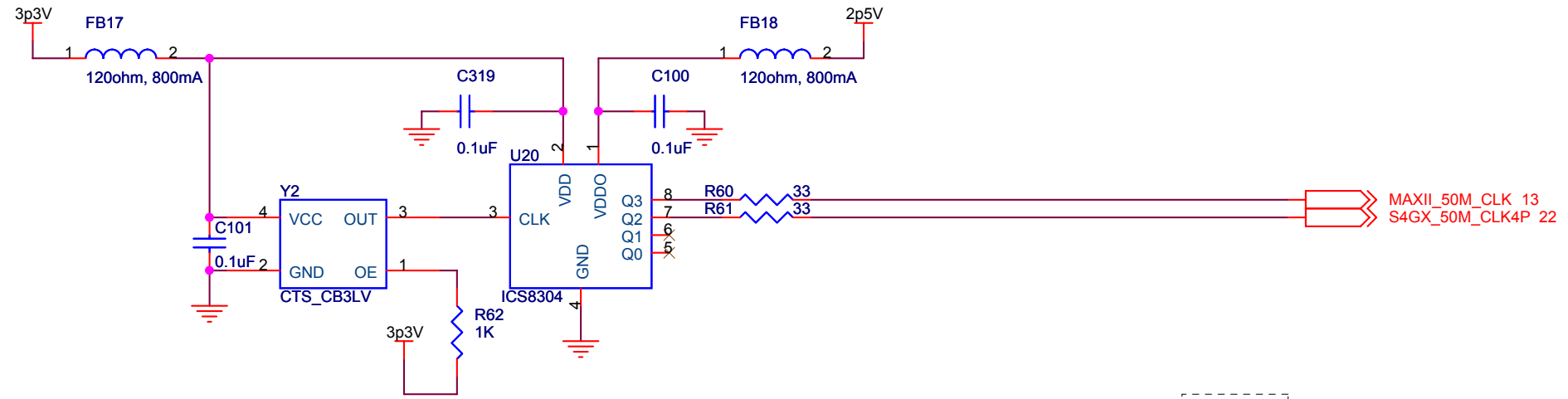
GLOBAL CLOCKS

Output Select Table 1(MHz)

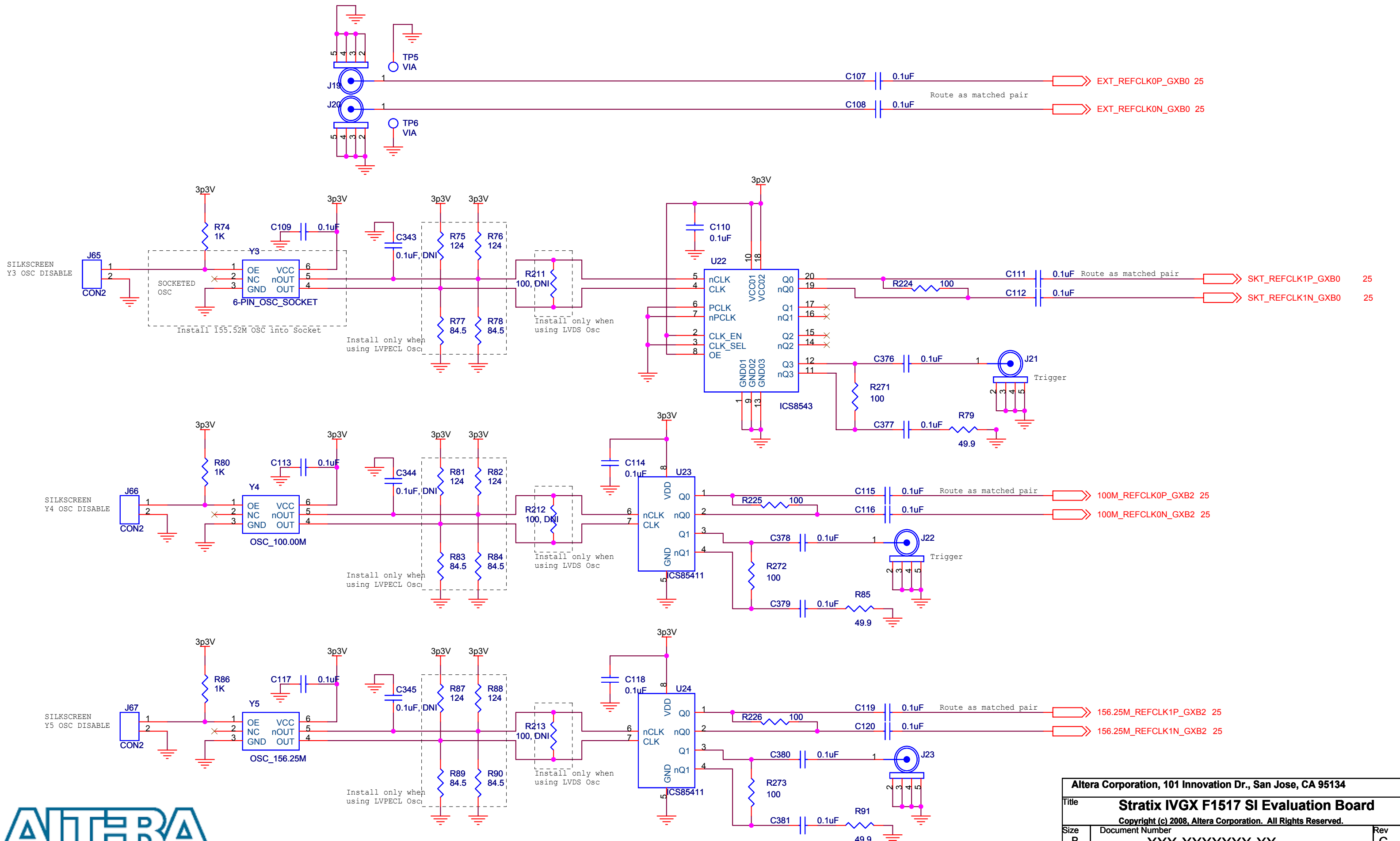
S1	S0	CLK(1:0), CLK(1:0)
0	0	25M
0	1	100M
1	0	125M
1	1	200M

Spread Selection Table 2

SS1	SS0	Spread %
0	0	Center ±0.25
0	1	Down -0.5
1	0	Down -0.75
1	1	No Spread

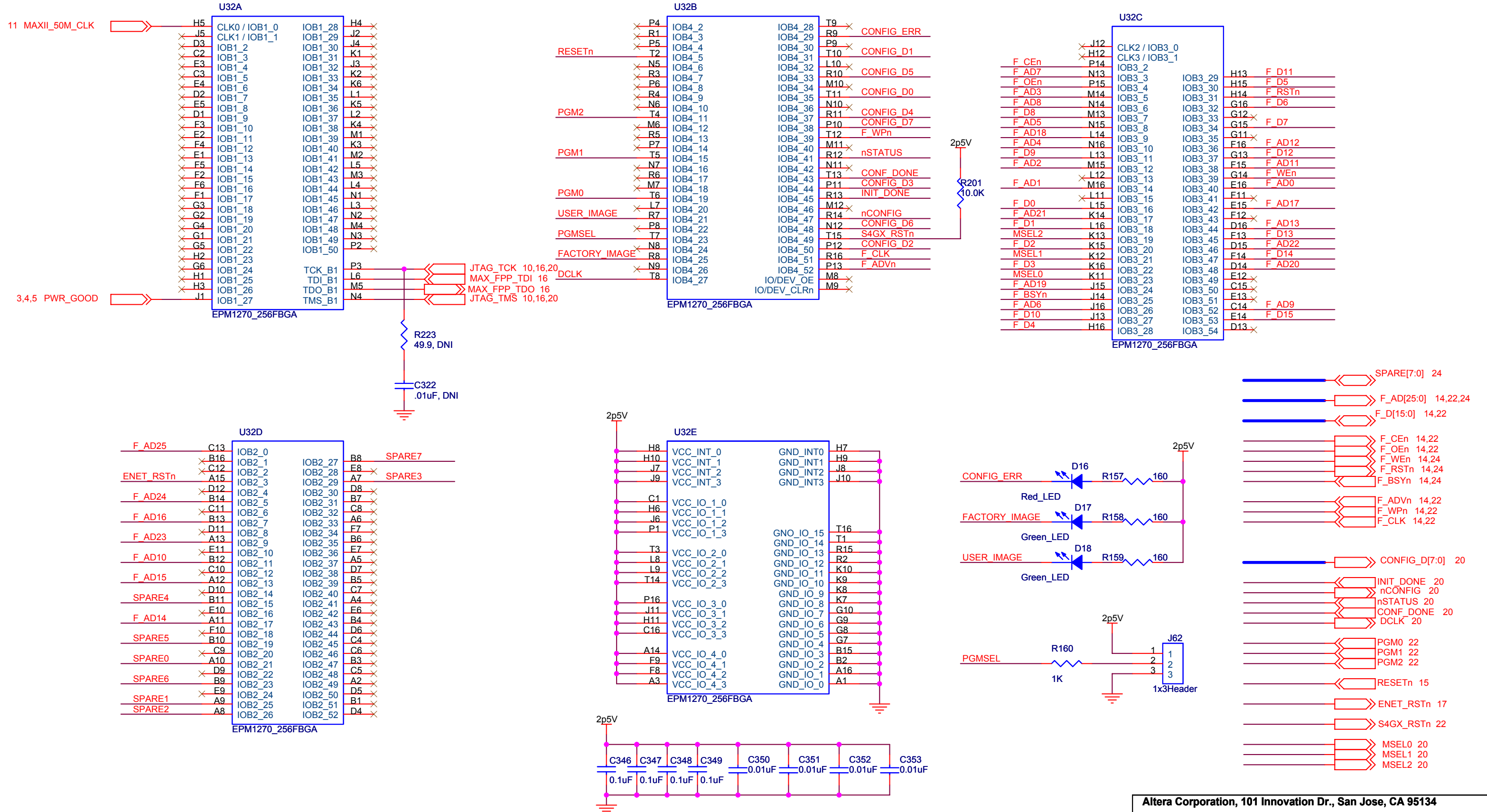


TRANSCEIVER CLOCKS



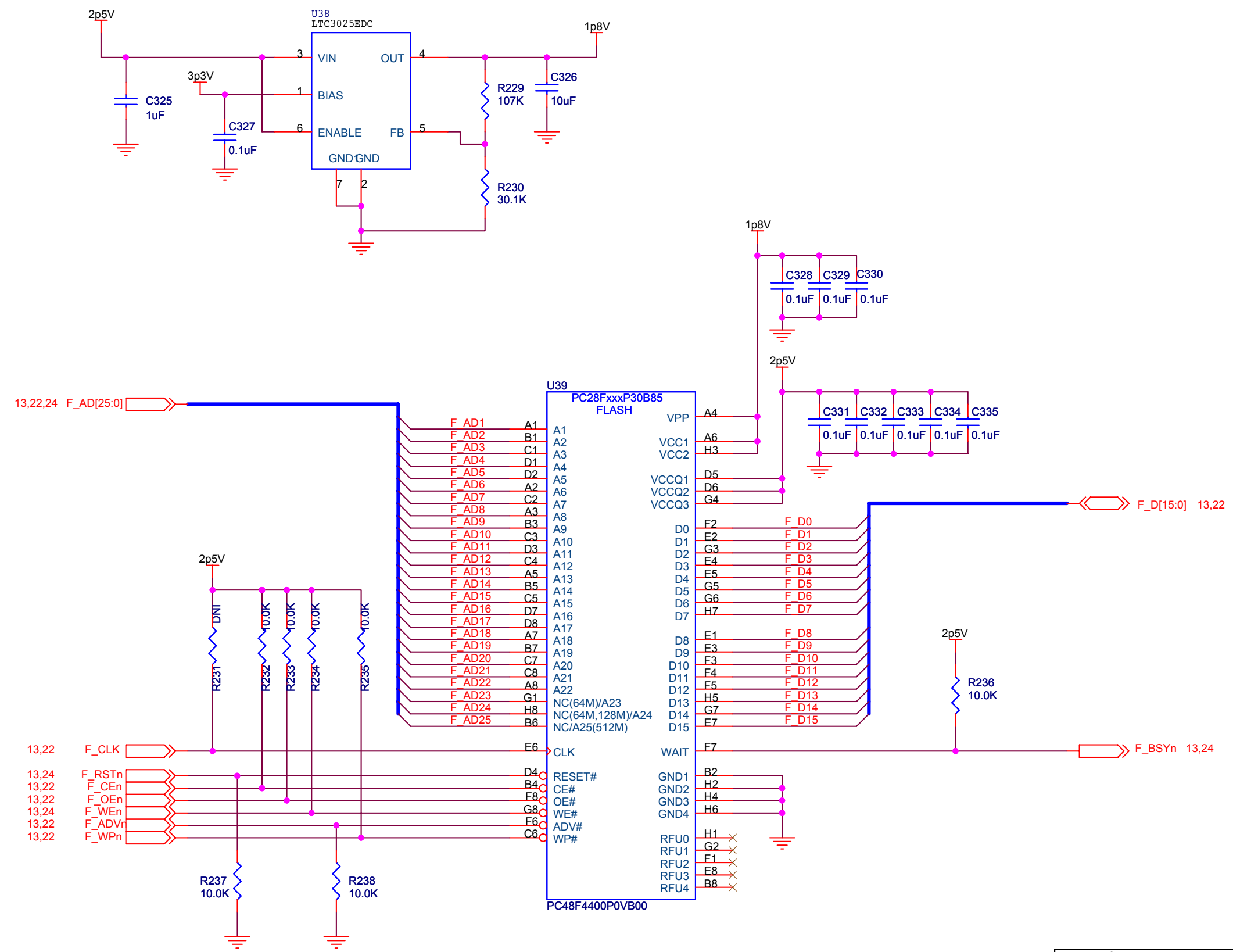
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MAXII FPP CONFIGURATION



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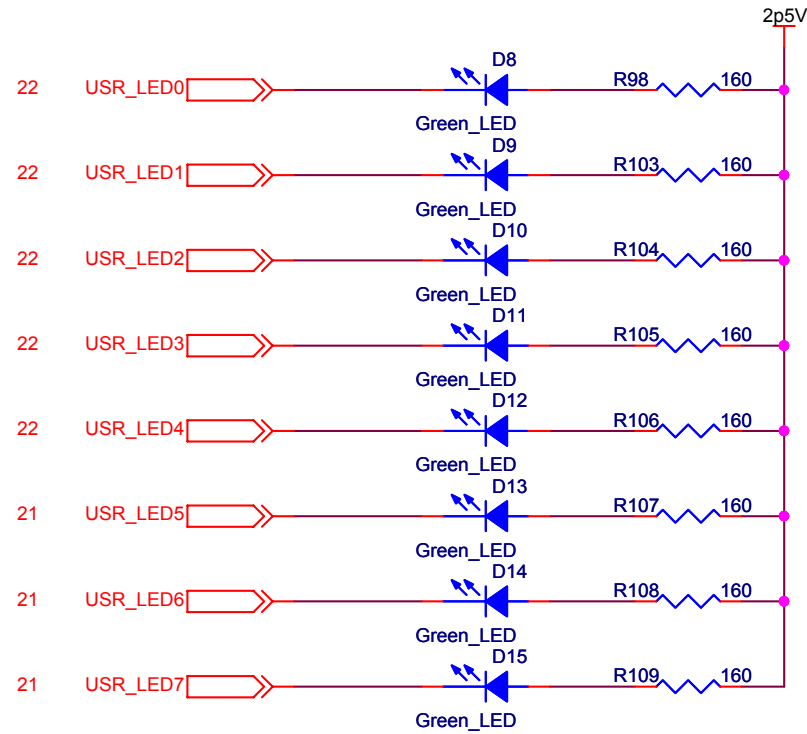
FLASH MEMORY



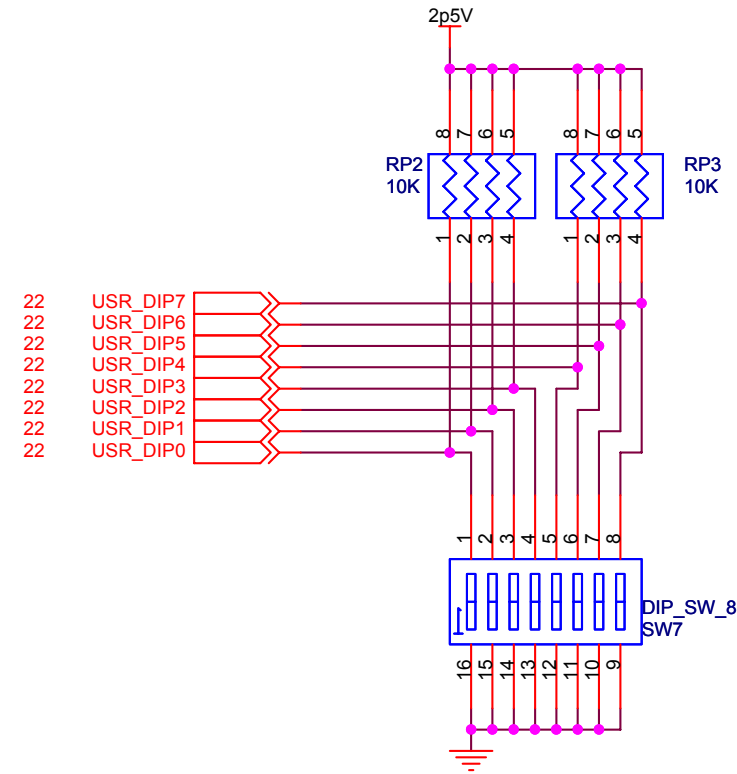
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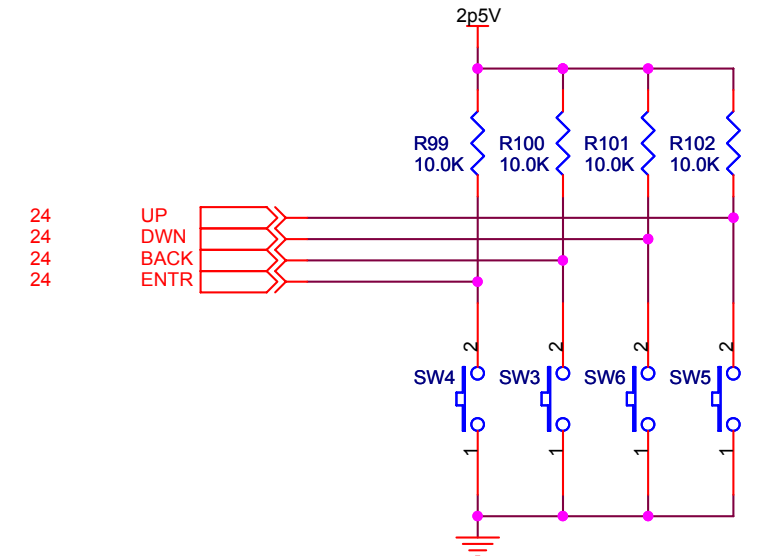
BUTTONS, SWITCHES, LEDES, LCD DISPLAY



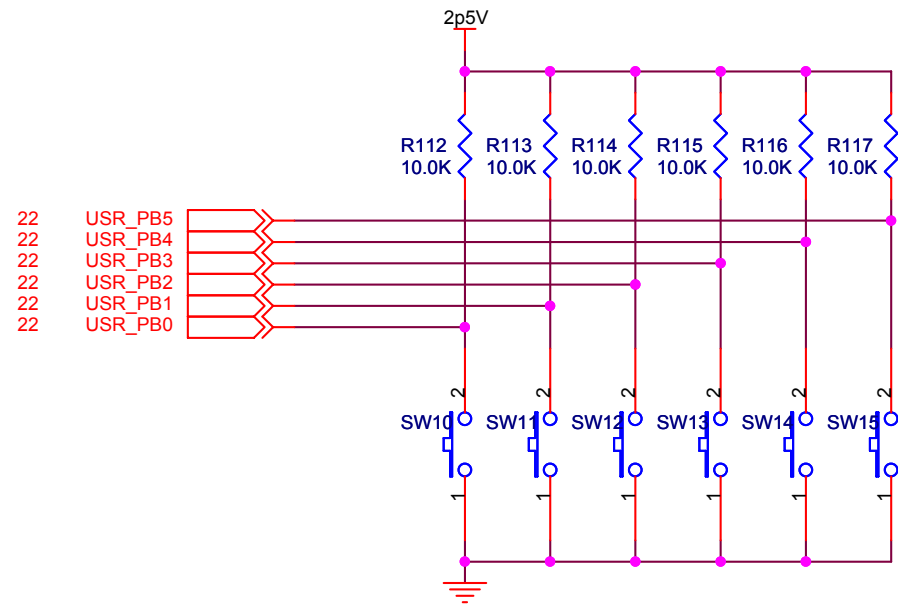
USER LEDES



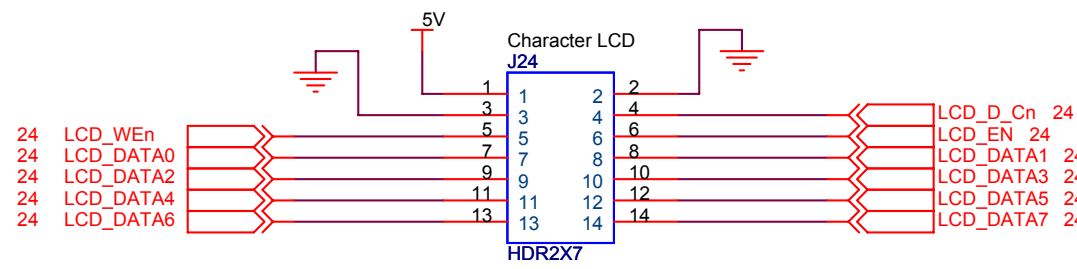
USER DIP SWITCHES



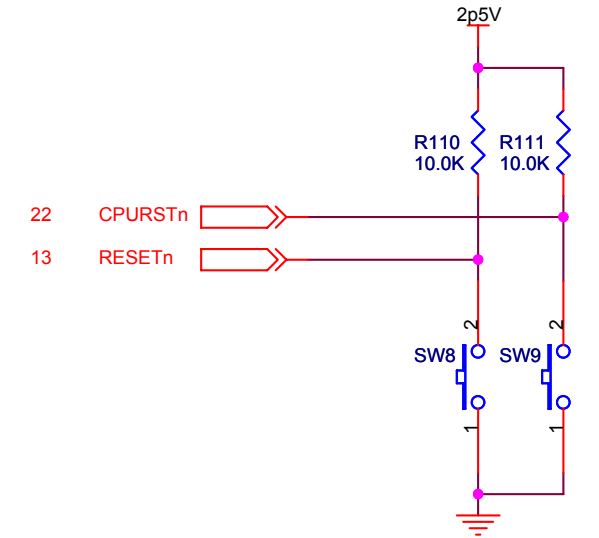
LCD DIRECTIONAL BUTTONS



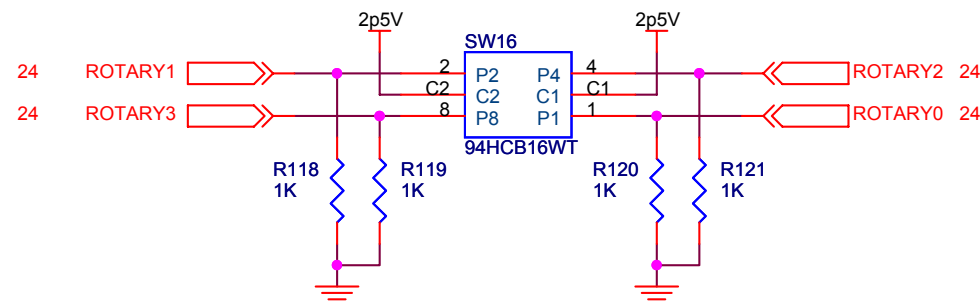
USER PUSHBUTTONS



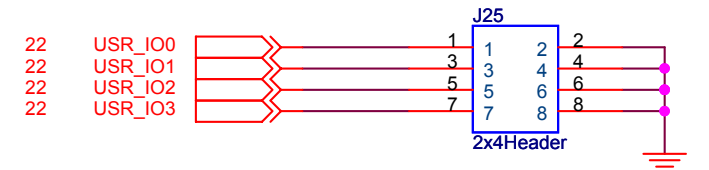
LCD DISPLAY HEADER



RESET PUSHBUTTONS



HEX ROTARY SWITCH

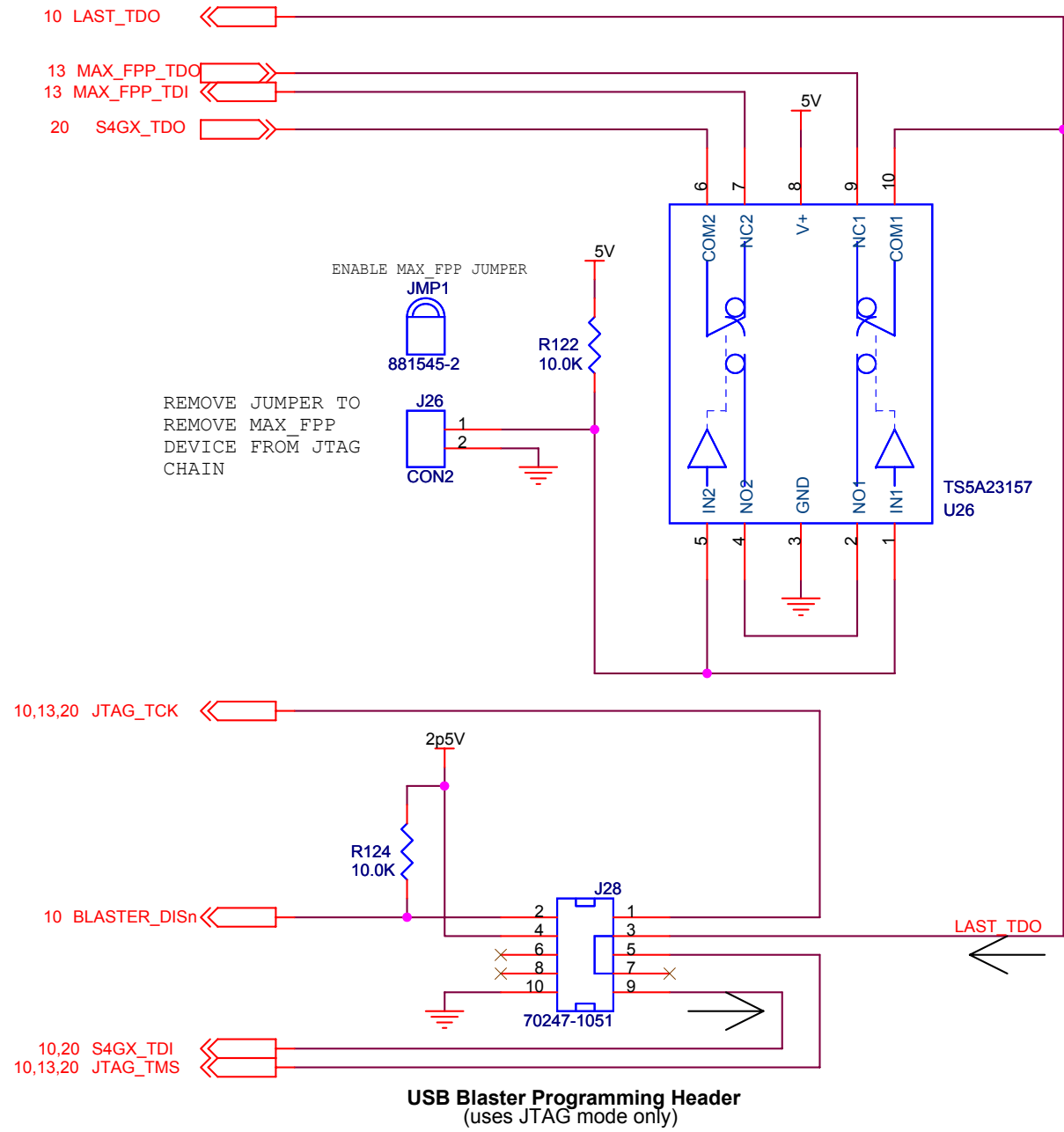


USER I/O'S

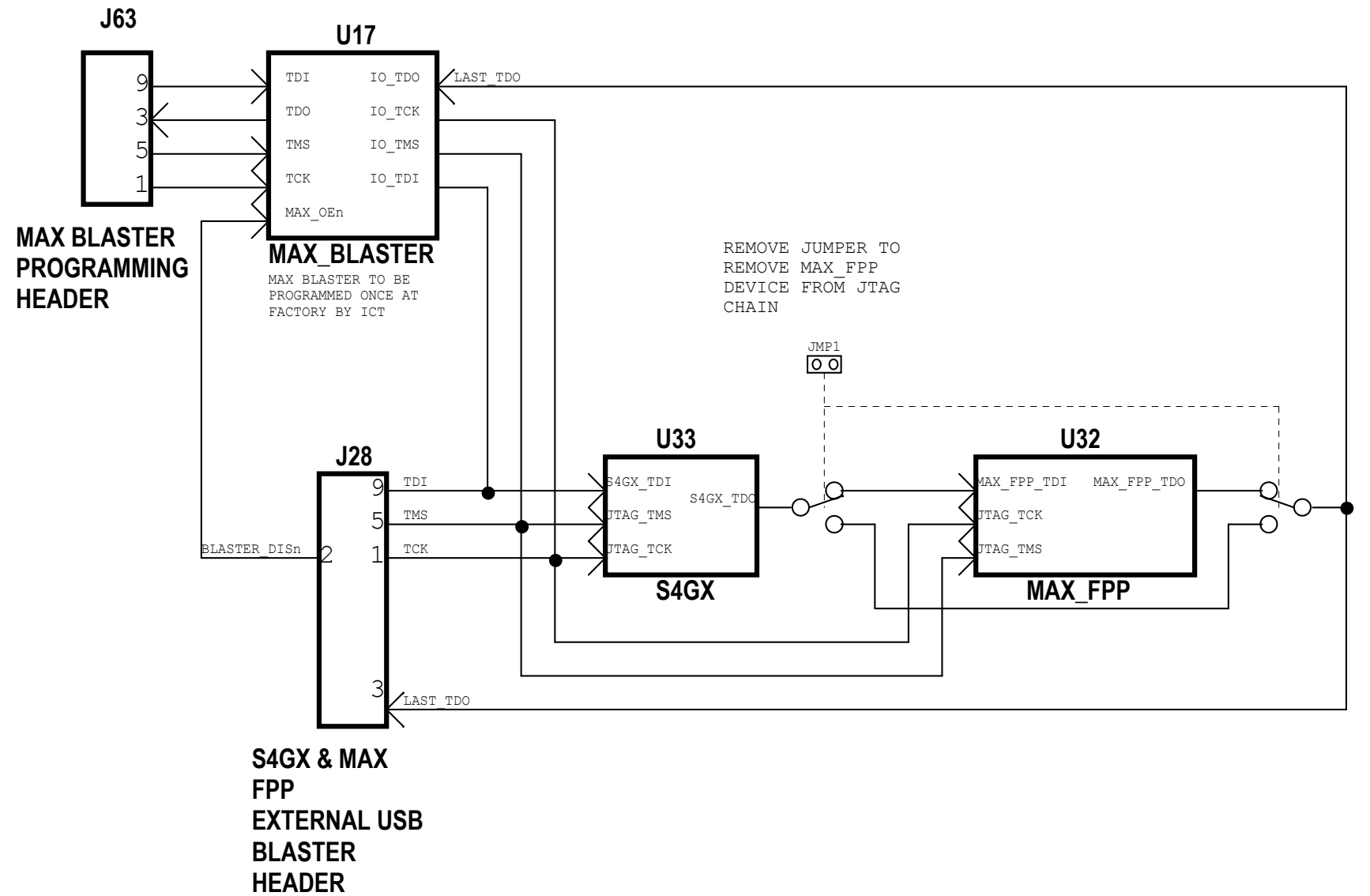


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JTAG CHAIN

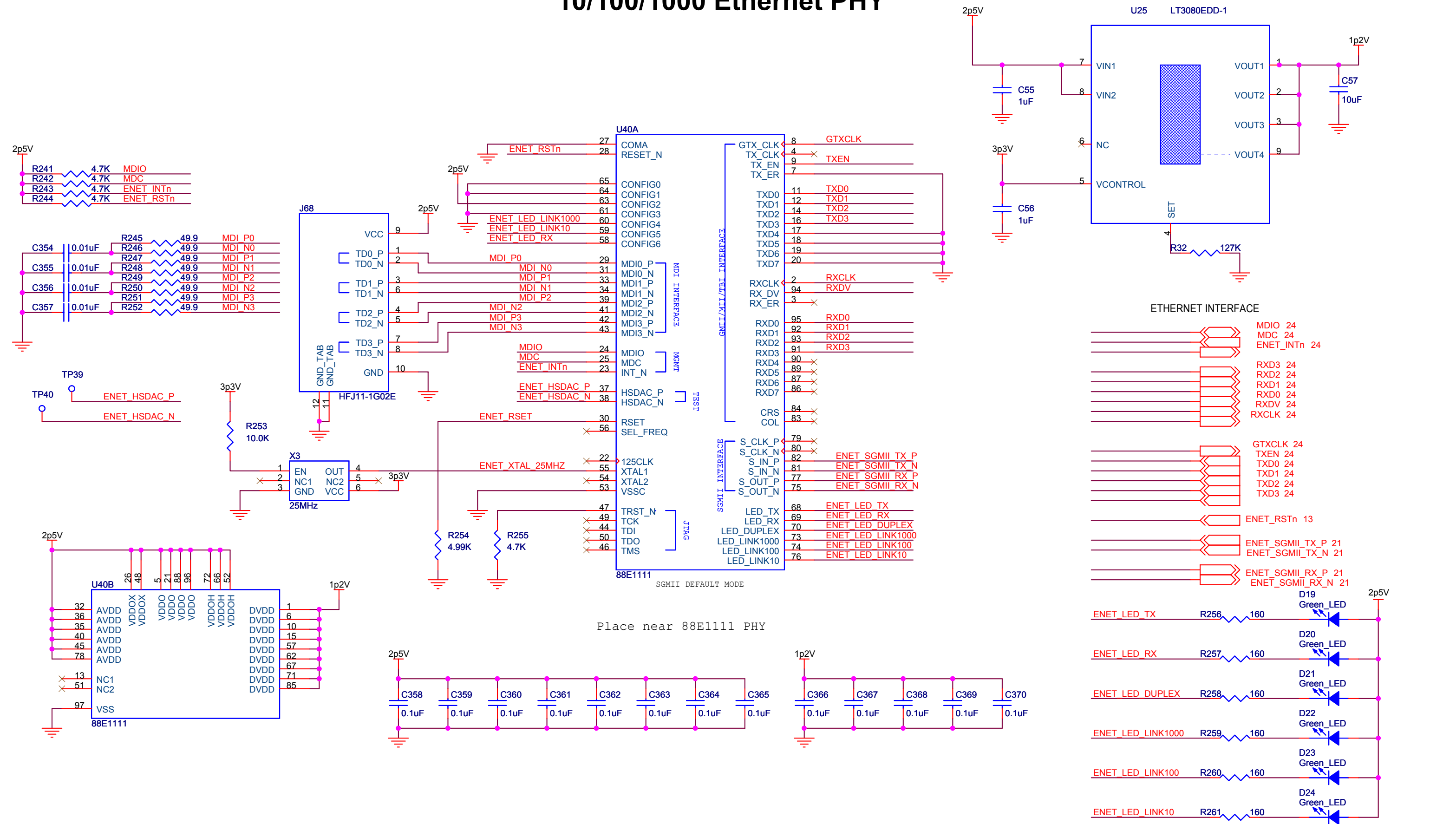


JTAG CHAIN BLOCK DIAGRAM



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10/100/1000 Ethernet PHY



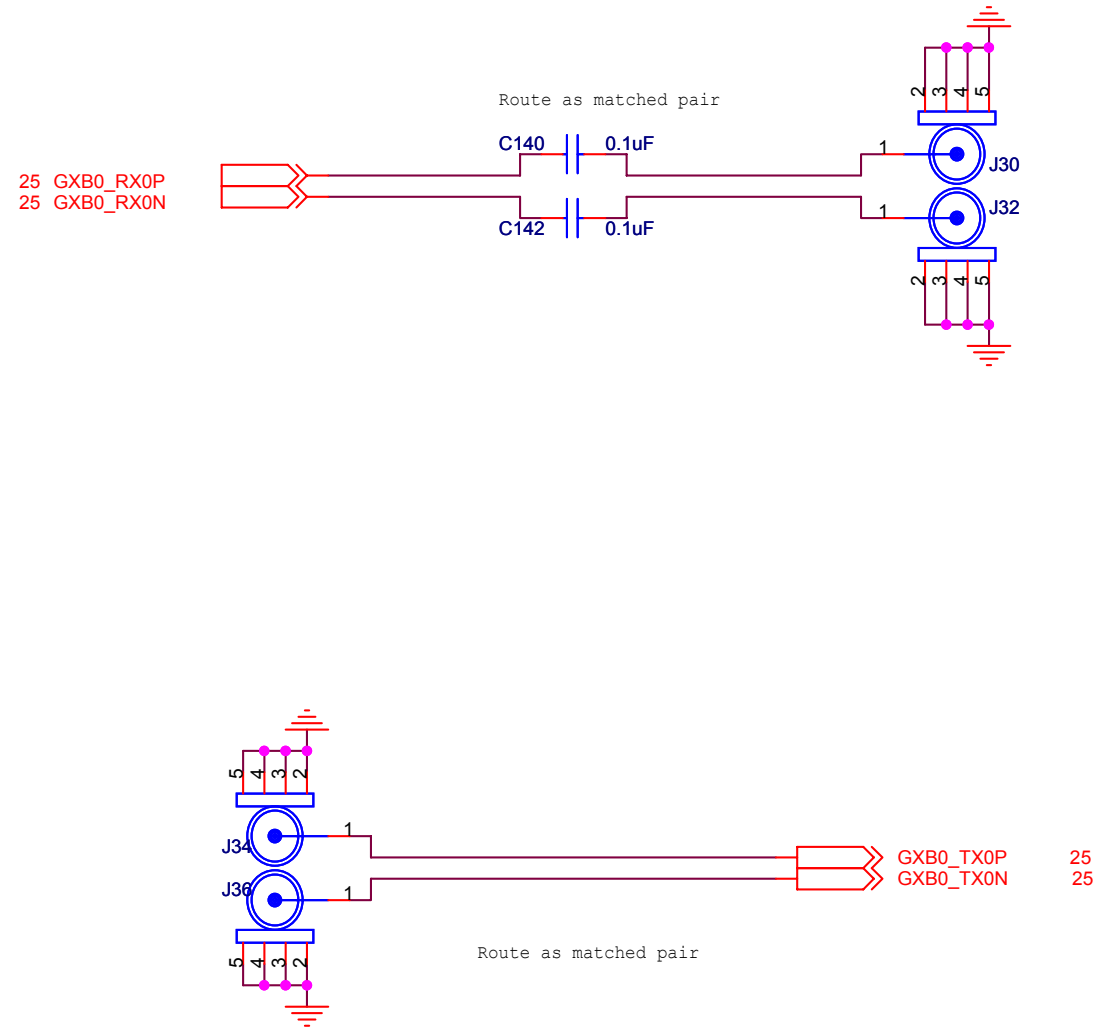
Place near 88E1111 PHY



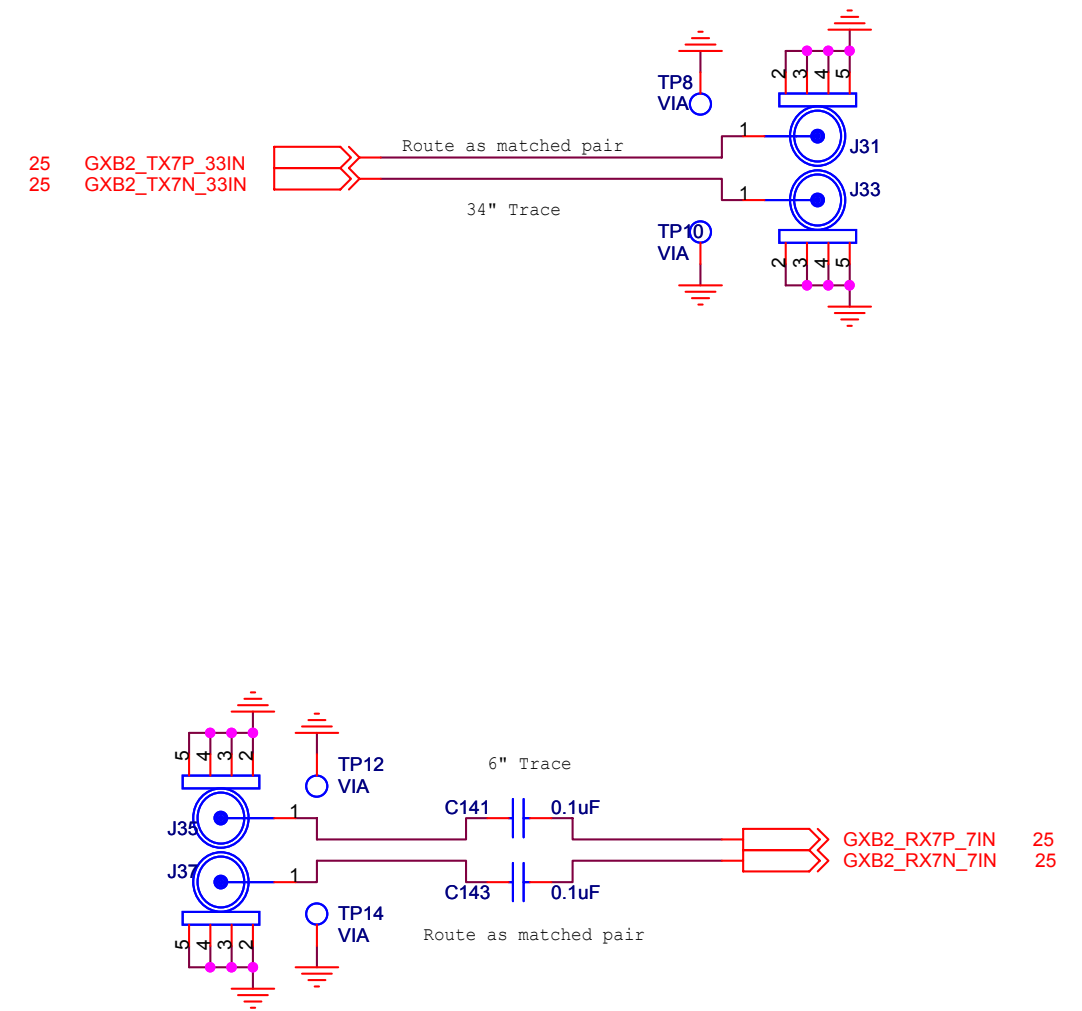
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Transceiver Channels (GXB0, GXB2)

GXB0 - TX0, RX0



GXB2 - Long TX, Short RX

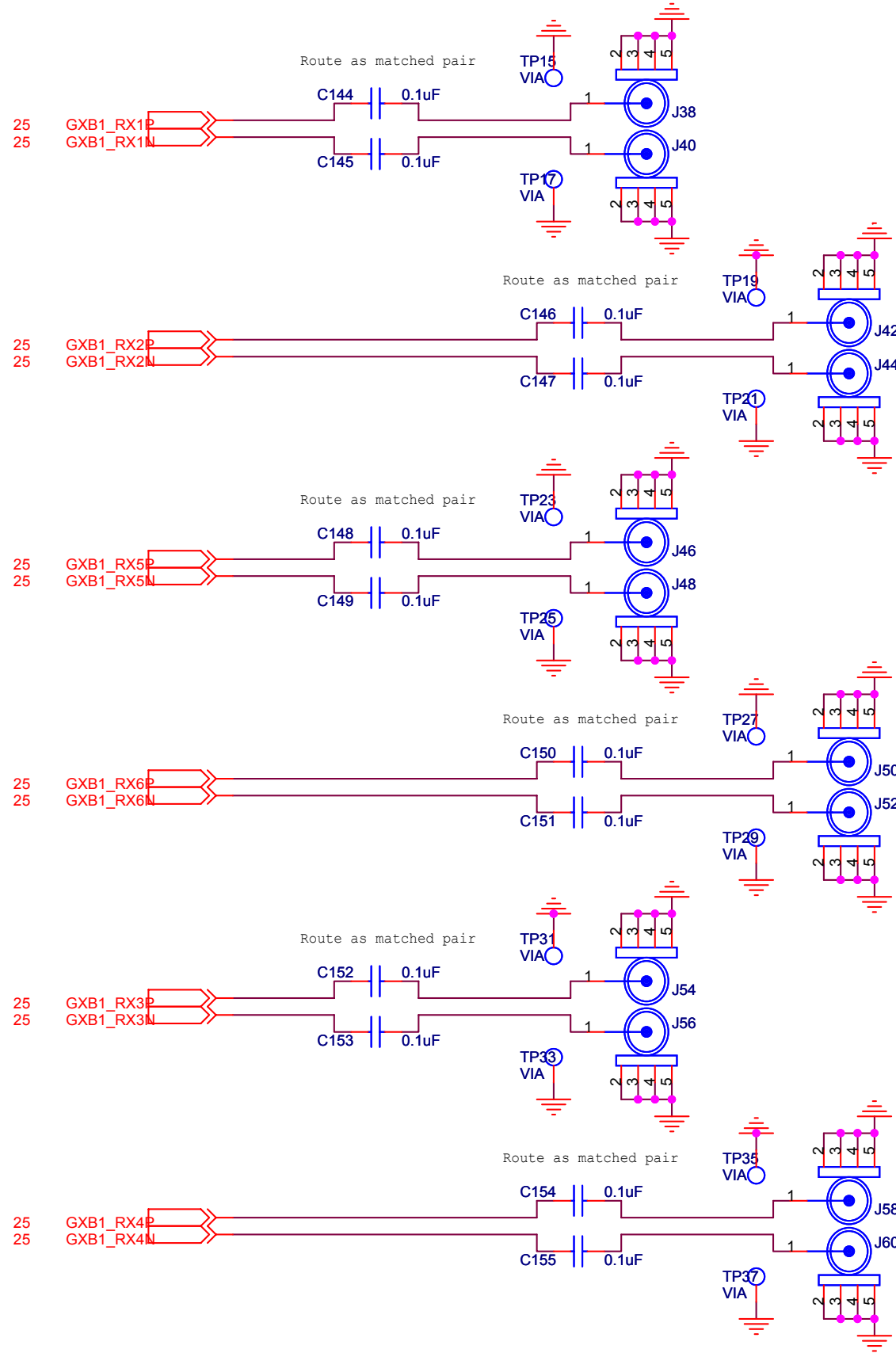


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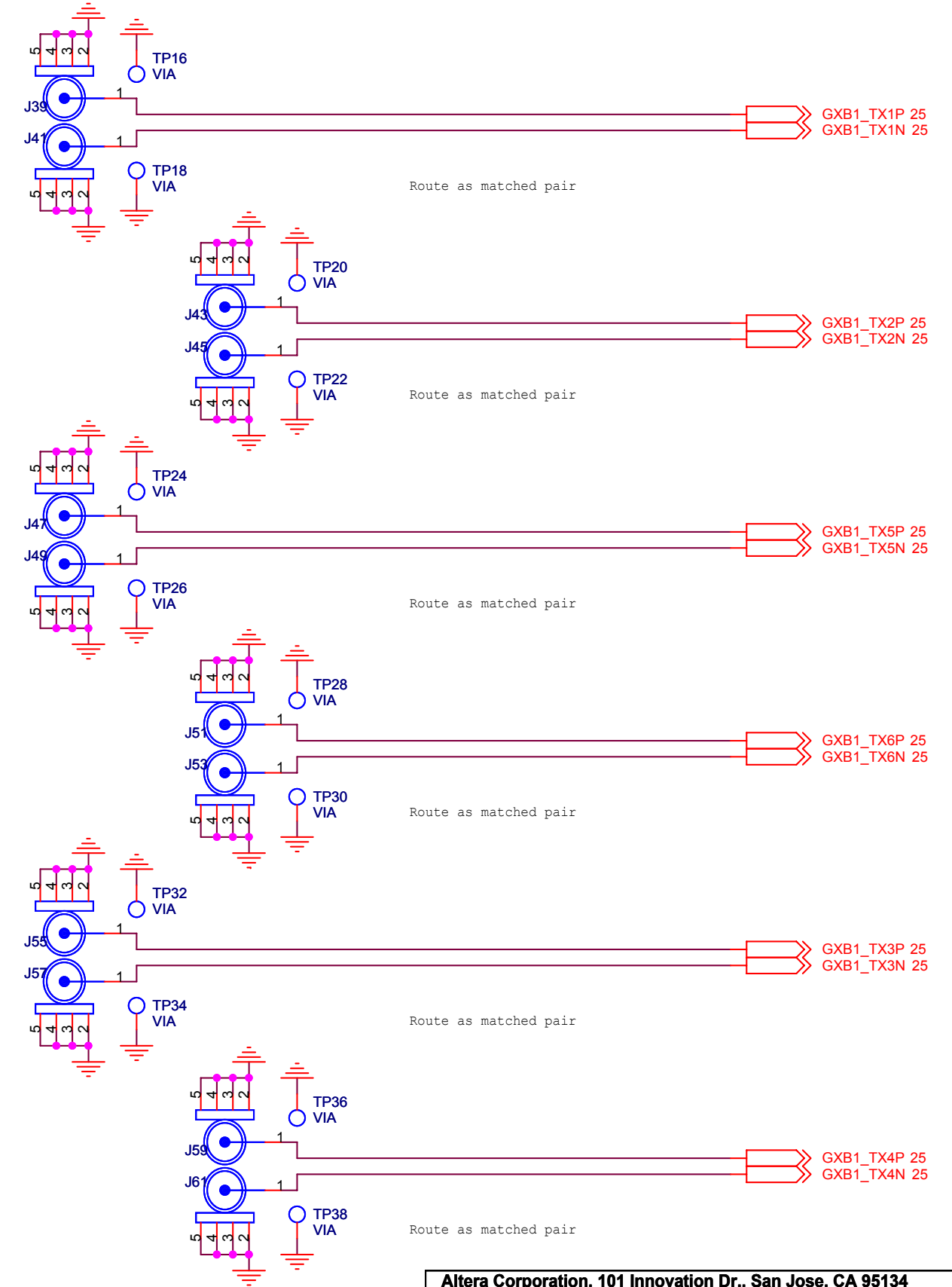
Transceiver Channels (GXB1)

Full 6 Channels

Receive

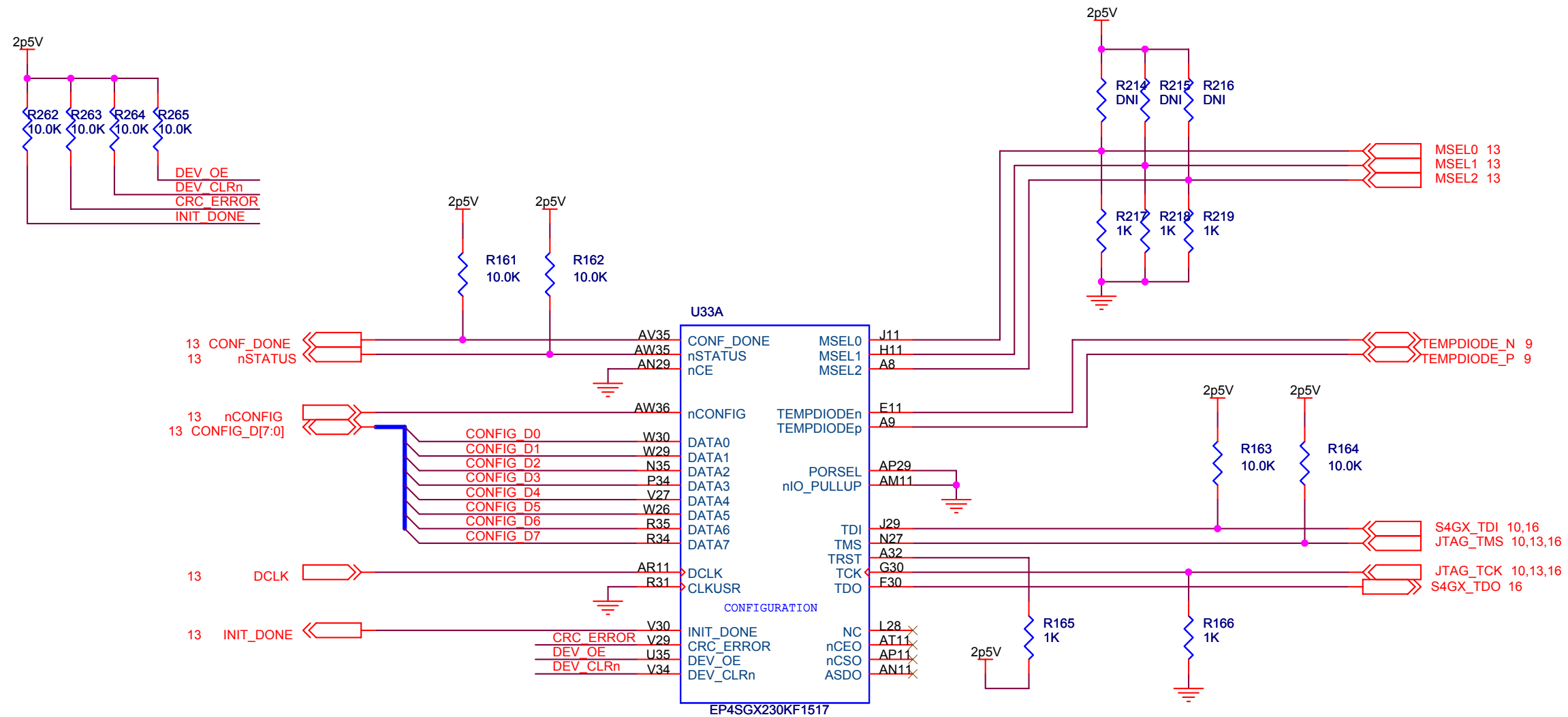


Transmit



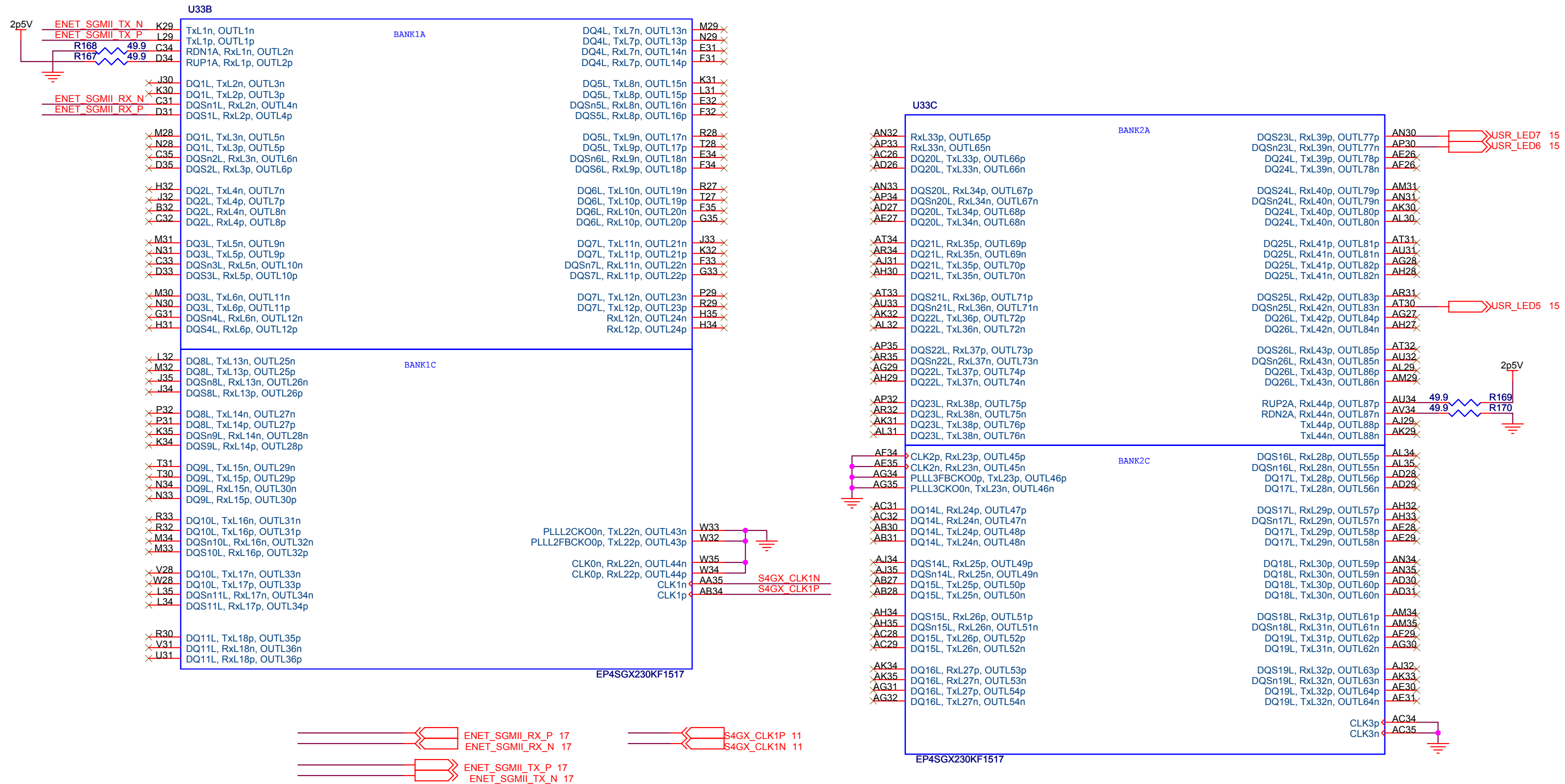
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STRATIX IVGX CONFIGURATION

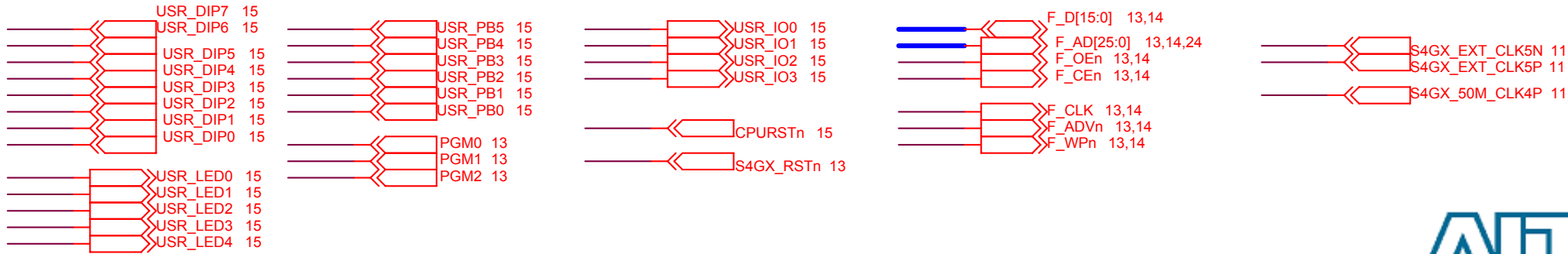
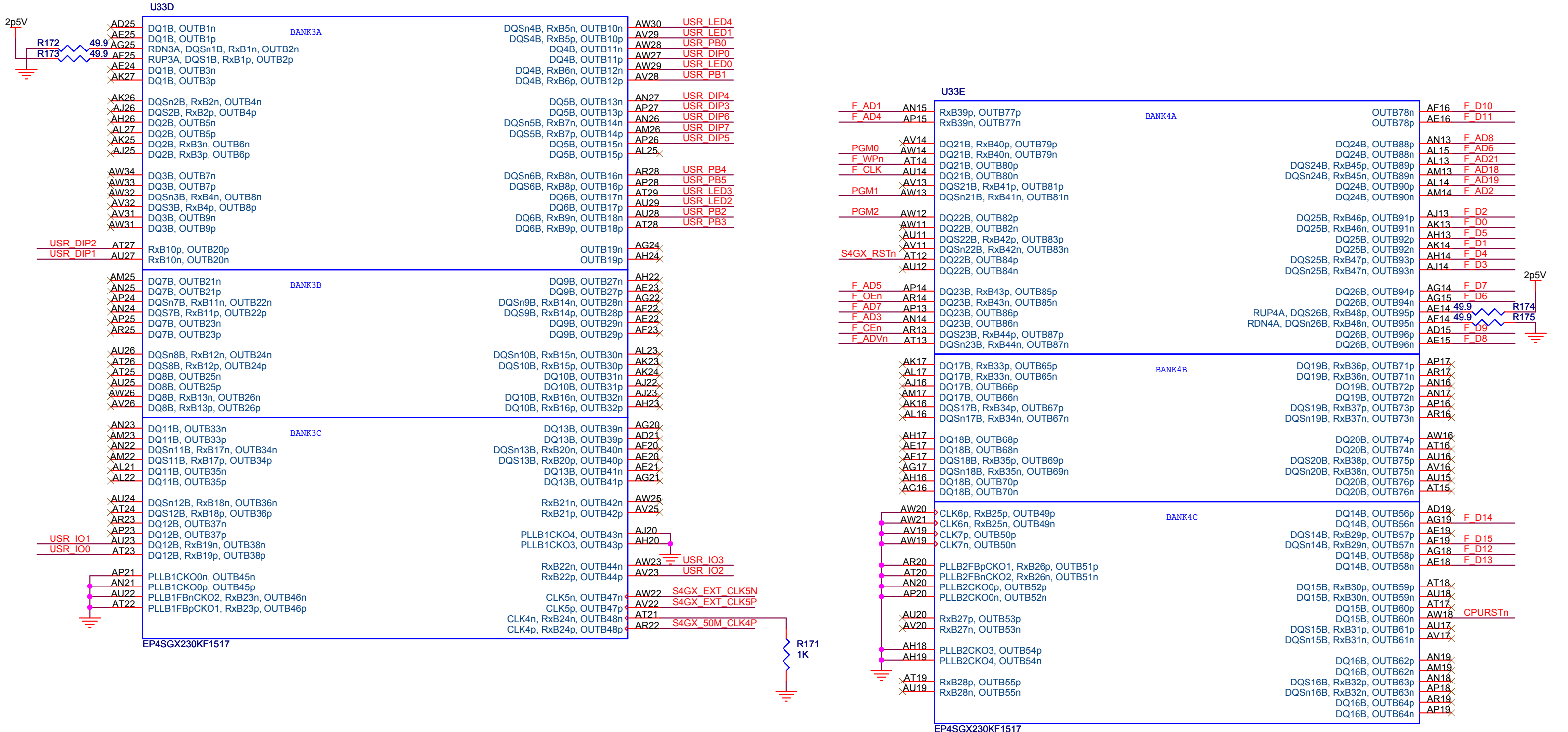


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STRATIX IVGX BANKS 1 & 2



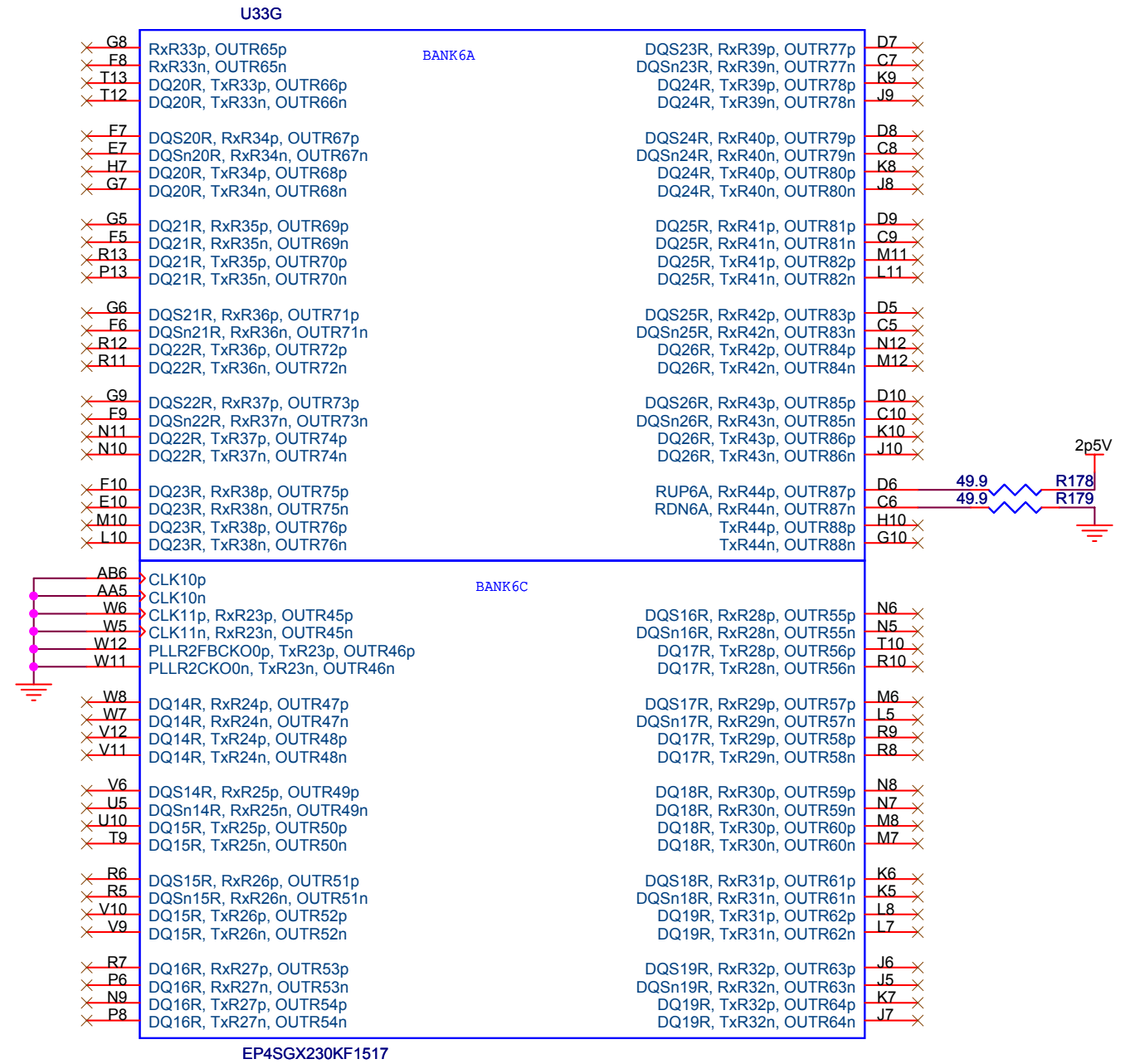
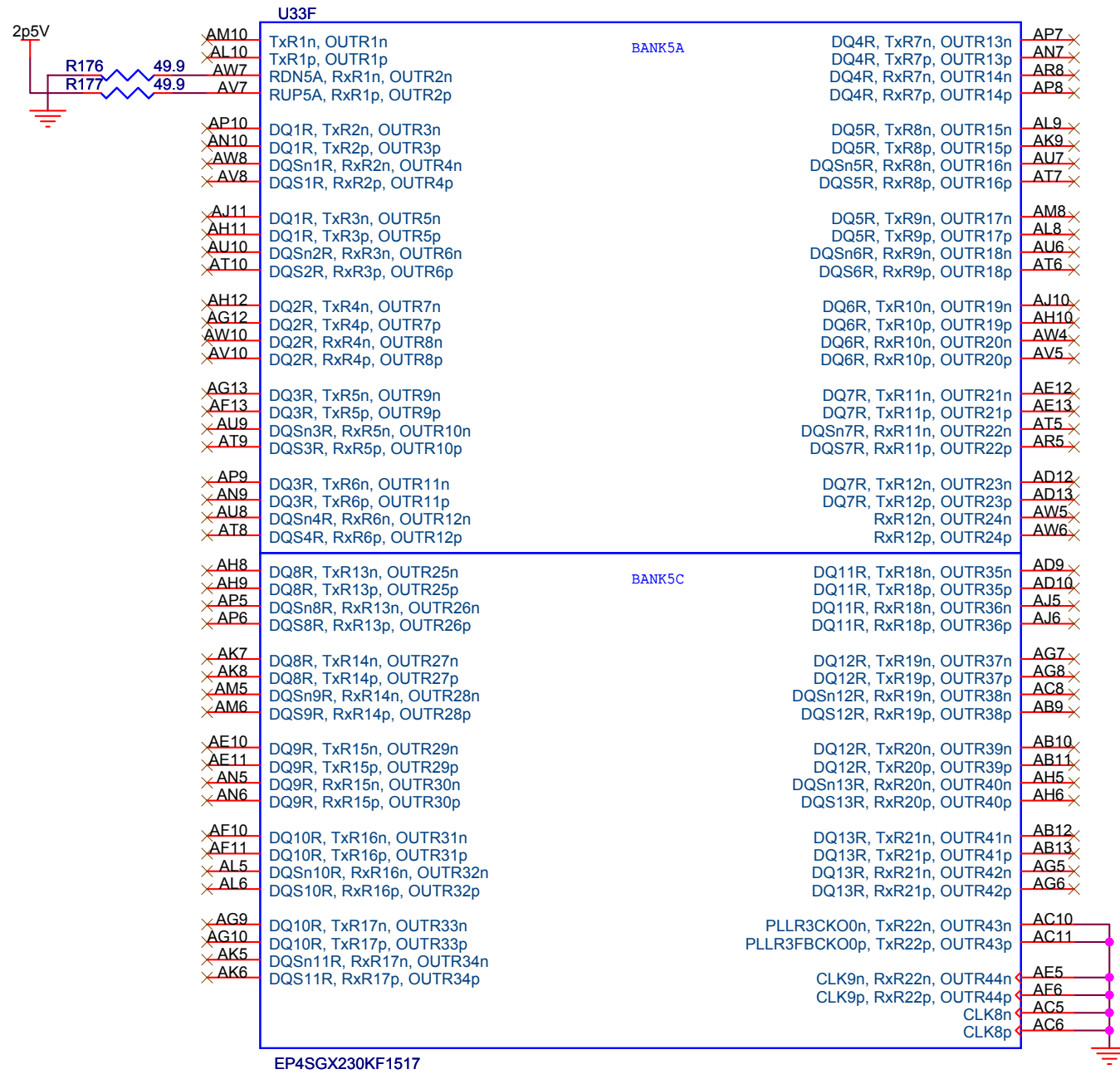
STRATIX IVGX BANKS 3 & 4



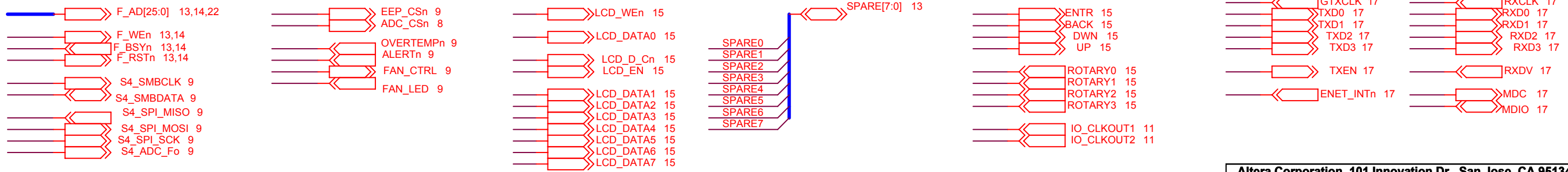
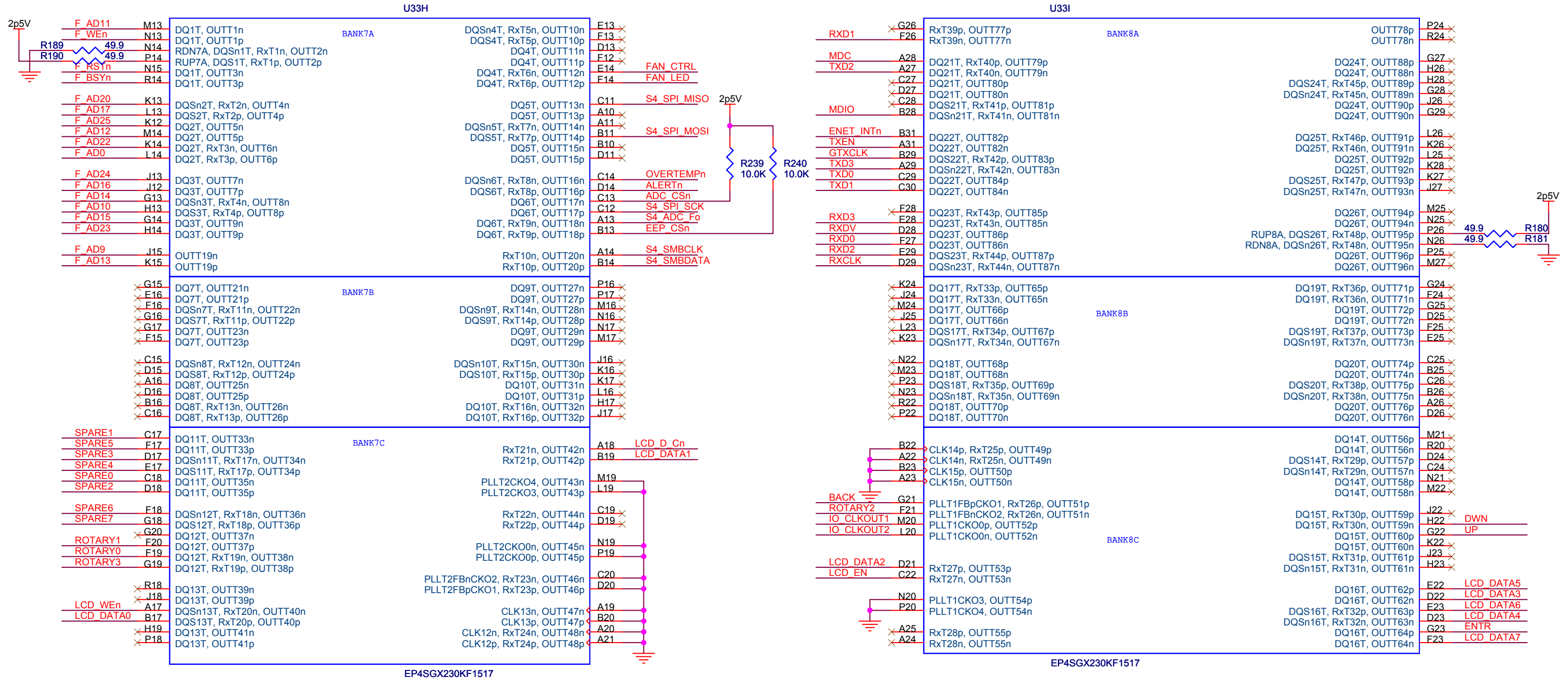
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STRATIX IVGX BANKS 5 & 6



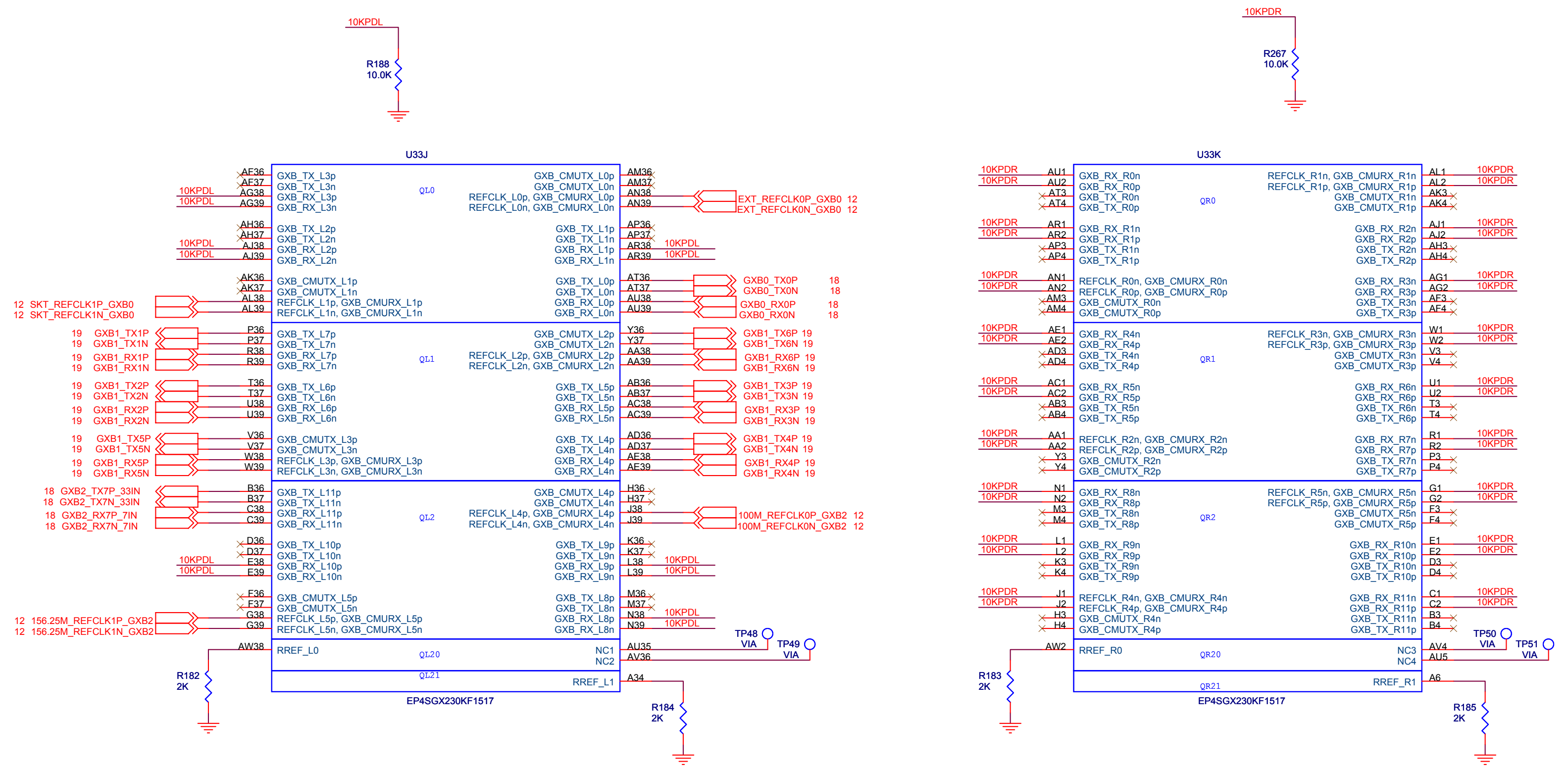
STRATIX IVGX BANKS 7 & 8



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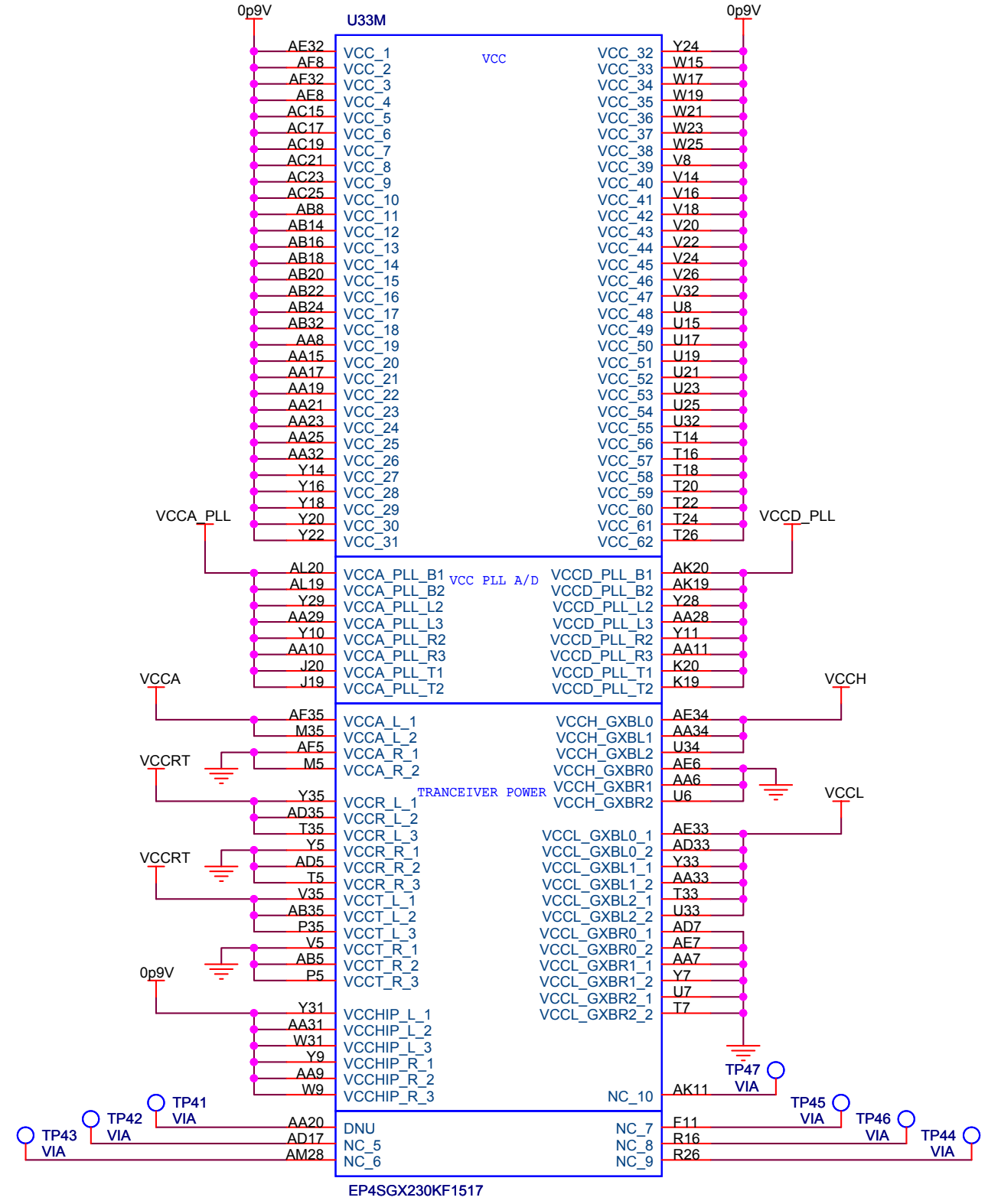
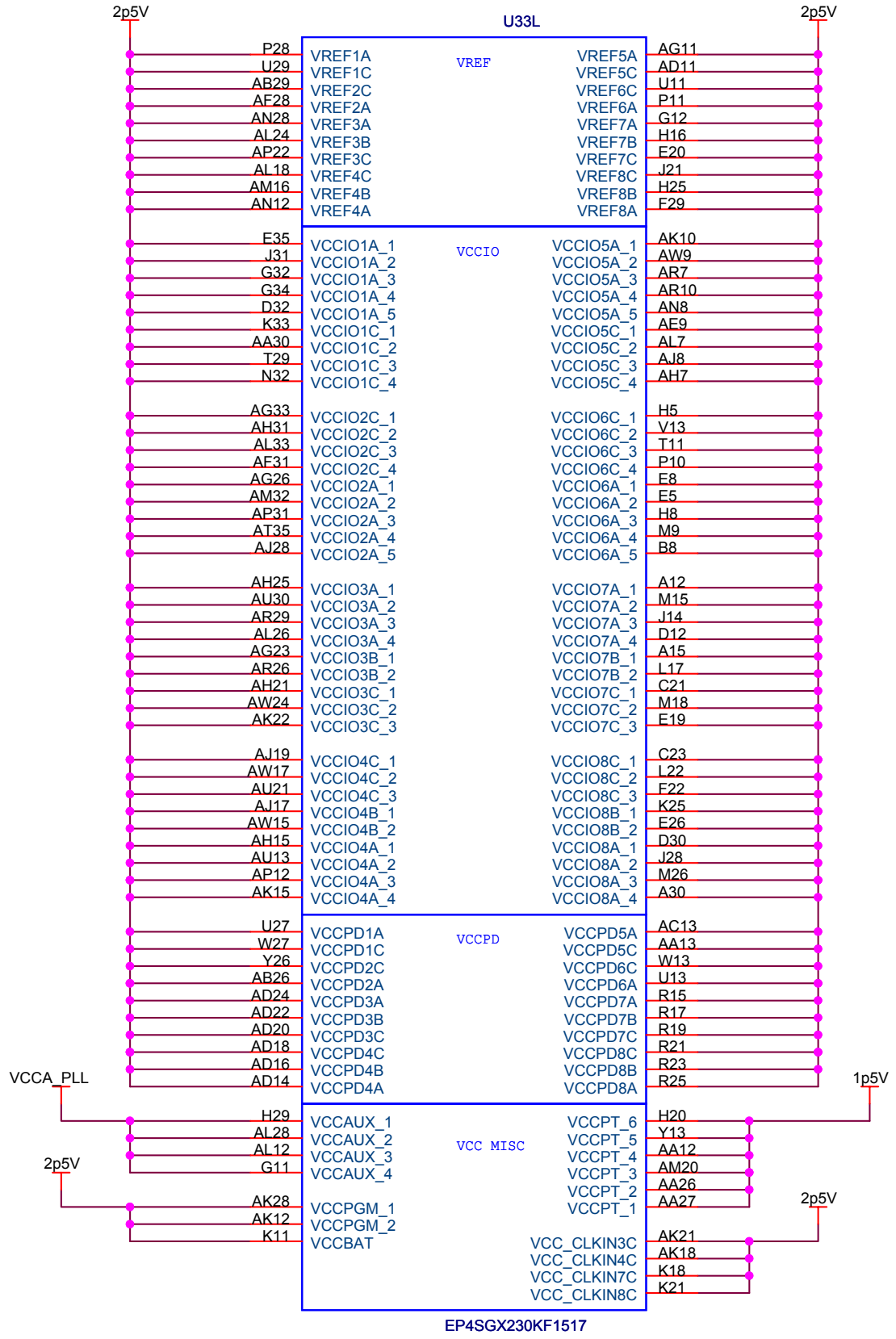


STRATIX IVGX TRANSCEIVERS

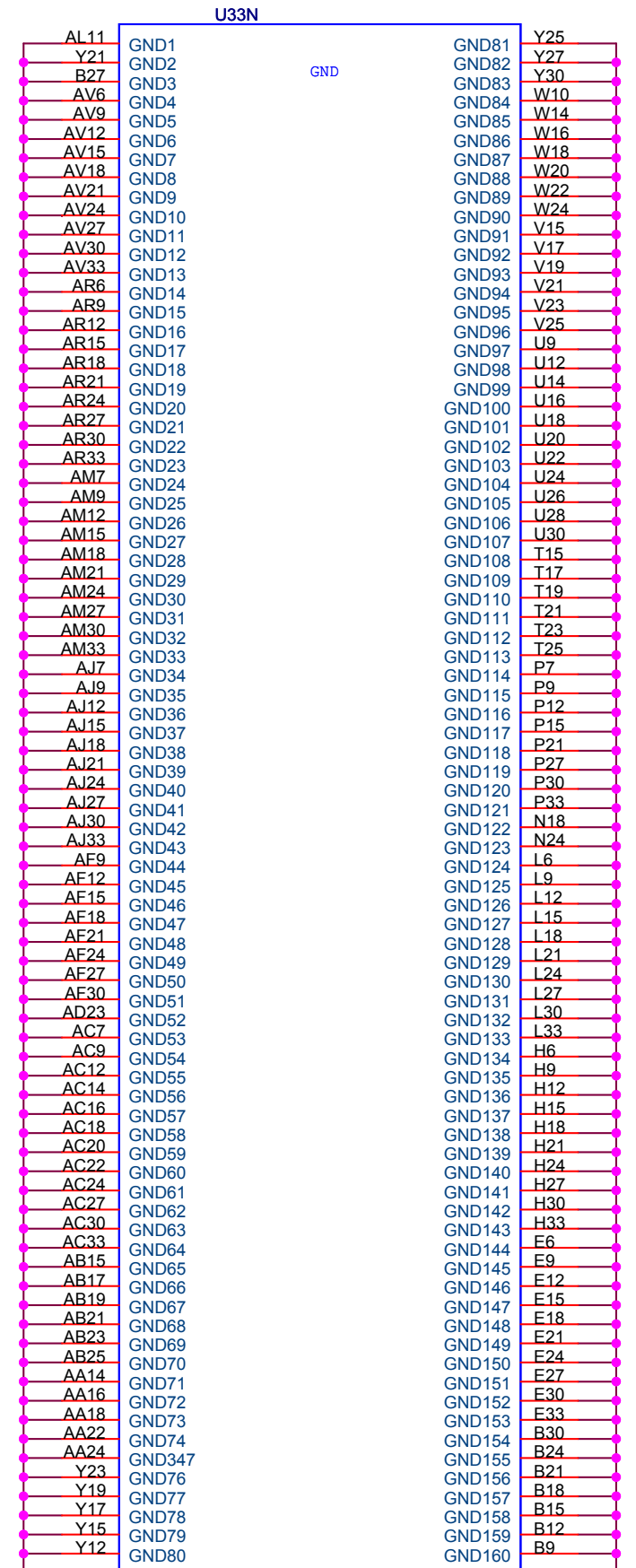


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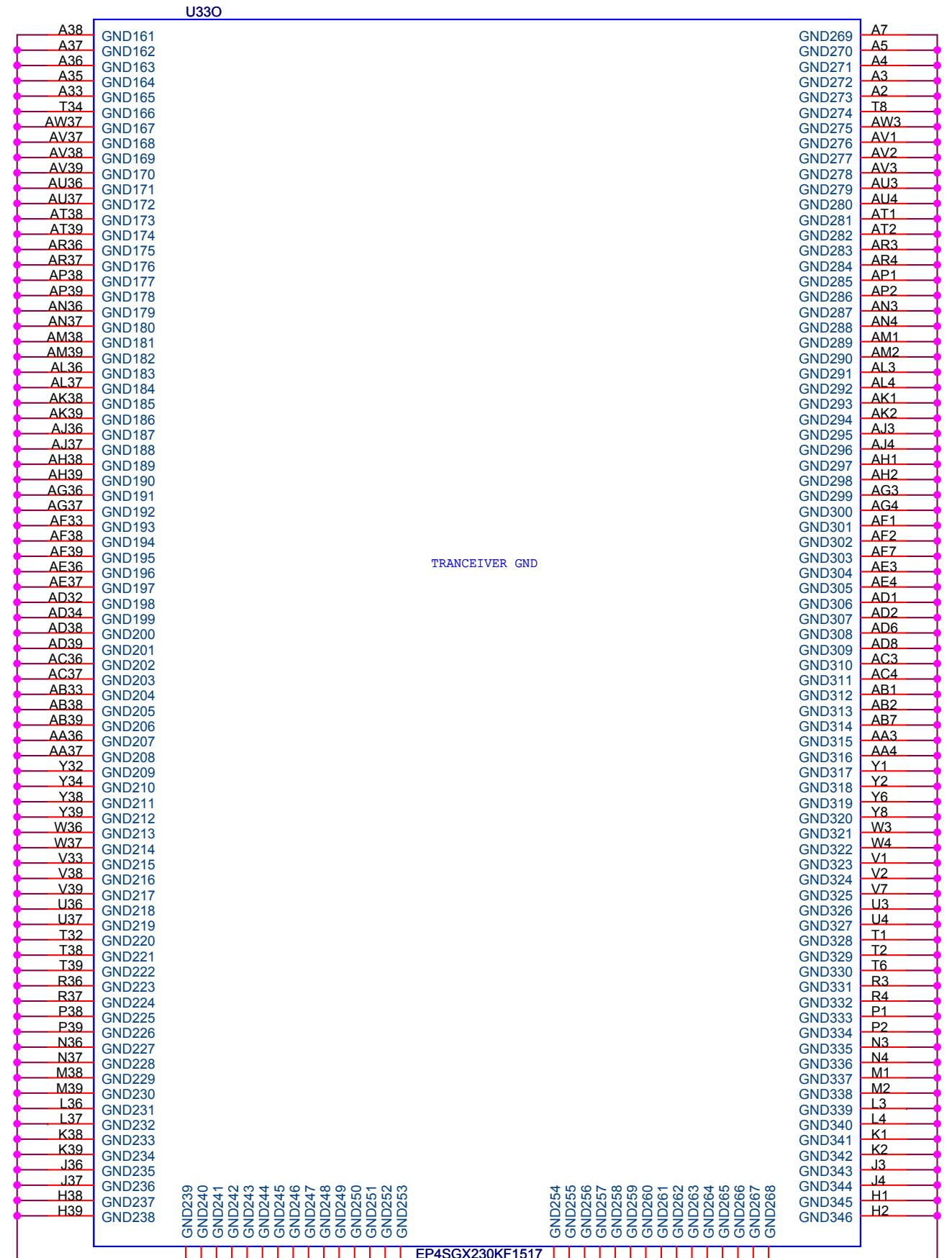
STRATIX IVGX POWER



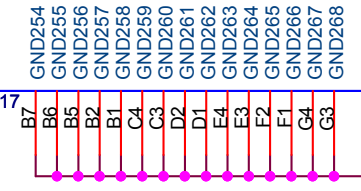
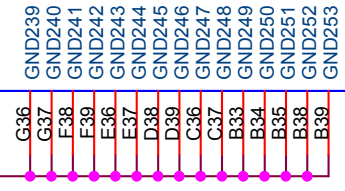
STRATIX IVGX GND



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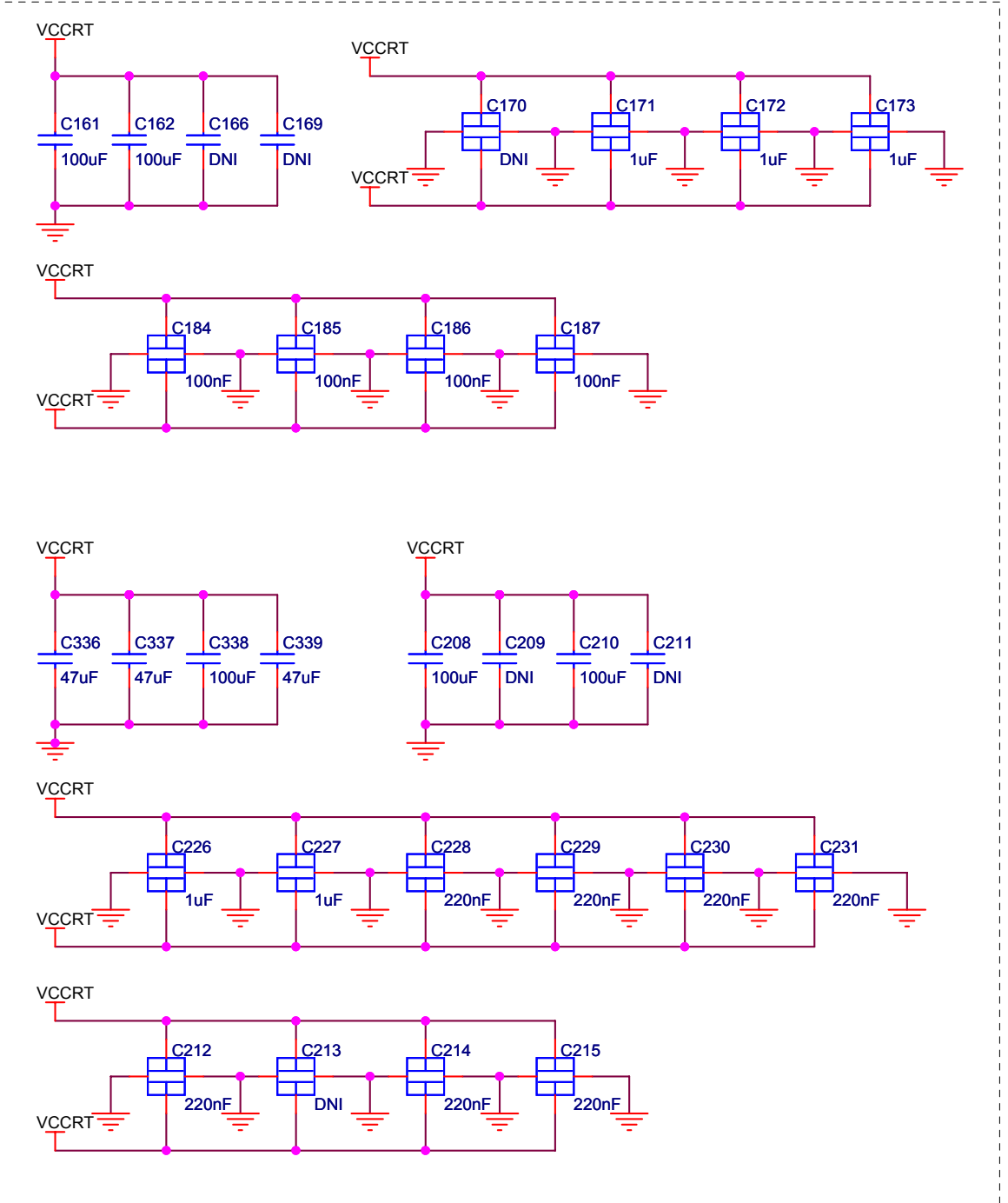
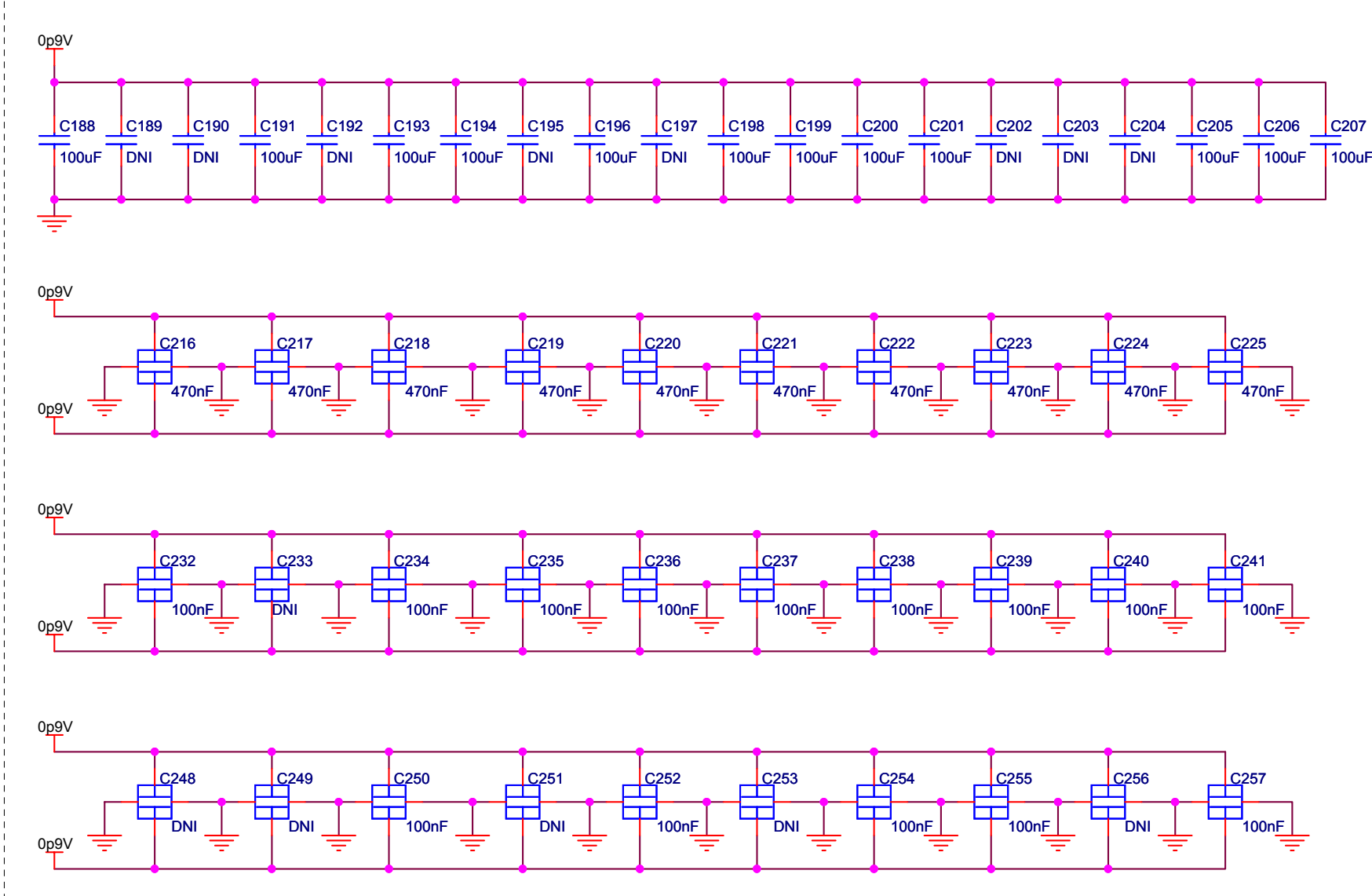
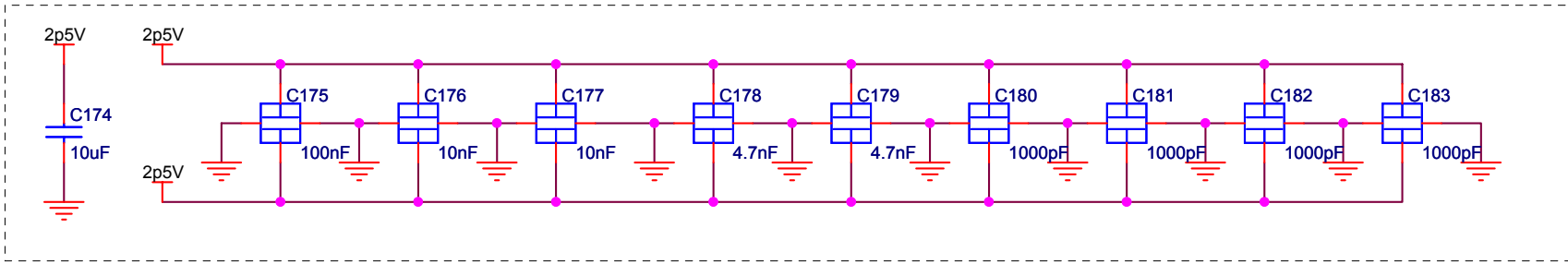
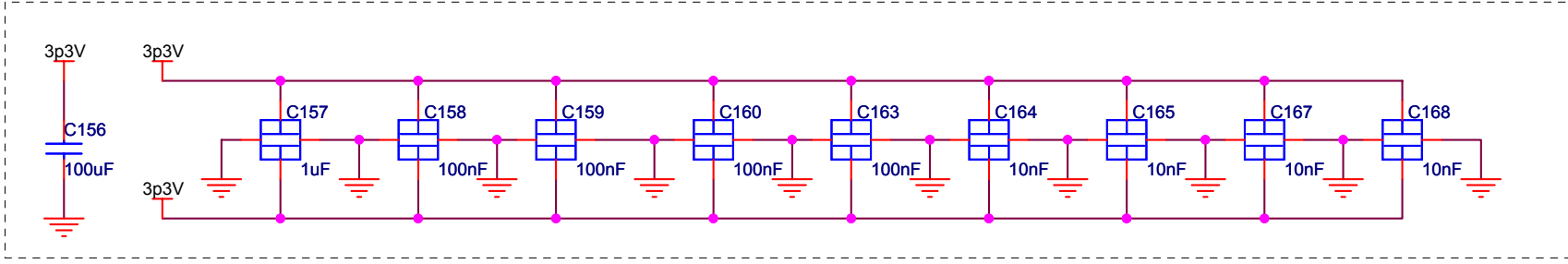
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Decoupling 1

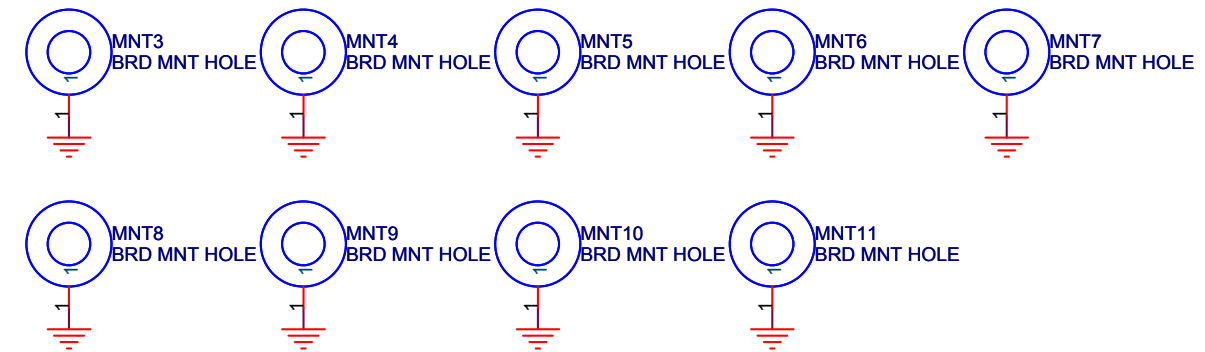
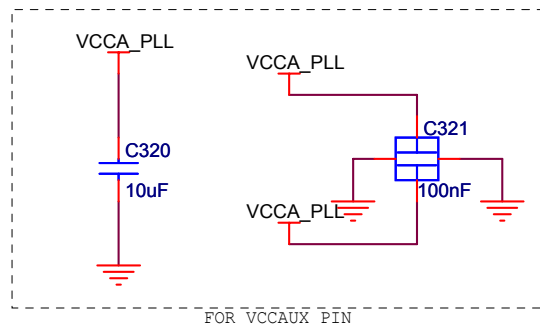
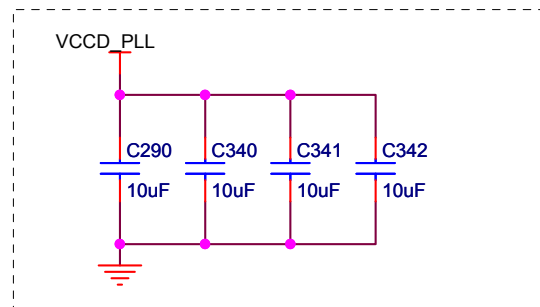
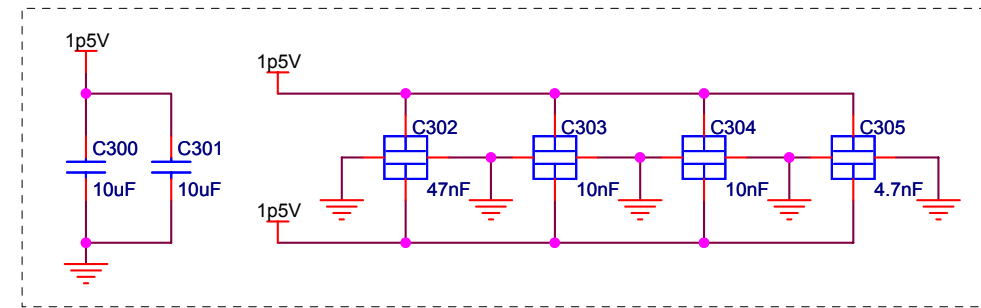
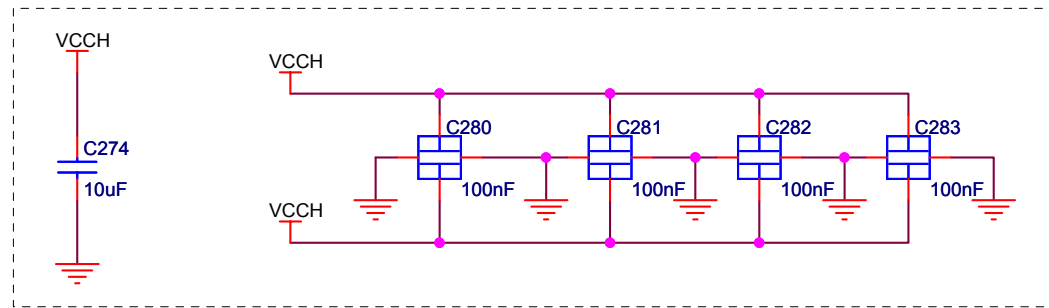
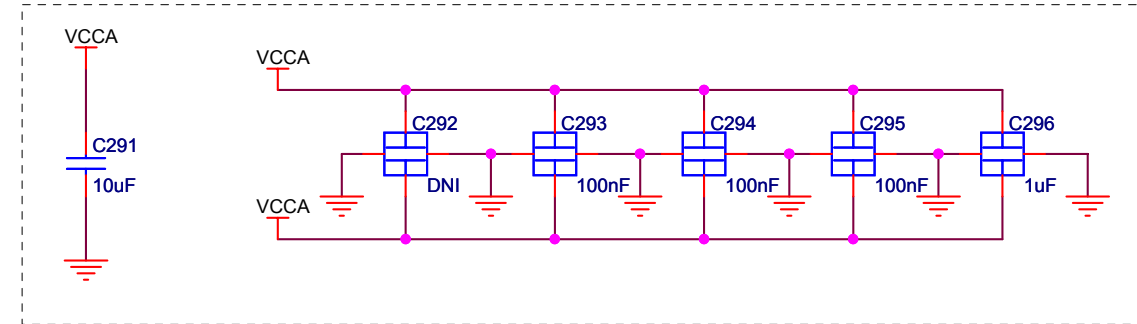
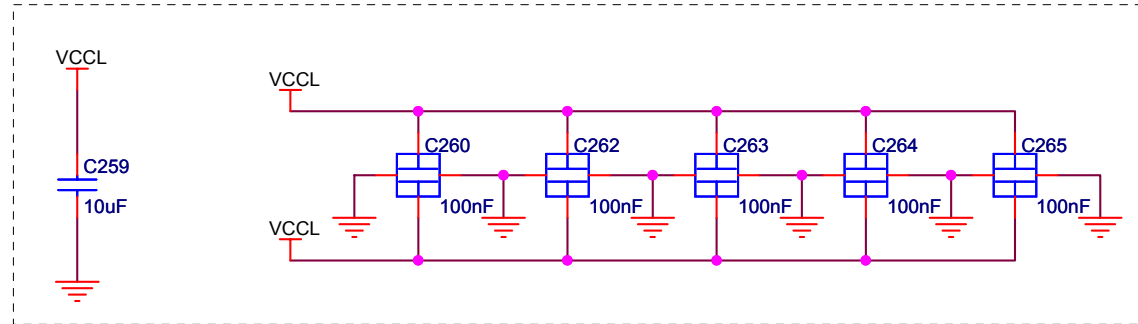
Place 6 vias minimum on each X2Y cap.



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Decoupling 2

Place 6 vias minimum on each X2Y cap.



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