RELAY CONTROL CHART

CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR

JUMPER TABLE

JP#	ON	OFF
1		
2		
3		
4		
5		

* SEE ASSEMBLY INSTRUCTIONS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

P.O SPEC.	BK/BD SPEC.	SOCKET OEM	OEM PART#	HANDLER

TEMPLATE ENGINEER -	DATE
HARDWARE SERVICES -	<DATE>
HARDWARE SYSTEMS -	
TEST ENGINEER -	
COMPONENT ENGINEER -	
TEST PROCESS -	
HARDWARE RELEASE -	
DESIGNER -	
PTD ENGINEER <PTD_ENGINEER>	<DATE>
CHECKER -	

SCHEMATIC

ANALOG DEVICES

```
HW TYPE    : Customer Evaluation
Product(s): AD7606C-18
           : n/a
PACKAGE    : 64-lead 12X12_MM LQFP-family
           : Pitch-pitch StyleVendor Style
<User Define>
<User Define>
<User Define>
```

MASTER PROJECT TEMPLATE: TBD
TESTER TEMPLATE: no_template

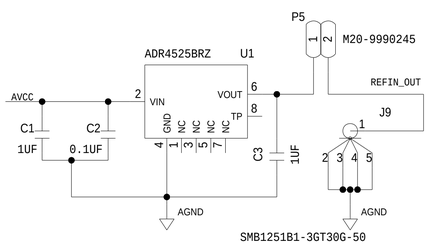
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS: X.XX +-0.010, X.XXX +-0.005
FRACTIONS: +-1/32
ANGLES: +-2

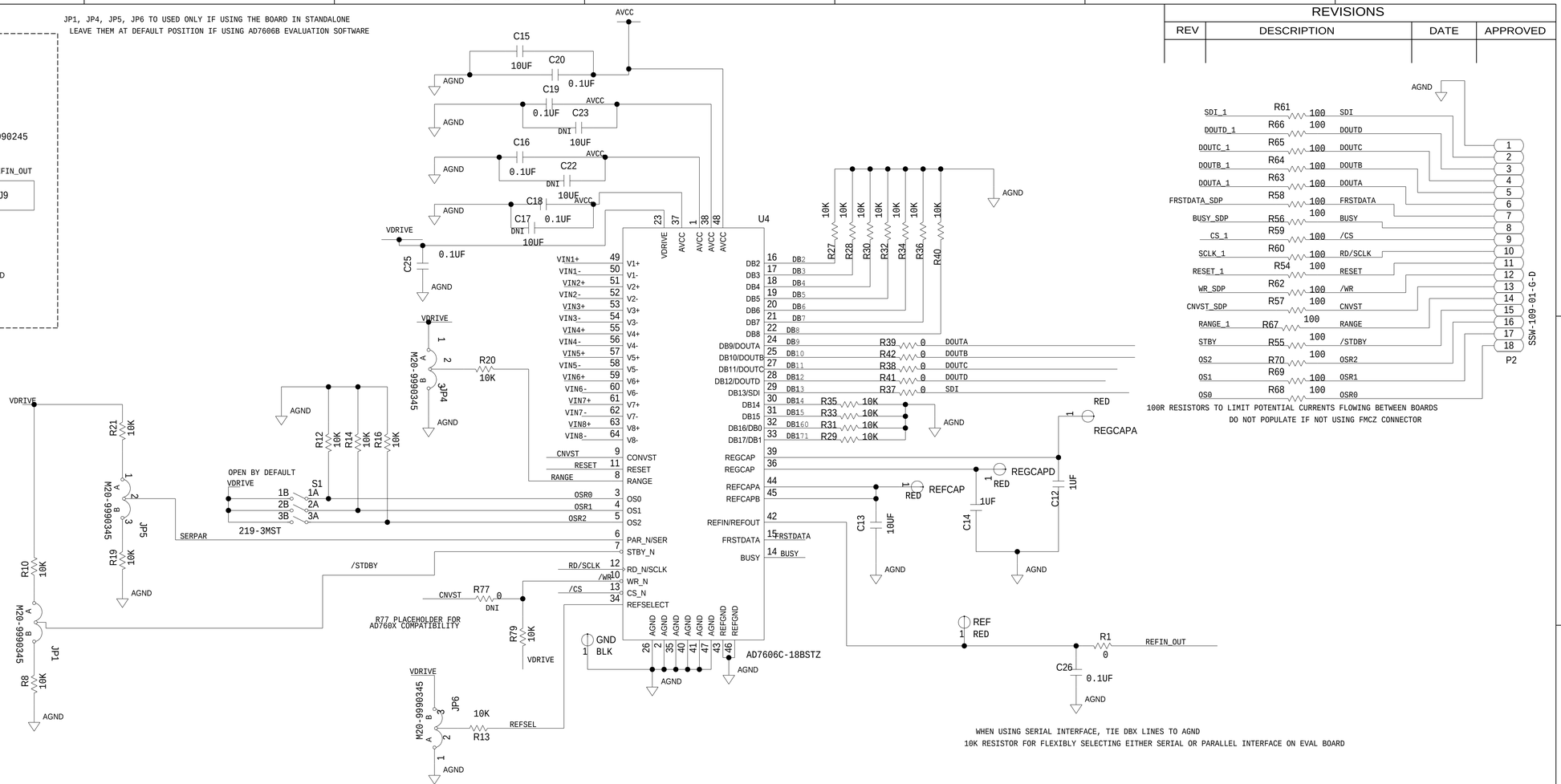
DRAWING NO. 02_057655
REV. B

SIZE D | SCALE 1:1 | CODE ID NO. CodeID | SHEET 1 OF 4

JP1, JP4, JP5, JP6 TO USED ONLY IF USING THE BOARD IN STANDALONE
LEAVE THEM AT DEFAULT POSITION IF USING AD7606B EVALUATION SOFTWARE

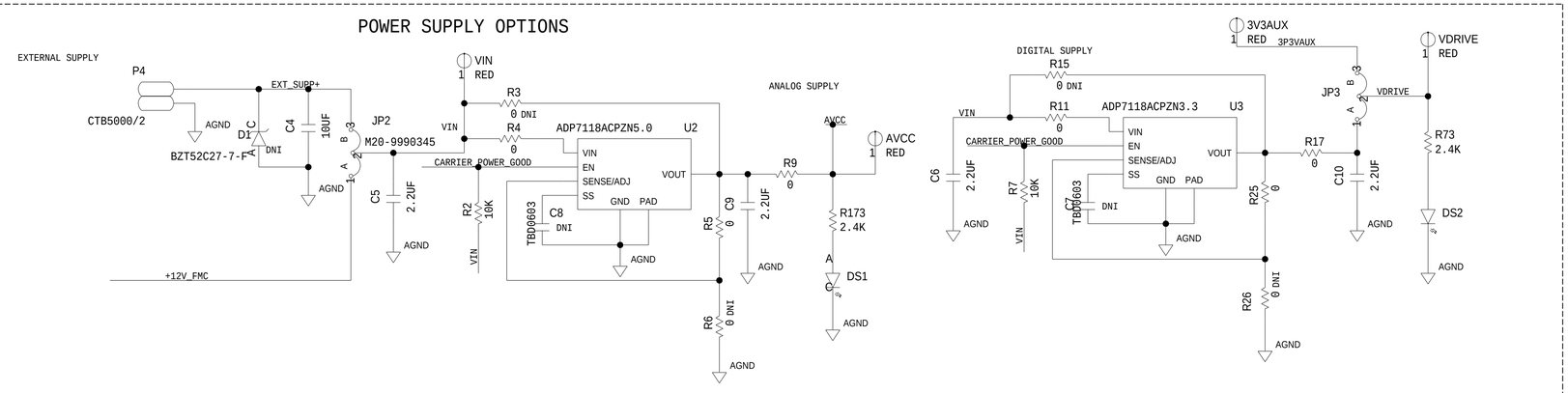
EXTERNAL REFERENCE

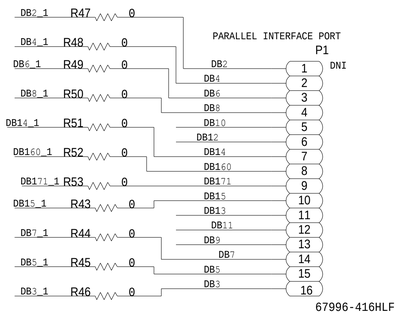




WHEN USING SERIAL INTERFACE, TIE DBX LINES TO AGND
10K RESISTOR FOR FLEXIBLY SELECTING EITHER SERIAL OR PARALLEL INTERFACE ON EVAL BOARD

POWER SUPPLY OPTIONS





REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

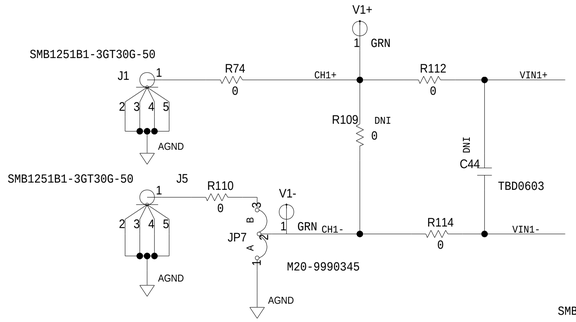
ANALOG DEVICES

SCHEMATIC

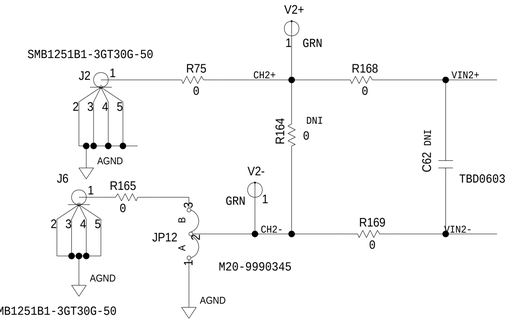
HW TYPE : Customer Evaluation
Product(s): AD7606C-18
: n/a

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_057655	B
PTD ENGINEER	SIZE / SCALE	SHEET 2 OF 4
<PTD_ENGINEER>	D / 1:1	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



JUMPER LINK ALLOWS SELECTION BETWEEN SINGLE-ENDED AND DIFFERENTIAL



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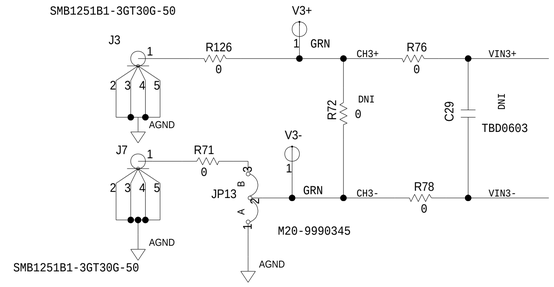

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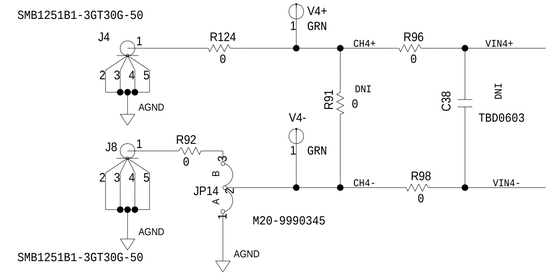

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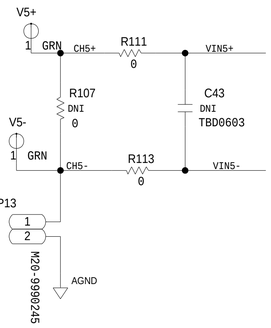
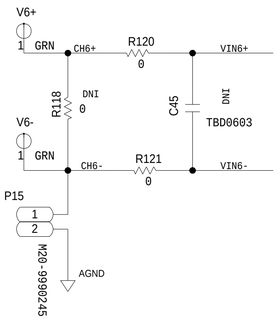
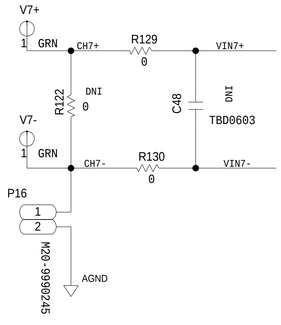
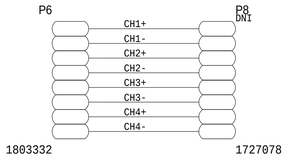
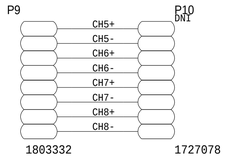
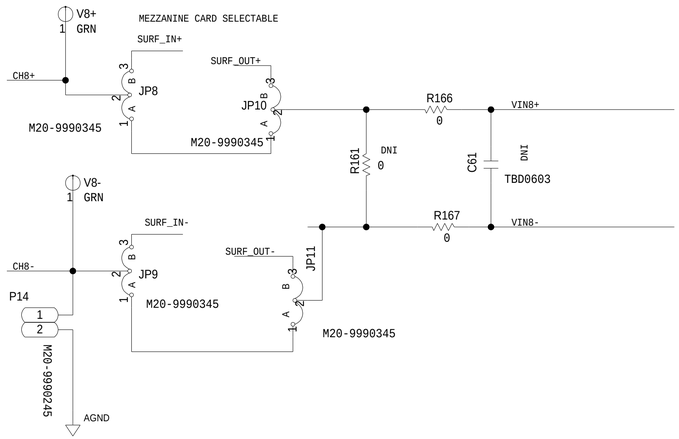




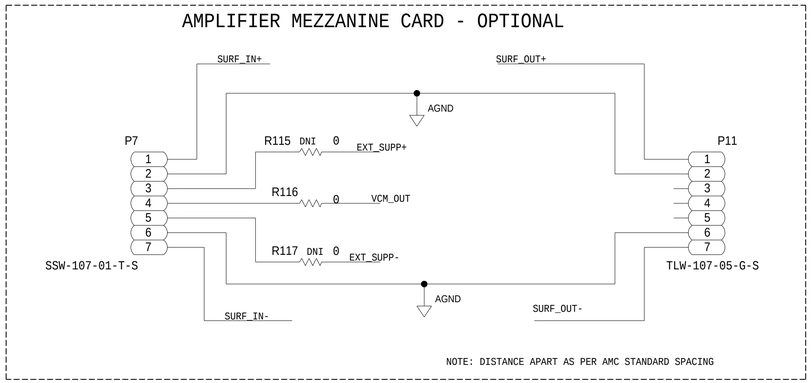








JUMPER LINK ALLOWS SELECTION BETWEEN SINGLE-ENDED AND DIFFERENTIAL



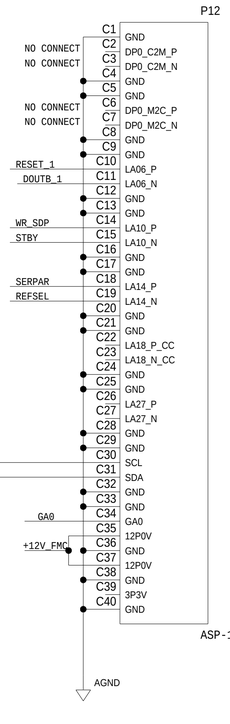
ANALOG DEVICES	SCHEMATIC		
	HW TYPE : Customer Evaluation Product(s): AD7606C-18 : n/a		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_057655	REV B
	PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE 1:1	SHEET 3 OF 4

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

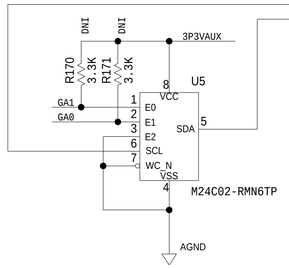
FPGA FMC CONNECTIONS

LIST OF FMC-LPC CONNECTOR PINS THAT
ARE NOT CONNECTED ON THE SDP-H1:

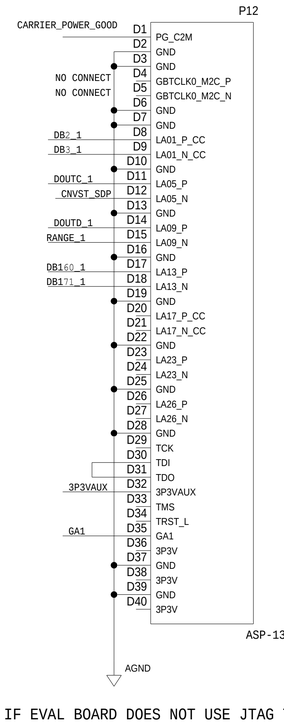
C2 (DP0_C2M_P)
C3 (DP0_C2M_N)
C6 (DP0_M2C_P)
C7 (DP0_M2C_N)
D4 (GBTCLK0_M2C_P)
D5 (GBTCLK0_M2C_N)
H1 (VREF_A_M2C)



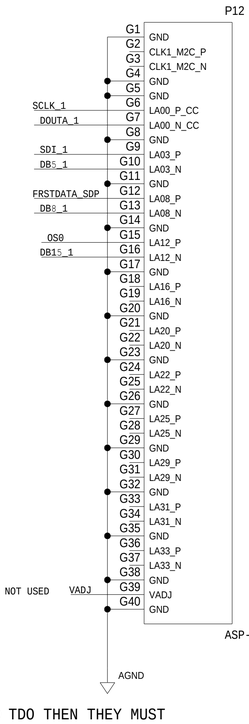
EEPROM

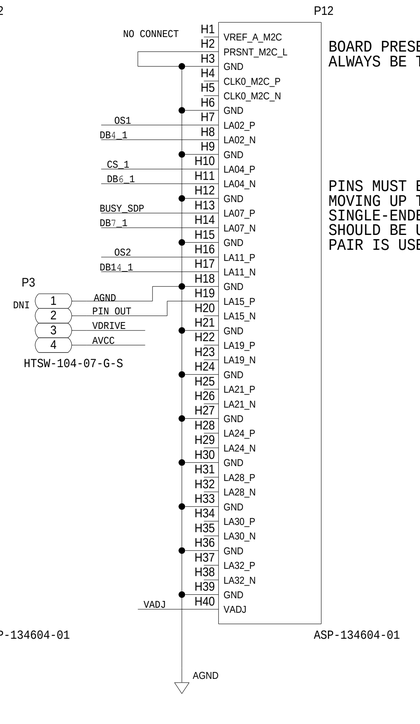


EEPROM REQUIRED IN VITA57.1 STANDARD.
I2C LINE PULL-UP RESISTORS ON FPGA BOARD.
I2C ADDRESS SET BY CONTROLLER BOARD.



IF EVAL BOARD DOES NOT USE JTAG TDI AND TDO THEN THEY MUST
BE SHORTED TOGETHER (AS SHOWN) SO AS NOT TO BREAK JTAG CHAIN





BOARD PRESENT PIN (H2) MUST
ALWAYS BE TIED TO GROUND

PINS MUST BE ASSIGNED STARTING WITH LA00 AND
MOVING UP THE LA BUS UNTIL IT IS FULL. WHEN
SINGLE-ENDED SIGNALING IS USED, THE _P LINE
SHOULD BE USED BEFORE THE _N LINE OF THE SAME
PAIR IS USED.

POWER SUPPLIES:
12P0V. 1A MAX CURRENT LIMIT
3P3V. 3A MAX CURRENT LIMIT
VADJ. 2A MAX CURRENT LIMIT. 1.2V TO 3.3V.

ANALOG DEVICES

SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): AD7606C-18
: n/a

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_057655	B
PTD ENGINEER	SIZE / SCALE	SHEET 4 OF 4
<PTD_ENGINEER>	D / 1:1	