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RELAY CONTROL CHART

CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR

JUMPER TABLE

JP#	ON	OFF
1		
2		
3		
4		
5		

* SEE ASSEMBLY INSTRUCTIONS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	30JUL25	D. HARRINGTON
B	AS PER ECR-128314	07NOV25	D. HARRINGTON
C	AS PER ECR-130698	27MAR26	D. HARRINGTON

EV-SC846-SOM

ADSP-SC846 for SOM 2.0 Evaluation System

Last Update: 03-26-2026

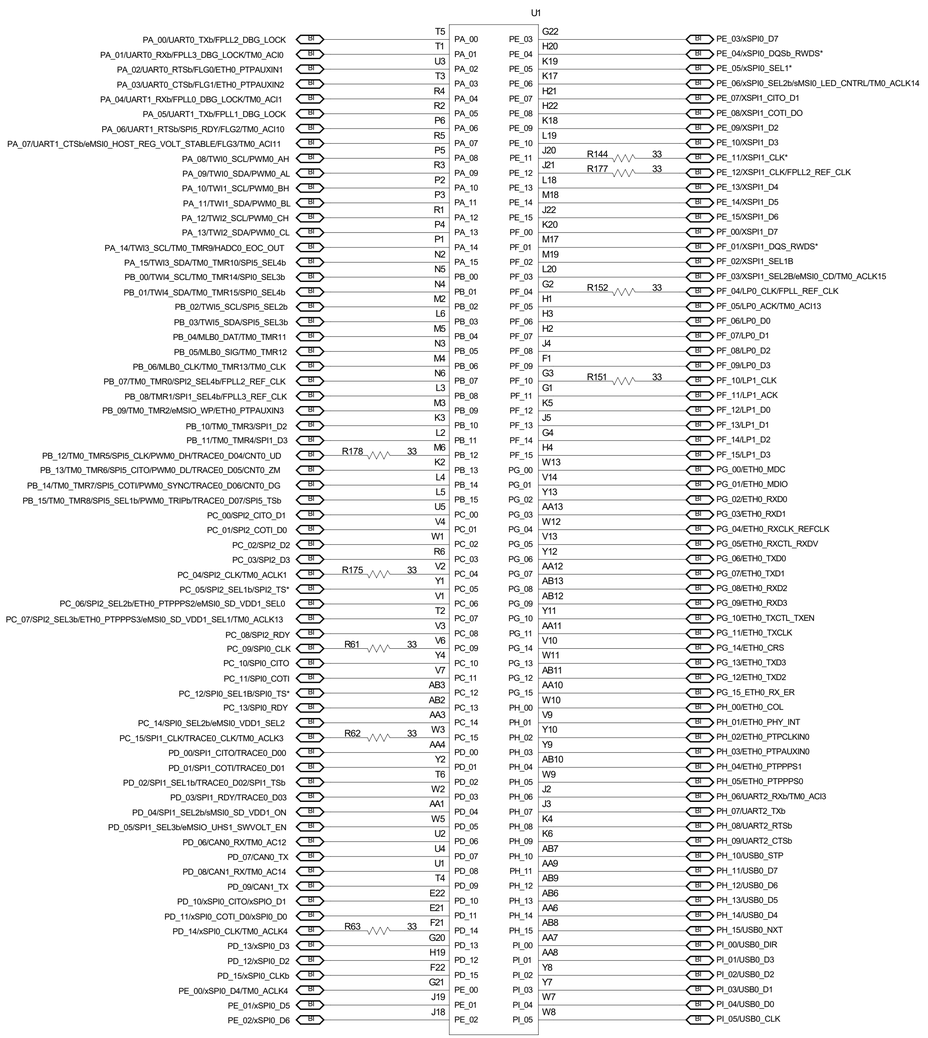
P.O SPEC.	BK/BD SPEC.	SOCKET OEM	OEM PART#	HANDLER

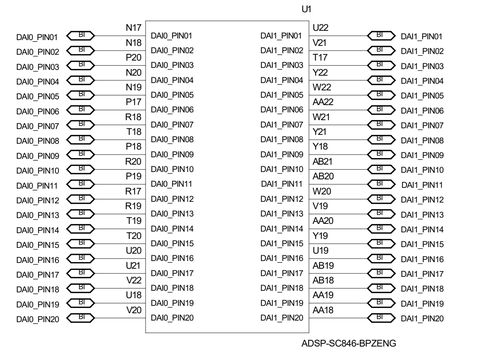
TEMPLATE ENGINEER -	DATE	SCHEMATIC
HARDWARE SERVICES M. VALE	30JUL25	HW TYPE : Customer Evaluation Z Product(s): ADSP-SC846 : SOM
HARDWARE SYSTEMS -		PACKAGE : LeadCount-lead BodySize PackageType-family : Pitch-pitch StyleVendor Style
TEST ENGINEER -		
COMPONENT ENGINEER N. CATALAN	30JUL25	<User Define> <User Define> <User Define>
TEST PROCESS -		
HARDWARE RELEASE E. CONDA	30JUL25	
DESIGNER G. ARON	30JUL25	MASTER PROJECT TEMPLATE: GENERIC_D_SIZE_FORMAT TESTER TEMPLATE: 067706_b
PTD ENGINEER D. HARRINGTON	30JUL25	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS X.XX +-0.010 X.XXX +-0.005 FRACTIONS +-1/32 ANGLES +-2
CHECKER -		

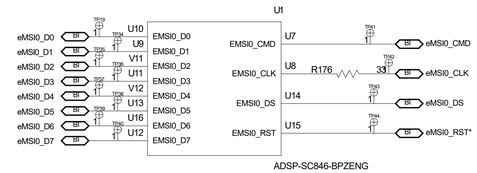
DRAWING NO. 02_083724 | REV. C

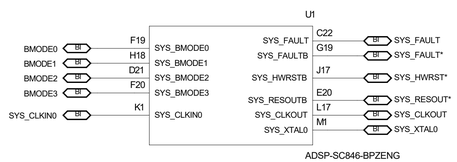
SIZE D | SCALE 1:1 | CODE ID NO. CodeID | SHEET 1 OF 12

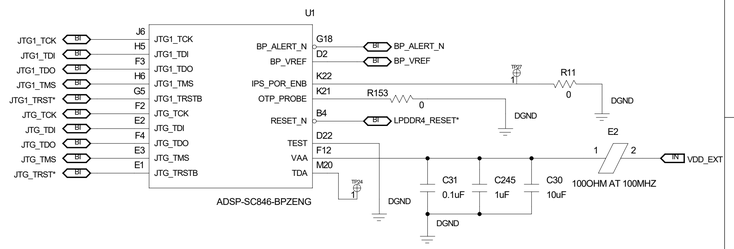
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

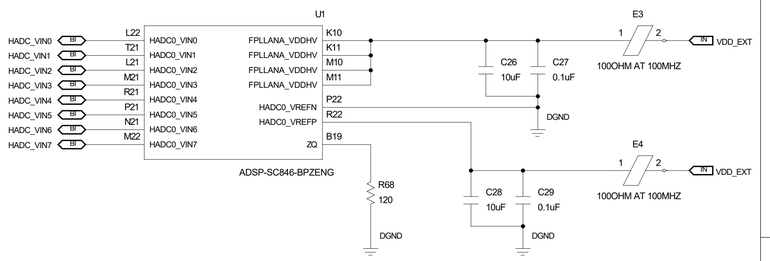












SCHEMATIC

ANALOG DEVICES

HW TYPE : Customer Evaluation Z
Product(s): ADSP-SC846
: SOM

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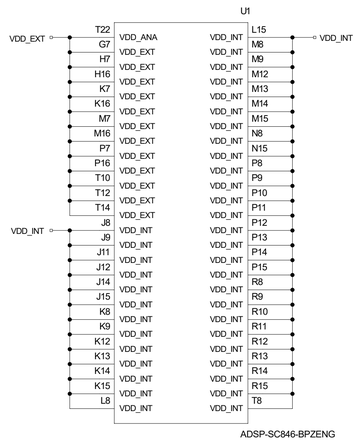
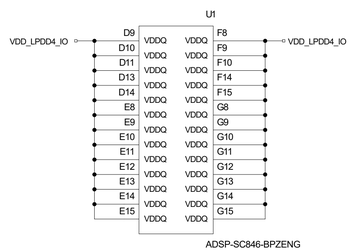
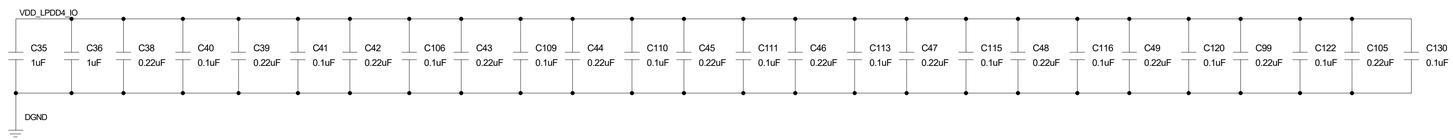
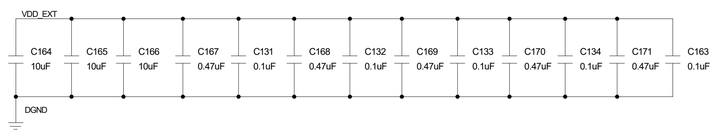
DESIGN VIEW	DRAWING NO.	REV
$DESIGN_VIEW	02_083724	C
PTD ENGINEER: D. HARRINGTON	SIZE: D / SCALE: 1:1	SHEET 2 OF 12

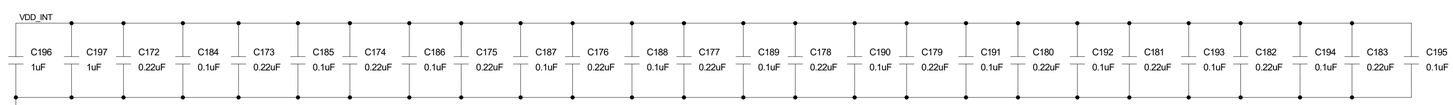
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

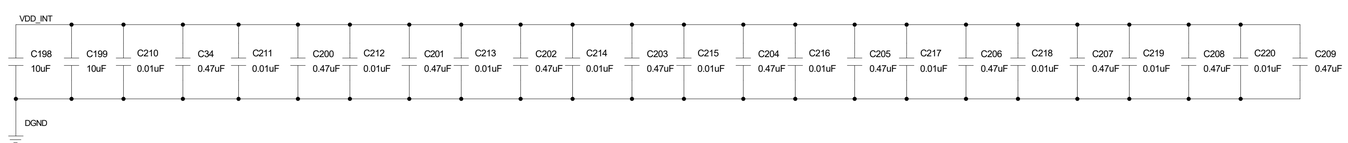


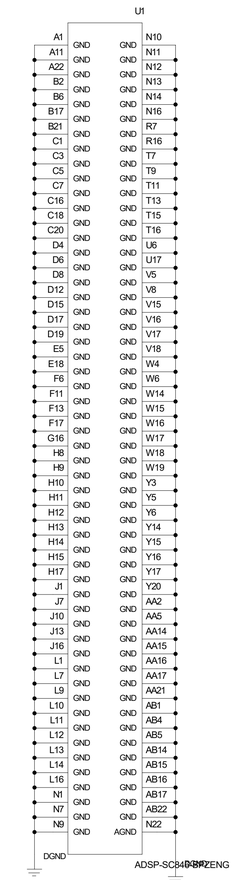












ANALOG DEVICES	SCHEMATIC			
	HW TYPE : Customer Evaluation Z Product(s): ADSP-SC846 : SOM			
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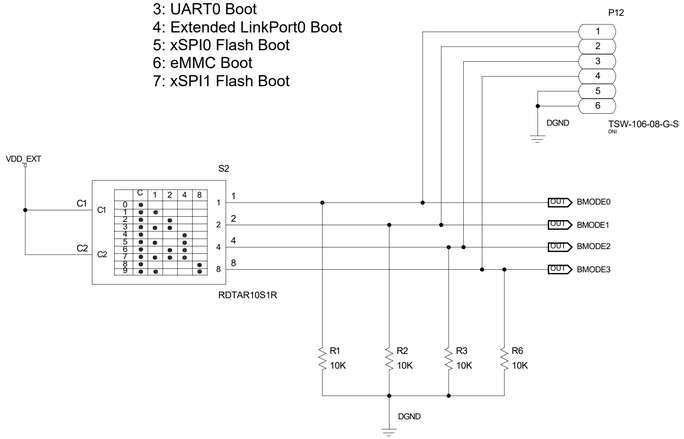
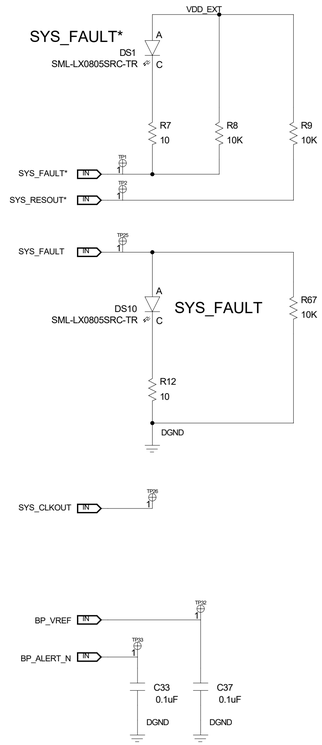
	PTD ENGINEER D. HARRINGTON	SIZE D	SCALE 1:1	SHEET 3 OF 12

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

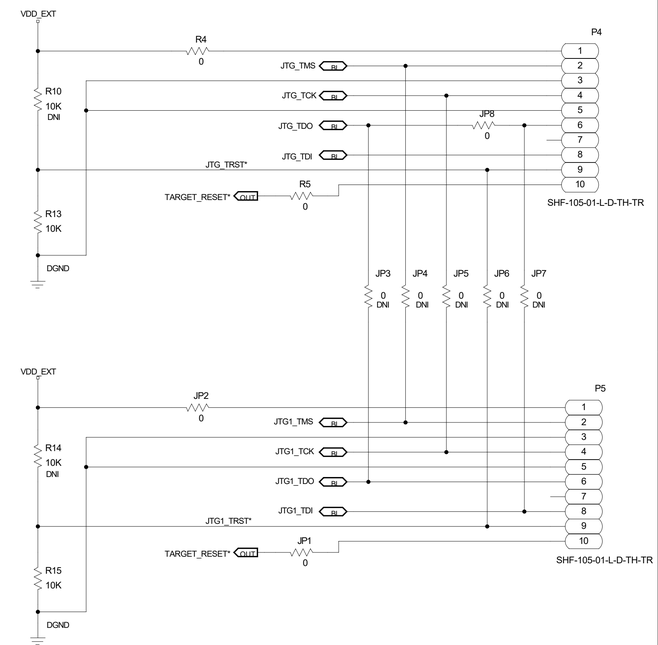
Boot Mode

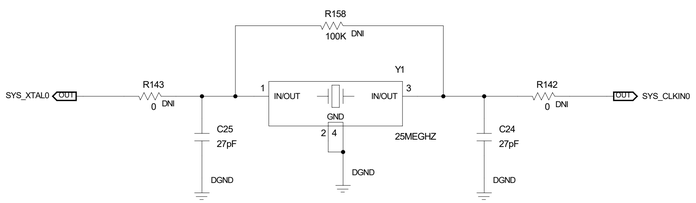
0: No Boot
1: SPI1 Flash Boot
2: SPI2 Host Boot
3: UART0 Boot
4: Extended LinkPort0 Boot
5: xSPI0 Flash Boot
6: eMMC Boot
7: xSPI1 Flash Boot

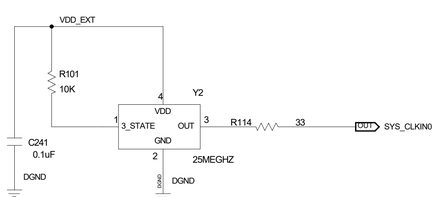




JTAG Daisy Chain Config:
DNI JP8, Install JP3-JP7.







ANALOG DEVICES	SCHEMATIC			
	HW TYPE : Customer Evaluation Z Product(s): ADSP-SC846 : SOM			
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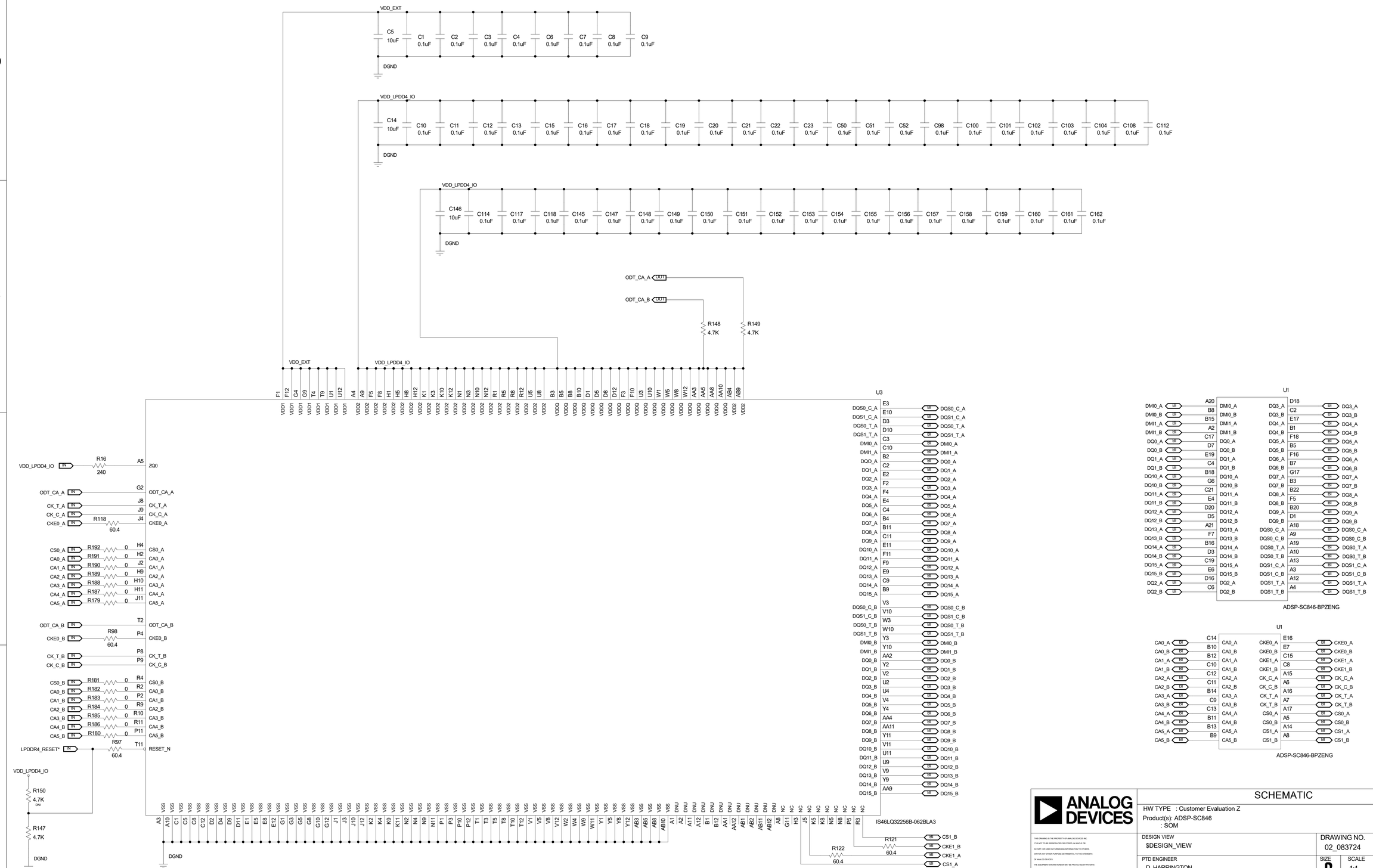
	PTD ENGINEER D. HARRINGTON	SIZE D	SCALE 1:1	SHEET 4 OF 12

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



SCHEMATIC

HW TYPE : Customer Evaluation Z
Product(s): ADSP-SC846
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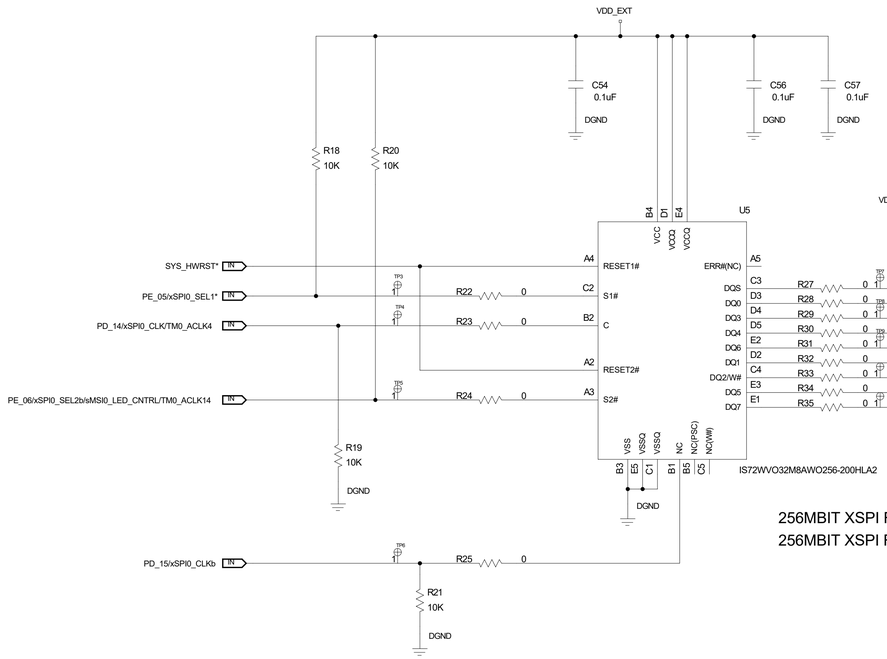
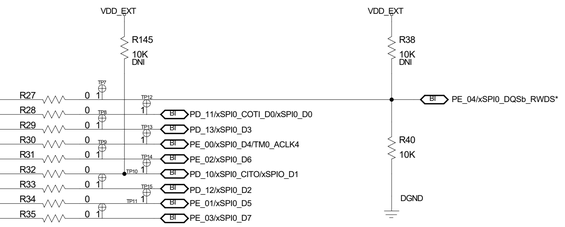
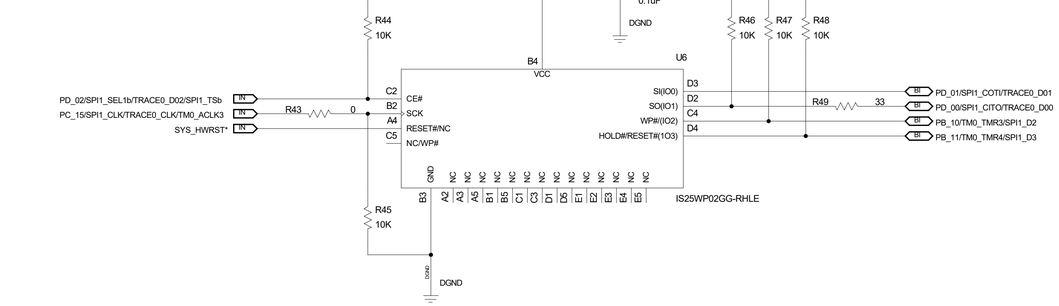
DESIGN VIEW $DESIGN_VIEW	DRAWING NO. 02_083724		REV C
PTD ENGINEER D. HARRINGTON	SIZE D	SCALE 1:1	SHEET 5 OF 12

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED





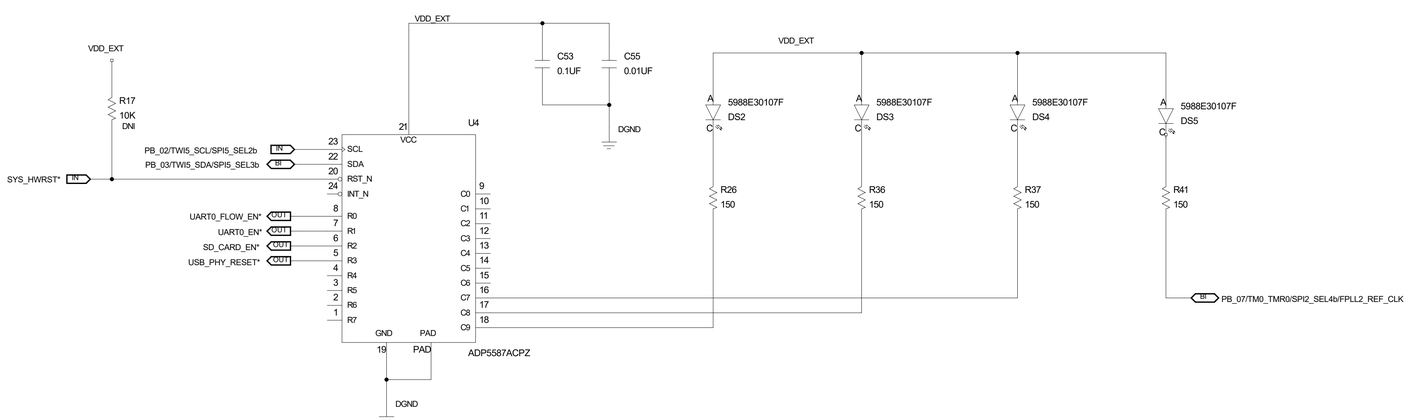


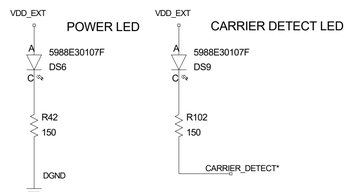
256MBIT XSPI FLASH
256MBIT XSPI RAM

DEFAULT SOFTCONFIG STATES

SIGNAL	STATE
UART0_FLOW_EN*	LOW
UART0_EN*	LOW
USB_QSPI_RESET*	HIGH
USB_QSPI_EN*	HIGH
SD_CARD_EN*	HIGH

TWI ADDRESS 0X34





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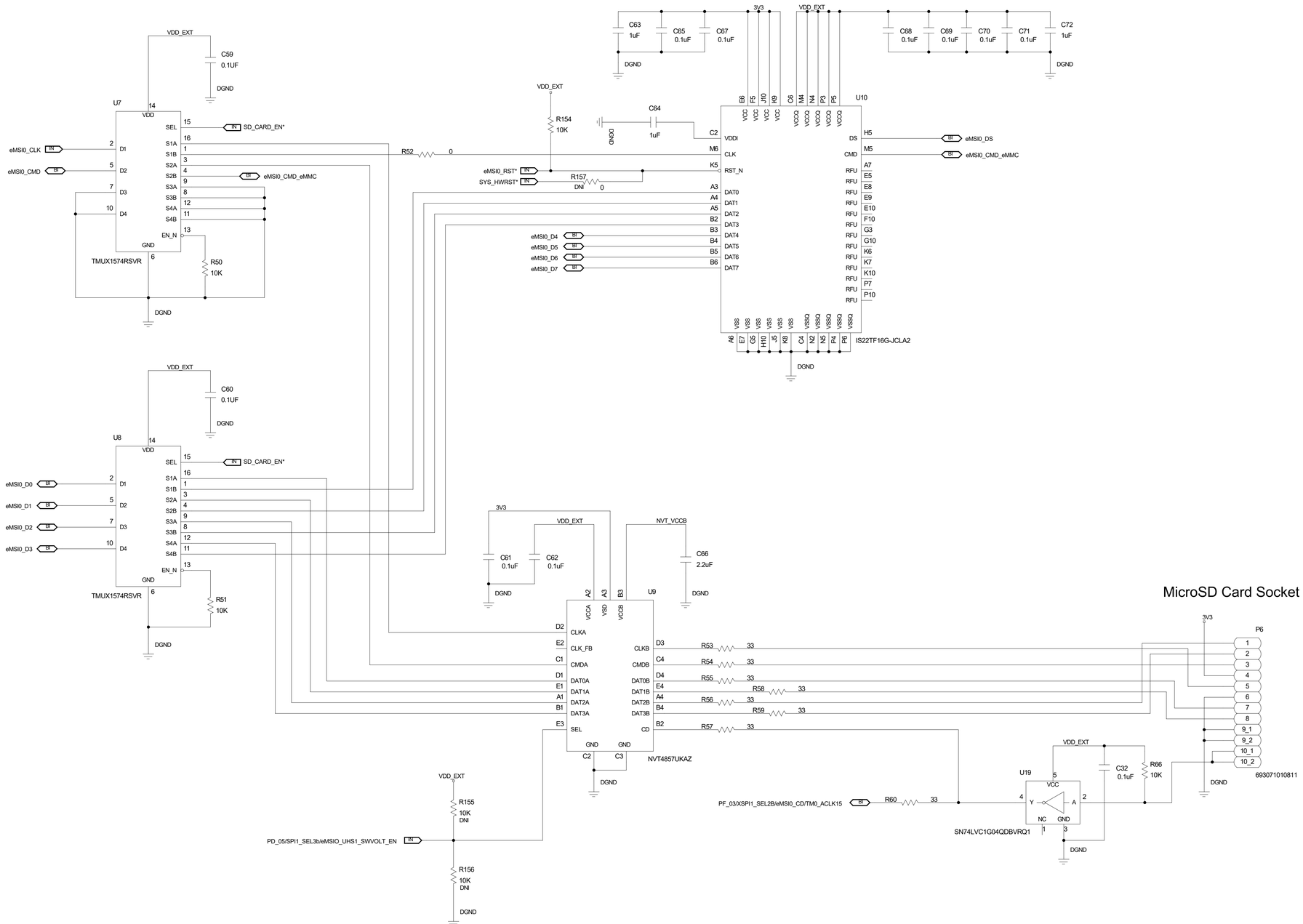
SCHEMATIC

HW TYPE : Customer Evaluation Z
Product(s): ADSP-SC846
: SOM

DESIGN VIEW	DRAWING NO.	REV
$DESIGN_VIEW	02_083724	C

PTD ENGINEER	SIZE	SCALE	SHEET 6 OF 12
D. HARRINGTON	D	1:1	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



SCHEMATIC

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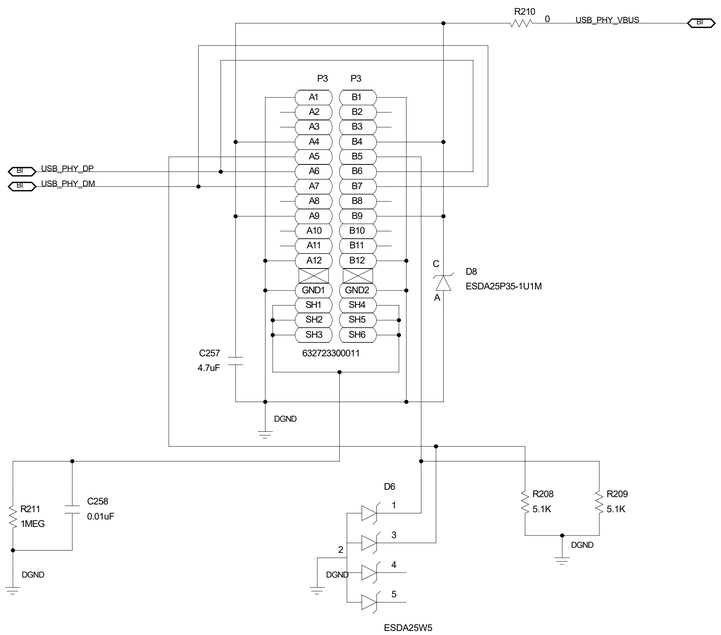
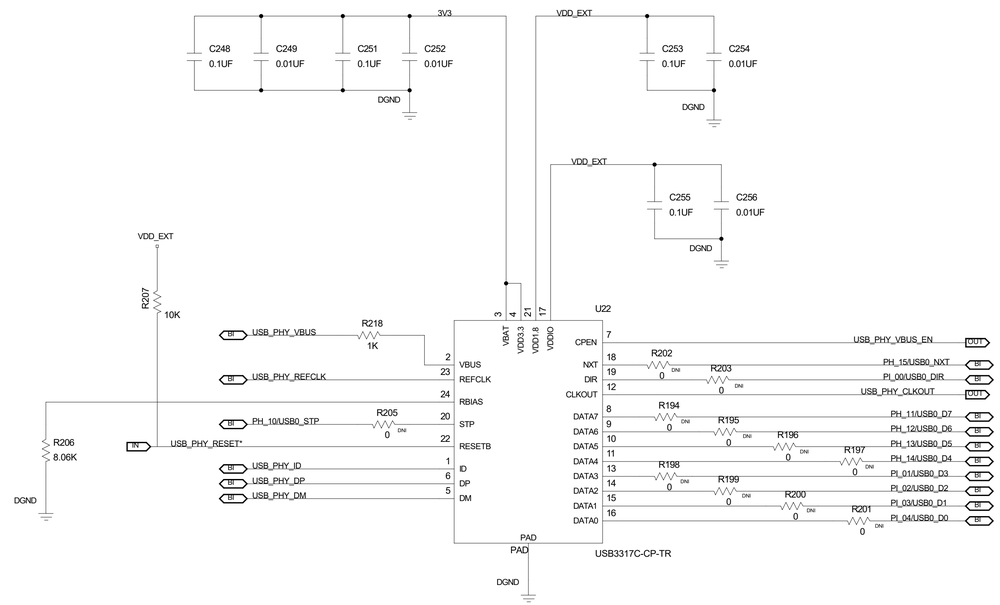
DESIGN VIEW	DRAWING NO.	REV
$DESIGN_VIEW	02_083724	C

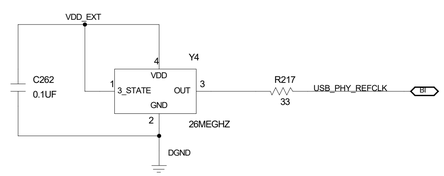
PTD ENGINEER	SIZE	SCALE	SHEET 7 OF 12
D. HARRINGTON	D	1:1	

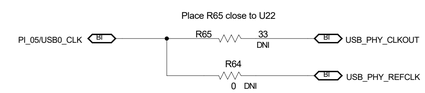
USB3317 PHY

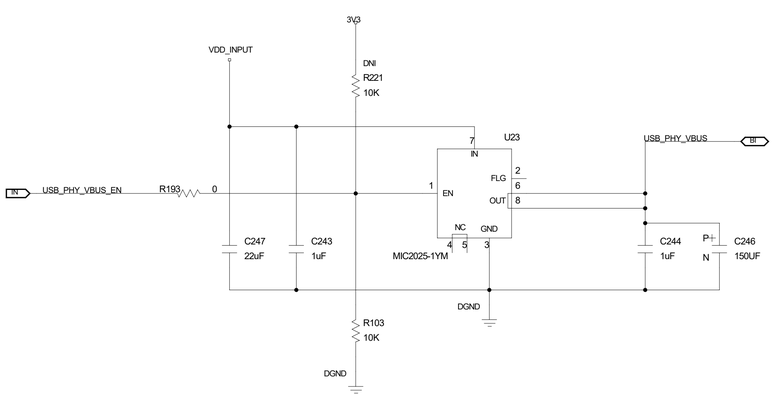
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

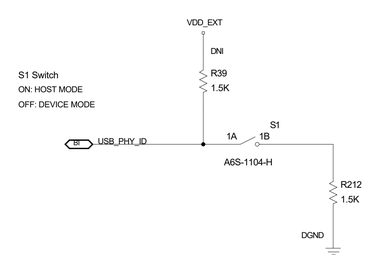












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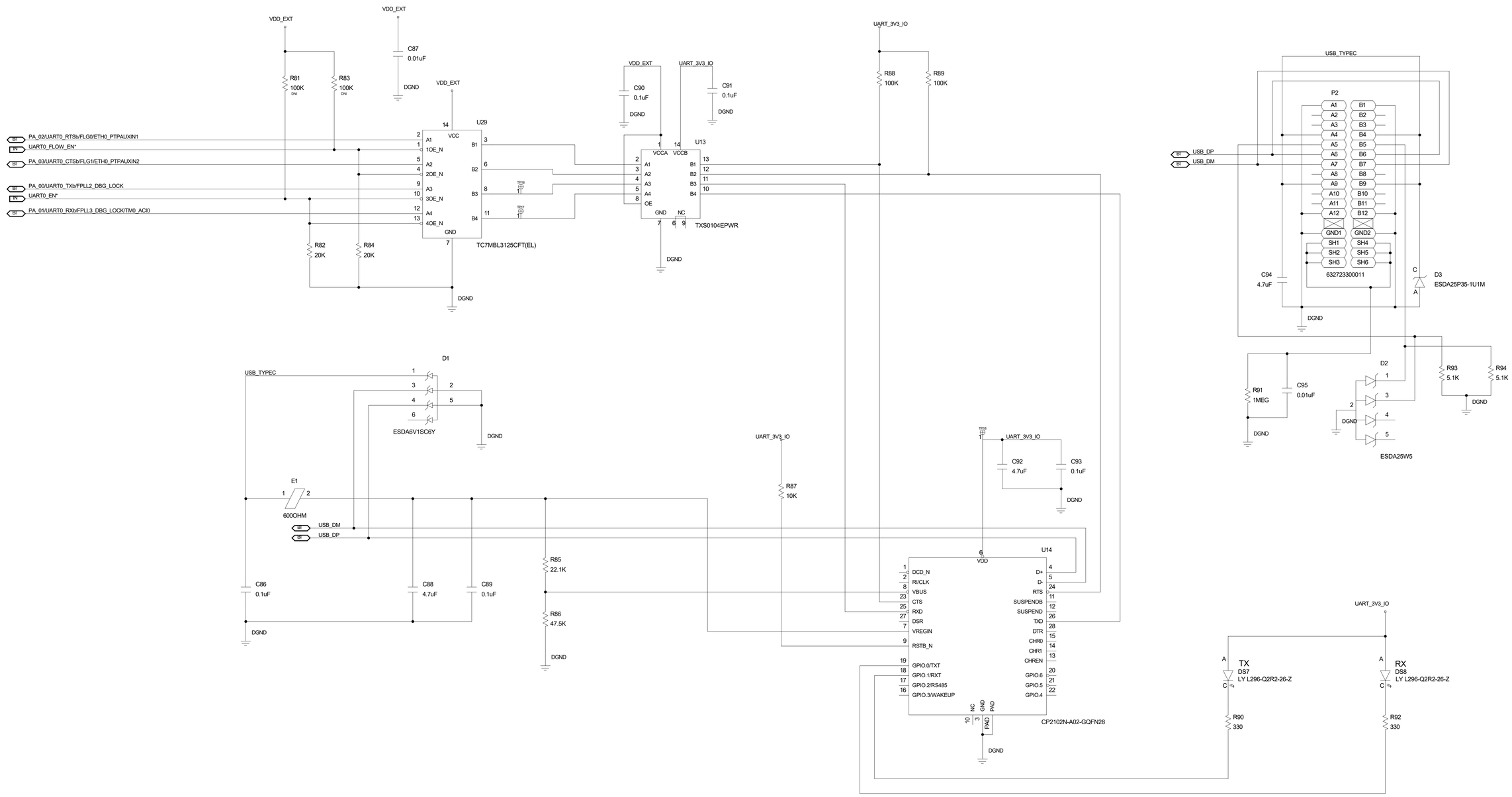
SCHEMATIC

HW TYPE : Customer Evaluation Z
Product(s): ADSP-SC846
: SOM

DESIGN VIEW	DRAWING NO.	REV
$DESIGN_VIEW	02_083724	C

PTD ENGINEER	SIZE	SCALE	SHEET 8 OF 12
D. HARRINGTON	D	1:1	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



ANALOG DEVICES

SCHEMATIC

HW TYPE : Customer Evaluation Z
Product(s): ADSP-SC846
: SOM

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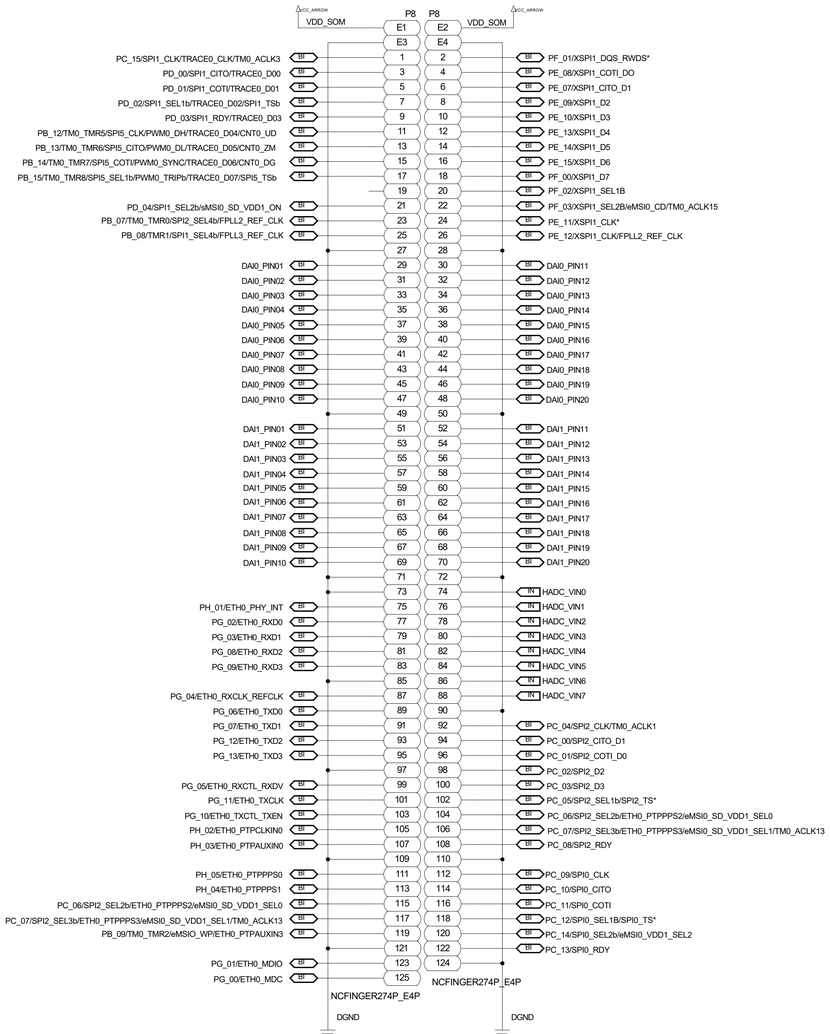
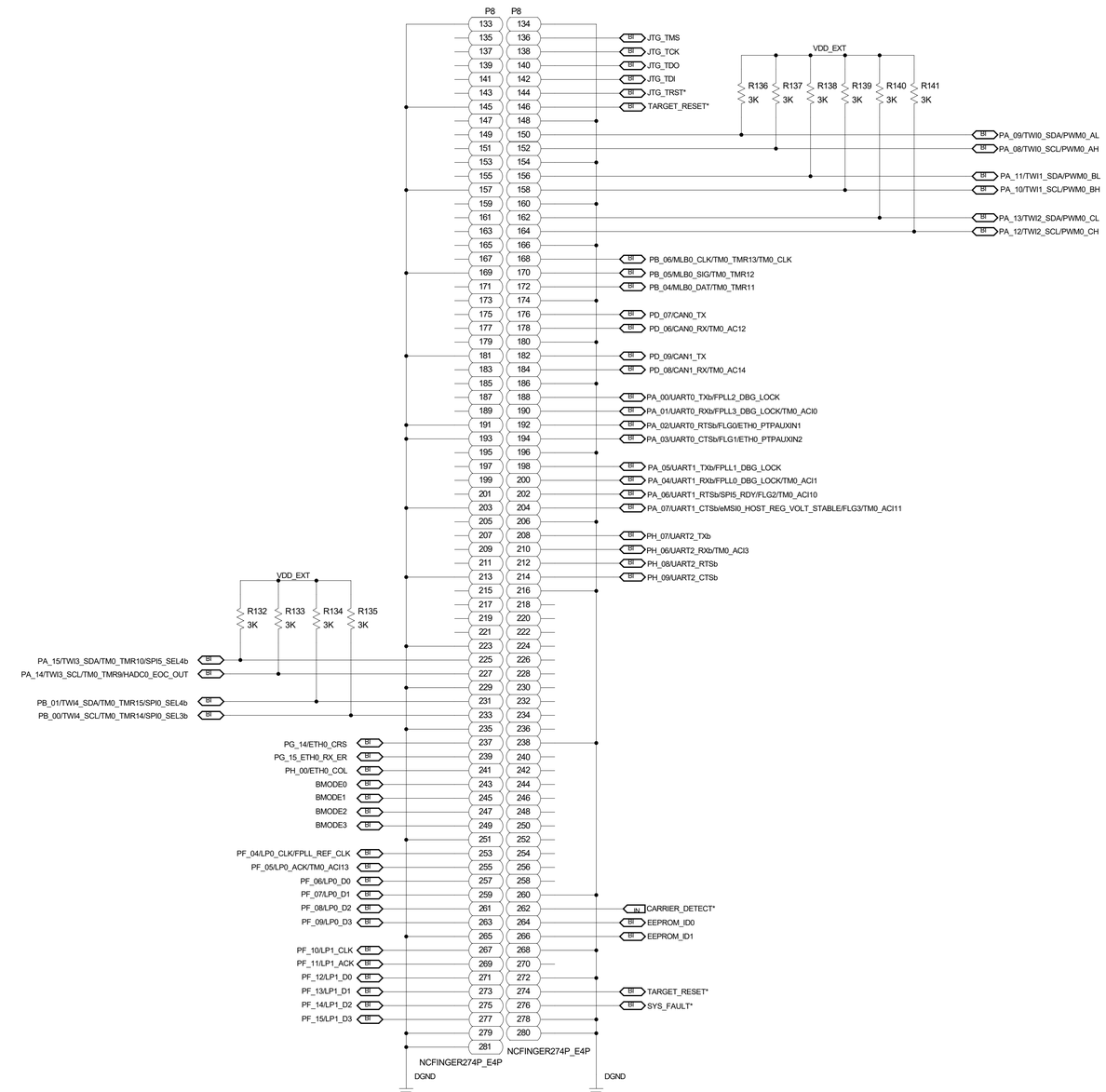
DESIGN VIEW $DESIGN_VIEW	DRAWING NO. 02_083724		REV C
PTD ENGINEER D. HARRINGTON	SIZE D	SCALE 1:1	SHEET 9 OF 12

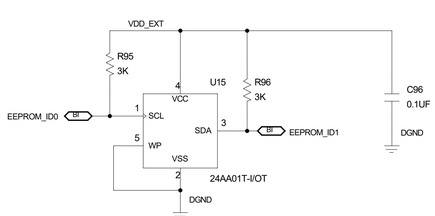
This connector is the mating PCI Express connector. This board will use Edge Fingers to connector to this connector.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

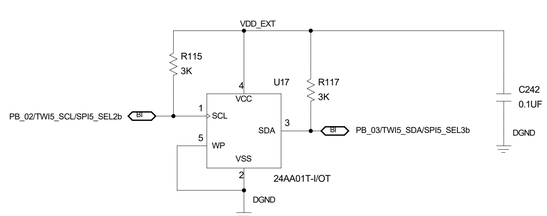




Debug Agent EEPROM



Board Revision EEPROM



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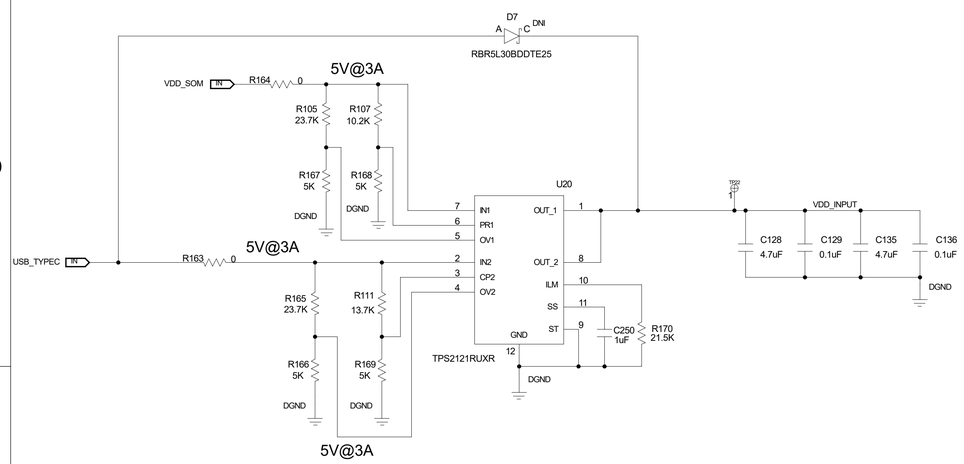
SCHEMATIC

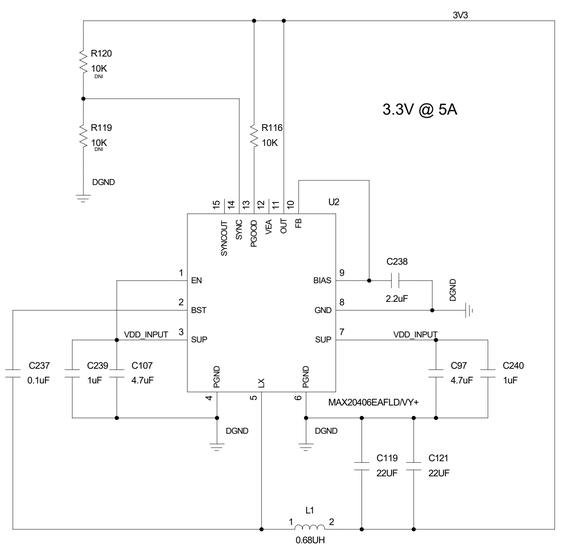
HW TYPE : Customer Evaluation Z
Product(s): ADSP-SC846
: SOM

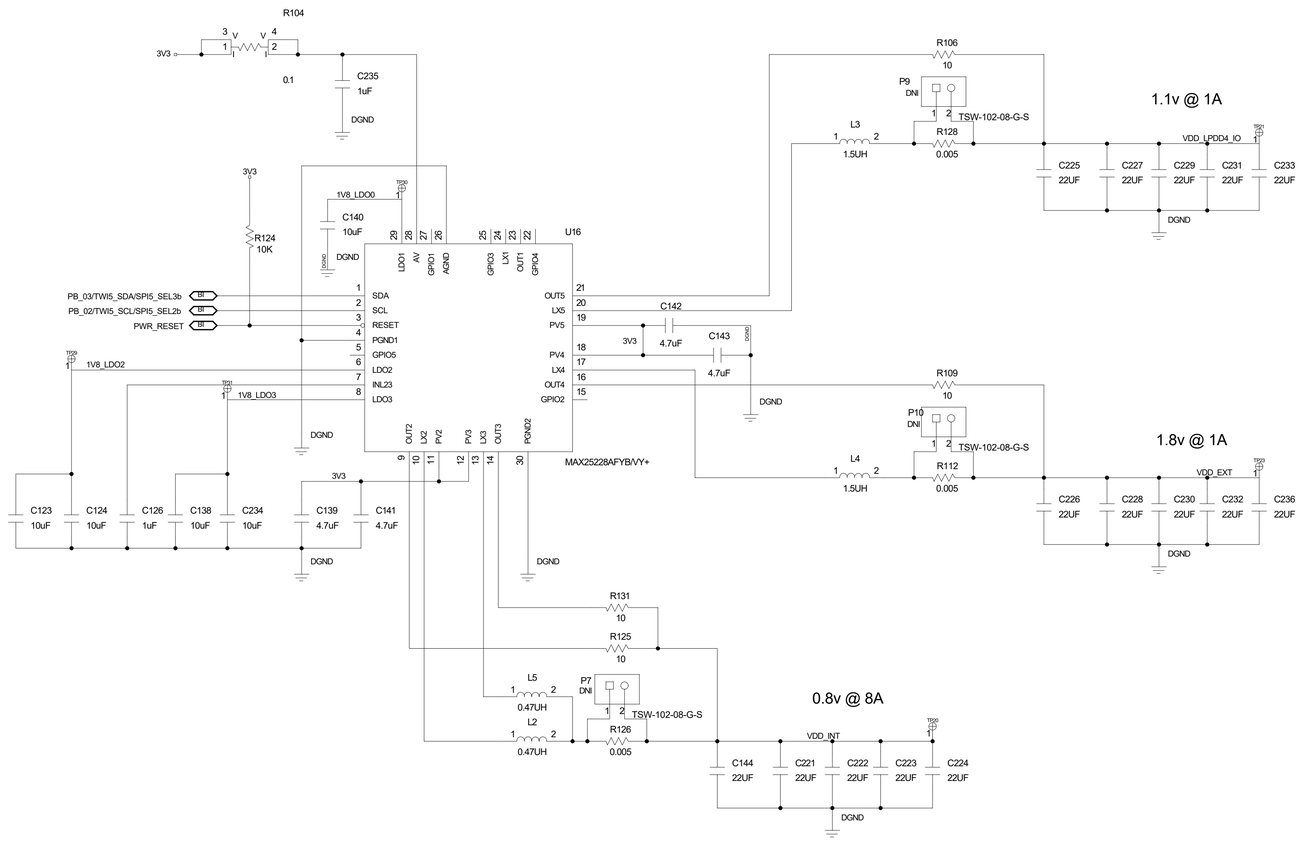
DESIGN VIEW	DRAWING NO.	REV
$DESIGN_VIEW	02_083724	C

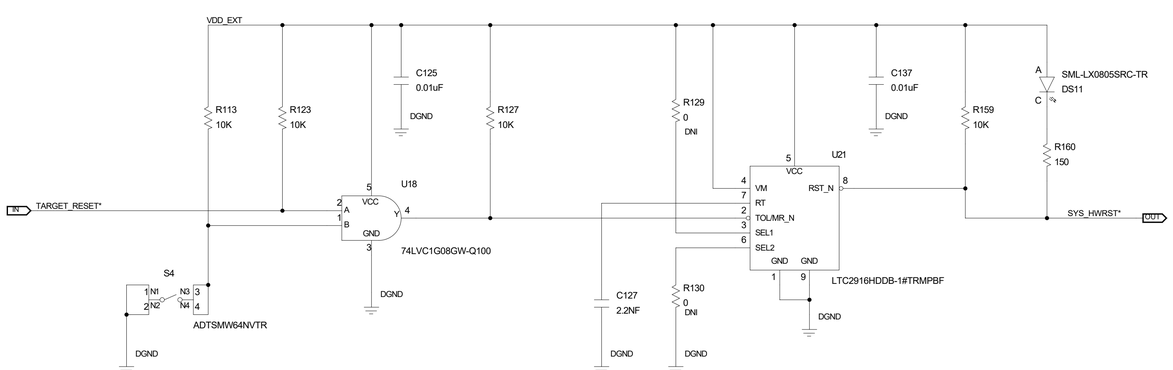
PTD ENGINEER	SIZE	SCALE	SHEET 10 OF 12
D. HARRINGTON	D	1:1	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED









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SCHEMATIC

HW TYPE : Customer Evaluation Z
Product(s): ADSP-SC846
: SOM

DESIGN VIEW	DRAWING NO.	REV
$DESIGN_VIEW	02_083724	C

PTD ENGINEER	SIZE	SCALE	SHEET 11 OF 12
D. HARRINGTON	D	1:1	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

Revision History

Schematic	BOM	Layout	Summary of Changes	Date	Production Status
A	A	A	Initial design	07/15/2024	Prototype
B	B	B	C64 Populated DQ11_B and DQ12_B swapped on U3 Fixed PG_12, PG_13, PG_14 ETHO signal swap on U1	10/24/2025	Prototype
C	C	C	ZQ net between U1 and U3 removed R67 10K pull down added to FAULT signal U1 top layer layout changed to dog bone configuration R68, R16 changed to 0.1%	3/26/2026	Prototype

ANALOG DEVICES

SCHEMATIC

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PTD ENGINEER	SIZE	SCALE	SHEET 12 OF 12
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