PCI Express Connector

Add Pull up connected to same voltage as IO bank

Add Pull up connected to same voltage as IO bank
Cyclone V GX SoC Bank 8

Diagram of Cyclone V GX SoC Bank 8 showing connections and descriptions of various signals and components.
- When using a single x16 flash device a word consists of 16 data bits so addressing starts with FM_A1 mapped to address bit 1 in software.
QSPI Flash & Reset Circuit

QSPI FLASH

RESET CIRCUIT

Input only to CV device cold reset

Input/output to CV device warm reset
DanP Update: SMSC schematic review reference number is 834654-B1081.
SMSC placement review reference number is 375404-B1082.

USB 2.0 OTG , Micro SD Card

USB 2.0 OTG

USB INTERFACE

Micro SD Card

USB 2.0 OTG

Micro SD / USB INTERFACE

PLACE NEAR USB3300

DanP: Should ESD protection diodes to be added?
FPGA Power Monitor

LTC2978
Address Select
PWRMON2 = 7'h5D

Altera Corporation, 101 Innovation Drive, San Jose, CA

Cyclone V SoC FPGA Development Kit Board
Power 2

CAD Note: Regulator input caps
Place near regulator controller.
Power 3 - 2.5V HPS

Cad Note: Place near INTVCC pin

Design Note: Added extra 1uF at INTVCC due to sourcing Vbias pin of LTC3605-1

Design Note: Regulator input caps Place near regulator controller

Design Note: Ith is tied to INTVCC for internal compensation

CAD Note: Overlap R289 & R290 pads at 1 of the pins Place resistor & cap near pin 6

Design Note: 1.2uF, max = 0.6V/2mA

Design Note: Prefil 0.003 size cap 25V rated voltage is sufficient

Cad Note: Place output caps near inductor

Cad Note: Prefer 0603 size cap 25V rated voltage is sufficient
Power 3 - 3.3V HPS

Cad Note: Place near INTVCC pin

Design Note: Added extra 1uF at INTVCC due to sourcing Vbias pin of LTC3605-1

Design Note: Ith is tied to INTVCC for internal compensation

CAD Note: Overlap R289 & R290 pads at 1 of the pins
Place resistor & cap near pin 6

Design Note: 3u = 0.6V/2uA
Ramp rate ~990us

CAD Note: Regulator input caps Place near regulator controller

Design Note: Added extra 1uF at INTVCC due to sourcing Vbias pin of LTC3605-1

Design Note: tss = Cc x 0.6V/2uA
Ramp rate ~990us

CAD Note: Place output caps near inductor

Design Note: Prefer 0603 size cap 25V rated voltage is sufficient

Cad Note: Place near INTVCC pin

Cad Note: 3.3V logic signal

Cad Note: 3.3V_REG_HPS

CAD Note: Place output caps near inductor

Cad Note: 3.3V_REG_HPS

Cad Note: 3.3V_HPS
Power - 1.1V_HPS, 5.0V, 1.8V

Design Note:
Abide only 1uf at INTVCC due to sourcing Vbias pin of LTC3605-1

CAD Note: Regulator input caps Place near regulator controller

Design Note:
Is = Cx x 0.5V/2mA
Ramp rate = 100us

CAD Note: Place output caps near inductor

Design Note:
Prefer 0603 size cap 25V rated voltage is sufficient

CAD Note: Overlap R289 & R290 pads at 1 of the pins Place resistor & cap near pin 6

CAD Note: Added extra 1uF at INTVCC due to sourcing Vbias pin of LTC3025-1

CAD Note:
Vbias is tied to INTVCC for internal compensation

Design Note:
Is = Isat = 6A

Design Note:
Ith is tied to INTVCC for internal compensation

CAD Note:
Regulator input caps Place near regulator controller

Design Note:
0.001 ohm sense resistor minimized IR drop @ 3A

CAD Note:
Place near regulator controller

CAD Note:
Place output caps near inductor

CAD Note:
Place near regulator controller
Power 6 - Power & Temperature Monitor
Power 8 - Cyclone V GX SoC Ground