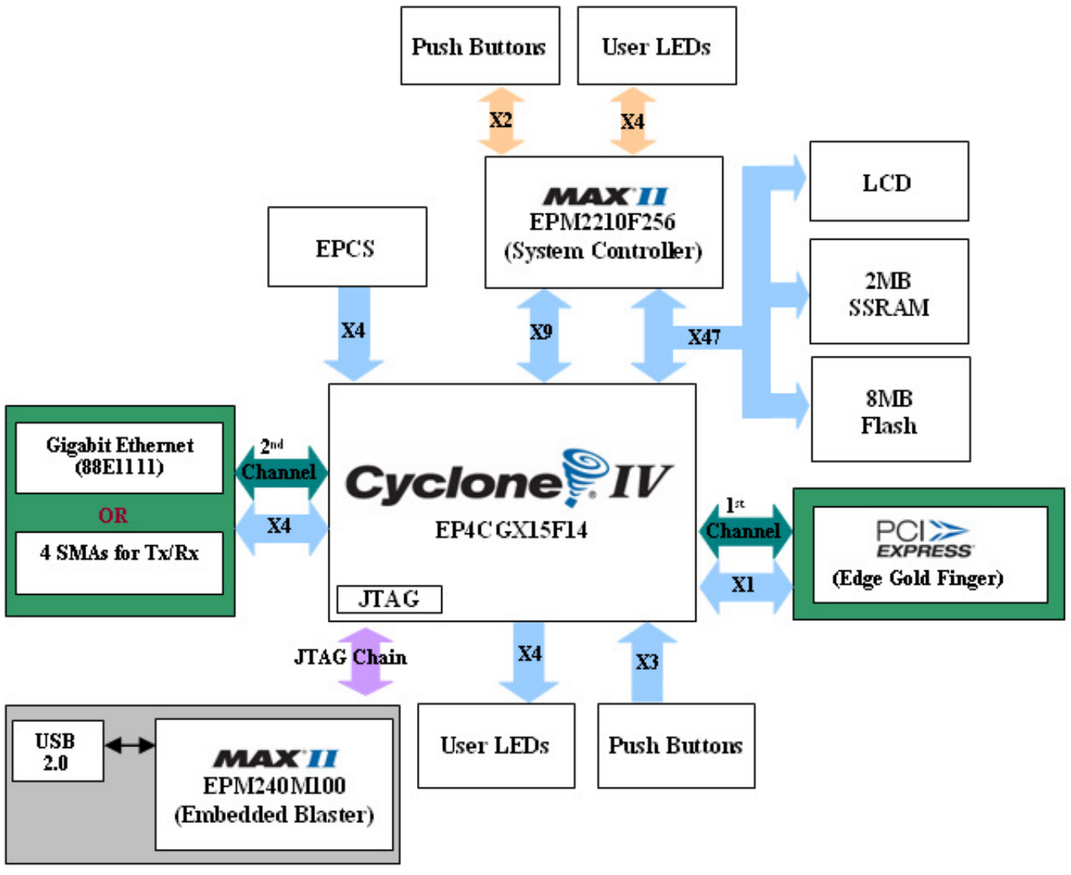
NOTES:

1. Project Drawing Numbers:

Raw PCB	100-0311002-B1
Gerber Files	110-0311002-B1
PCB Design Files	120-0311002-B1
Assembly Drawing	130-0311002-B1
Fab Drawing	140-0311002-B1
Schematic Drawing	150-0311002-B1
PCB Film	160-0311002-B1
Bill of Materials	170-0311002-B1
Schematic Design Files	180-0311002-B1
Functional Specification	210-0311002-B1
PCB Layout Guidelines	220-0311002-B1
Assembly Rework	320-0311002-B1

Cyclone IV GX Transceiver Starter Kit Board



REV	DATE	PAGES	DESCRIPTION
A	11/04/2009	All	Rev A Release

PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Revision History
2	FPGA Package Top
3	Cyclone IV GX Configuration
4	Cyclone IV GX Banks
5	Cyclone IV GX Clock
6	Cyclone IV GX Transceivers I/O and Power
7	10/100/1000 Ethernet
8	PCI Express Edge Connector
9	SRAM & FLASH
10	User IO & Power Monitor
11	EPM2210 System Controller
12	Embedded USB Blaster
13	Power - 2.5V and 1.2V Output
14	Power - 5V, 3.3V and 2.5V Output
15	Cyclone IV GX Decoupling
16	
17	
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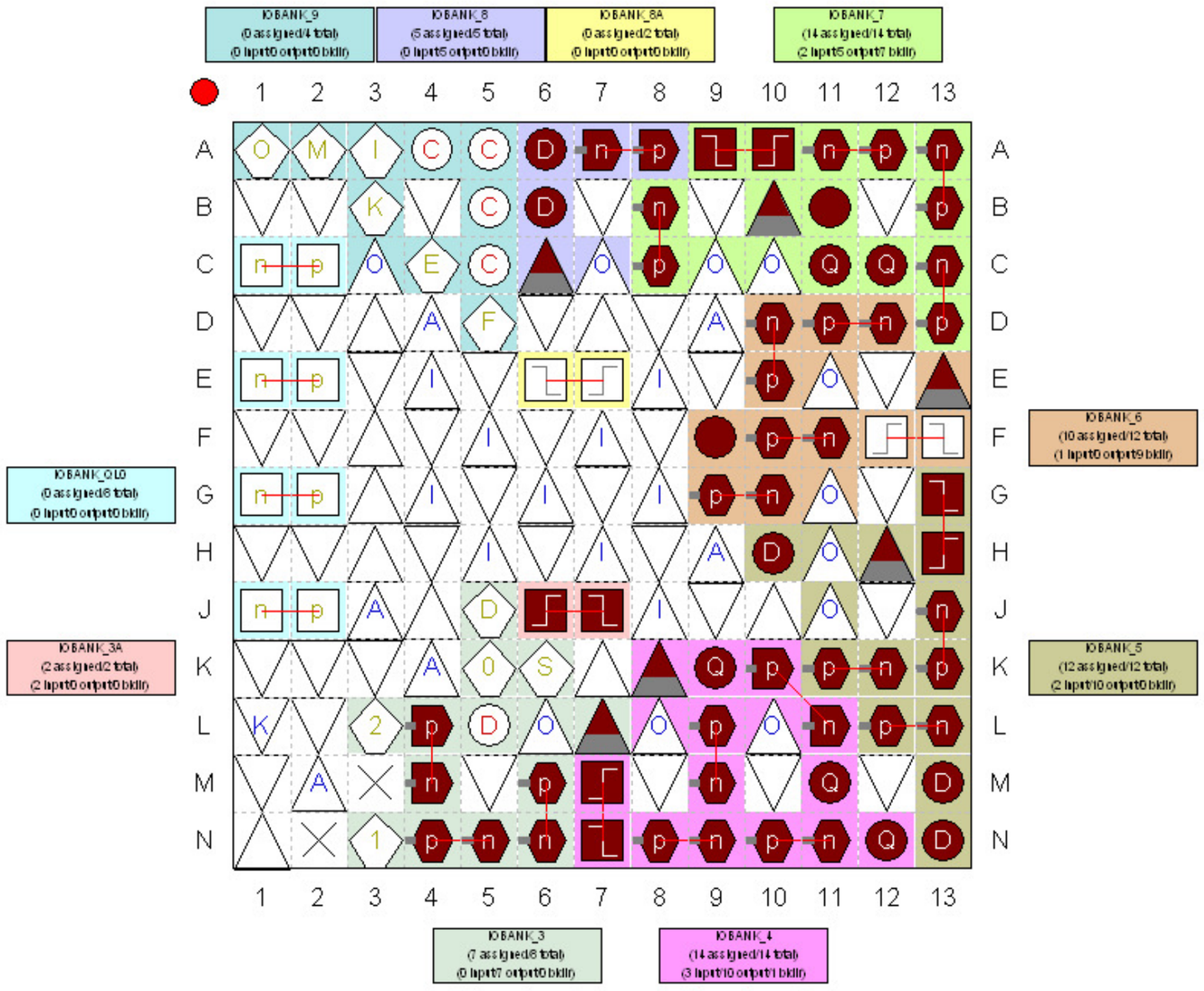
FPGA Package Top View

Top View - Wire Bond

Cyclone IV GX - EP4CGX15BF14C7

Notes:

1. FPGA Schematic Symbol Breakdown:
   - (A) Configuration
   - (B) Clocks
   - (C) Banks
   - (D) Transceivers
   - (E) Power
   - (F) GND



Pin Legend

Symbol	Pin Type
	User I/O
	User Assigned I/O
	Fitter Assigned I/O
	Unbonded Pad
	Reserved Pin
I	DIFF_n
P	DIFF_p
I	DIFF_n Output
P	DIFF_p Output
Q	DQ
S	DQS
S	DQSB
Q	CQ#
L	Other PLL
	CLK_n
	CLK_p
	PORSEL
I	GX_X*n
P	GX_X*p
T	TEMPDIODE
0	MSEL0
1	MSEL1
2	MSEL2
D	CONF_DONE
D	DCLK
C	nCEO
E	nCE
F	nCONFIG
I	TDI
K	TCK
M	TMS
O	TDO
R	TRST
S	nSTATUS
U	nIO_PLLUP
P	Other Dedicated Programming
	VREF
	VCCP/VCCR/VCCT
A	VCCA
0	VCCIO
	GND
R	RREF
	No Connect

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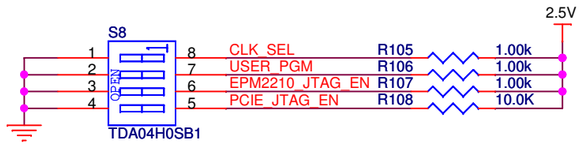
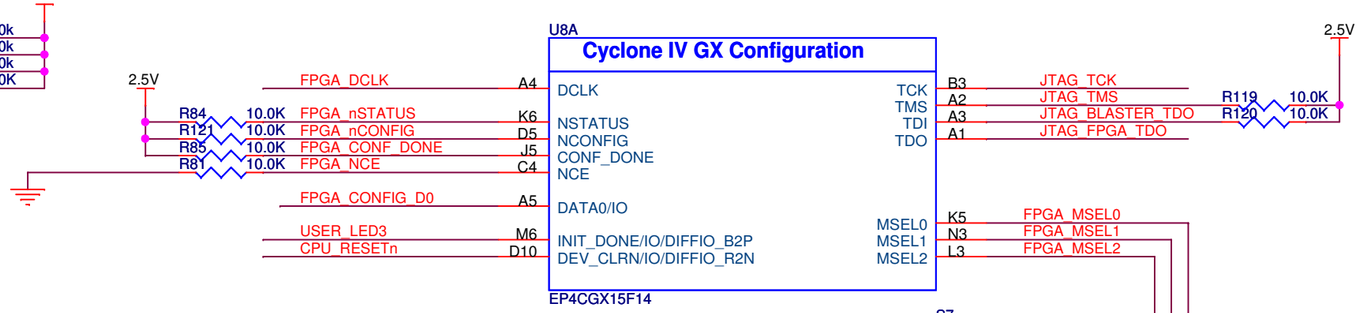
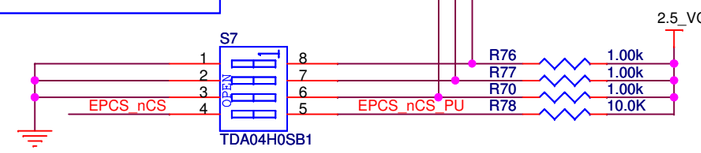
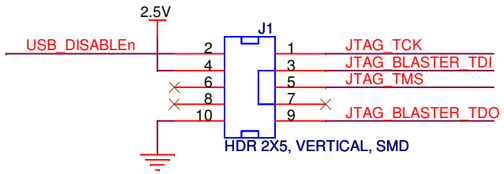
Cyclone IV GX Configuration

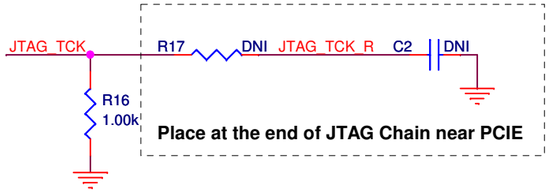


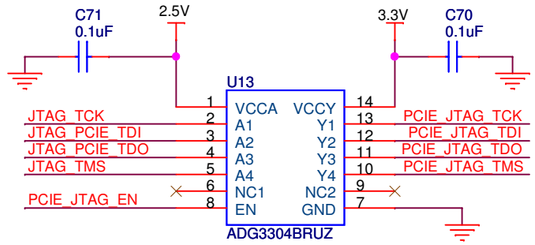


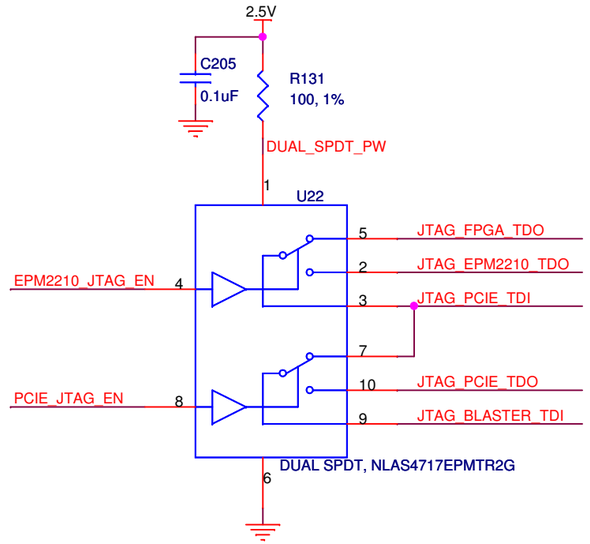


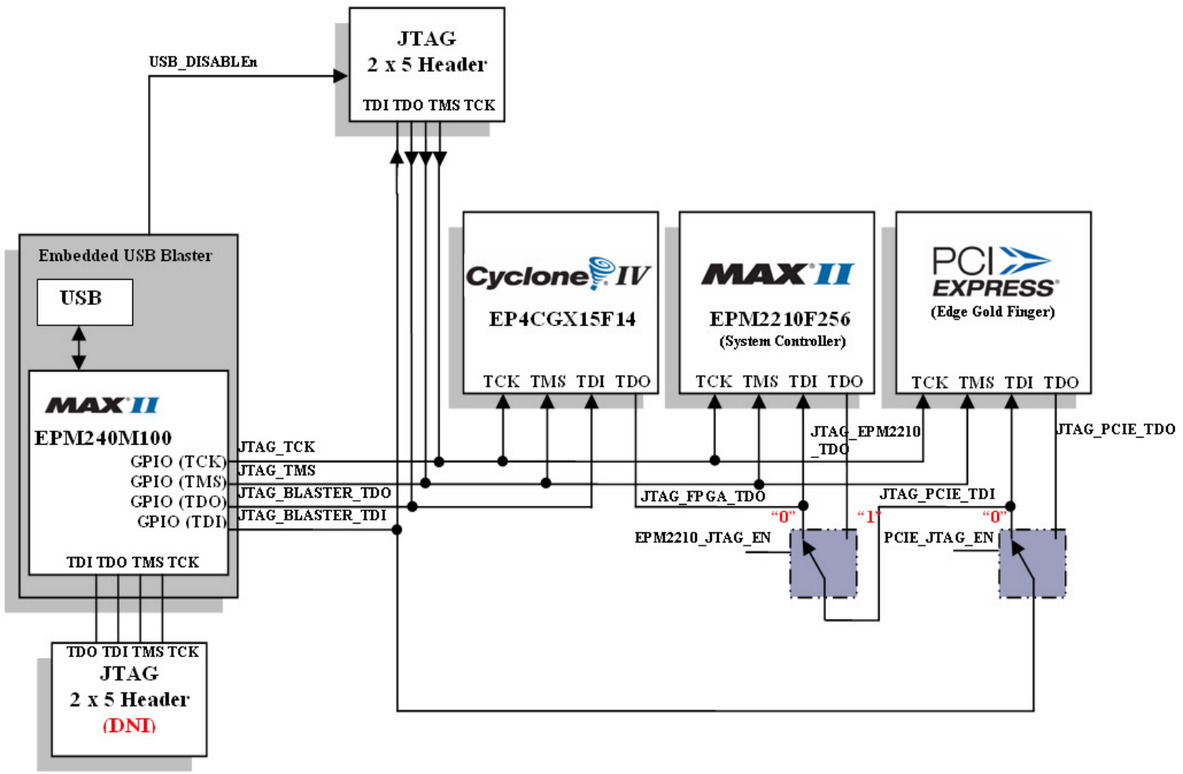
USB Blaster Programming Header
(uses JTAG mode only)

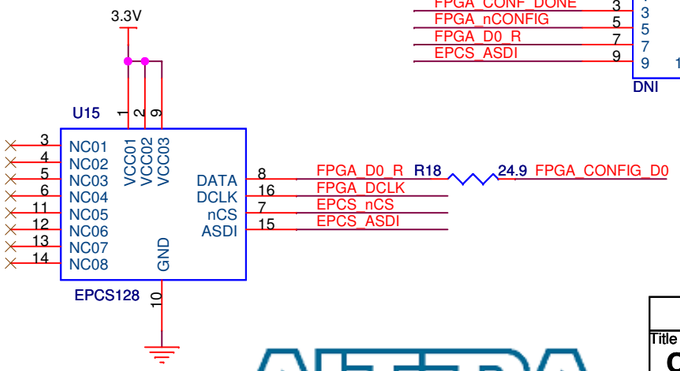


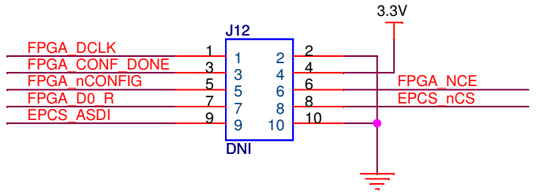












Configuration Signals

FPGA_DCLK FPGA_DCLK 11
FPGA_nSTATUS FPGA_nSTATUS 11
FPGA_nCONFIG FPGA_nCONFIG 11
FPGA_CONF_DONE FPGA_CONF_DONE 11
FPGA_CONFIG_D0 FPGA_CONFIG_D0 11

User IO

USER_LED[3..0] USER_LED[3..0] 4,10
CPU_RESETn CPU_RESETn 10
CLK_SEL CLK_SEL 5,11
USER_PGM USER_PGM 11

JTAG Signals

JTAG_TCK JTAG_TCK 11,12
JTAG_TMS JTAG_TMS 11,12
JTAG_BLASTER_TDO JTAG_BLASTER_TDO 12
JTAG_FPGA_TDO JTAG_FPGA_TDO 11
JTAG_EPM2210_TDO JTAG_EPM2210_TDO 11
JTAG_BLASTER_TDI JTAG_BLASTER_TDI 12
USB_DISABLEn USB_DISABLEn 12

PCIe JTAG Signals

PCIE_JTAG_TCK PCIE_JTAG_TCK 8
PCIE_JTAG_TMS PCIE_JTAG_TMS 8
PCIE_JTAG_TDO PCIE_JTAG_TDO 8
PCIE_JTAG_TDI PCIE_JTAG_TDI 8

EPCS INTERFACES

EPCS_nCS EPCS_nCS 4,11
EPCS_ASDI EPCS_ASDI 4

CONFIGURATION

FPGA_MSEL[2..0] FPGA_MSEL[2..0] 11

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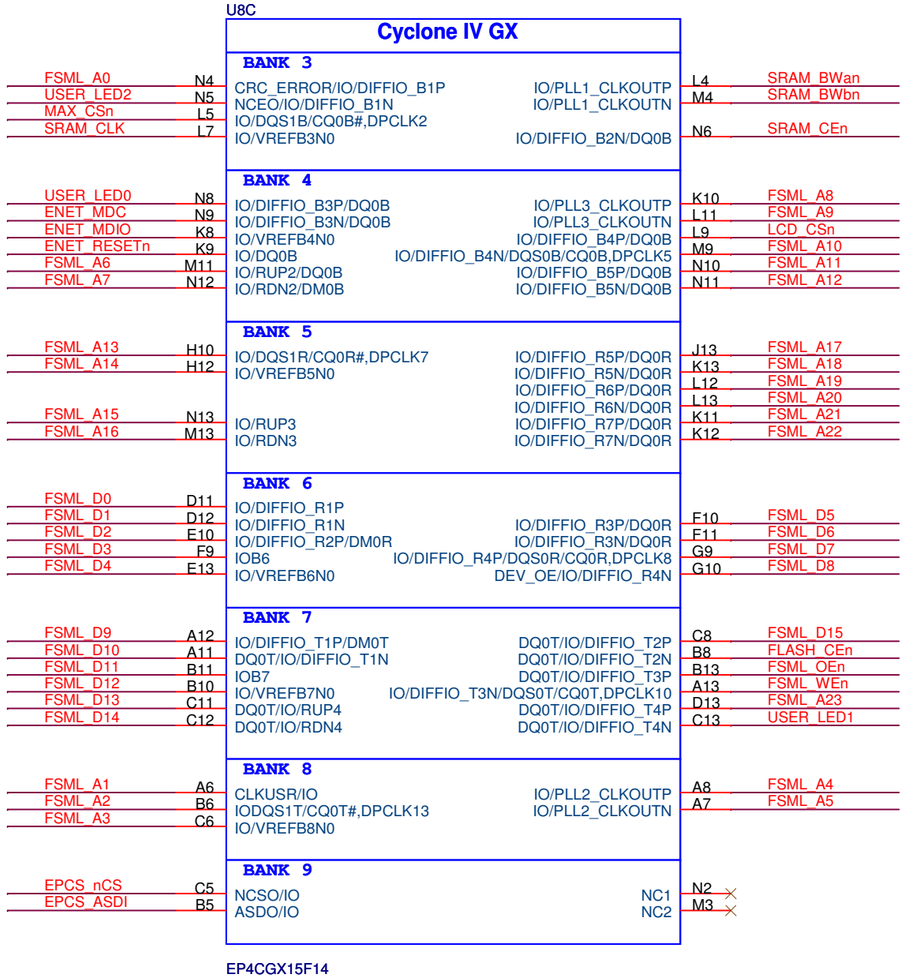
Cyclone IV GX Banks



FLASH & SRAM & LCD INTERFACE

FSML_D[15:0] — FSML_D[15:0] 9,10,11
FSML_A[23:0] — FSML_A[23:0] 9,10,11
FSML_OEn — FSML_OEn 9,11
FSML_WEn — FSML_WEn 9,11
SRAM_BWan — SRAM_BWan 9,11
SRAM_BWbn — SRAM_BWbn 9,11
SRAM_CEn — SRAM_CEn 9,11
SRAM_CLK — SRAM_CLK 9,11
FLASH_CEn — FLASH_CEn 9,11
LCD_CSn — LCD_CSn 10

LED INTERFACES

USER_LED[3..0] — USER_LED[3..0] 3,10

EPCS INTERFACES

EPCS_nCS — EPCS_nCS 3,11
EPCS_ASDI — EPCS_ASDI 3

ETHERNET INTERFACE

ENET_RESETn — ENET_RESETn 7
ENET_MDIO — ENET_MDIO 7
ENET_MDC — ENET_MDC 7

MAX II INTERFACE

MAX_CSn — MAX_CSn 11

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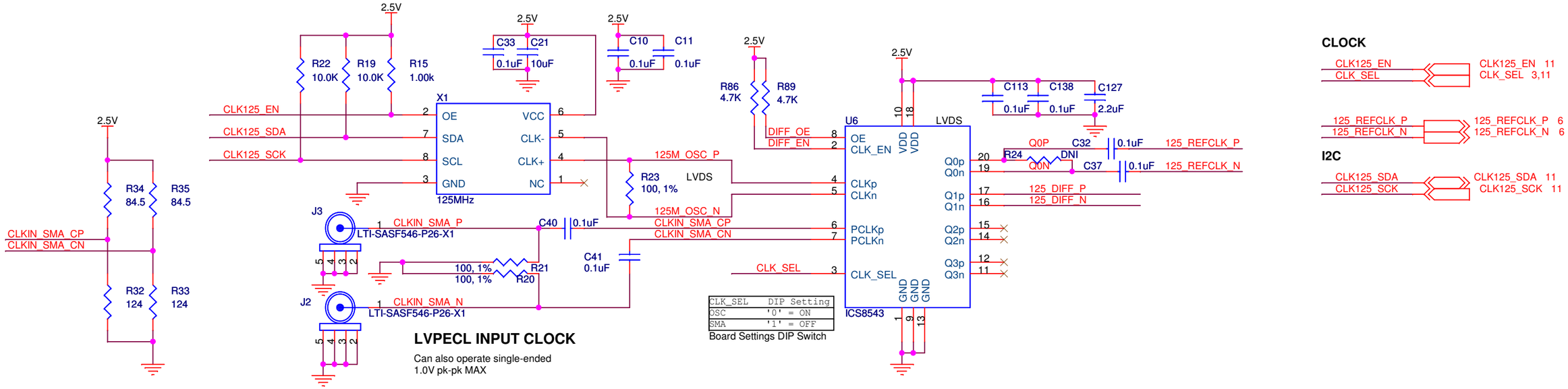
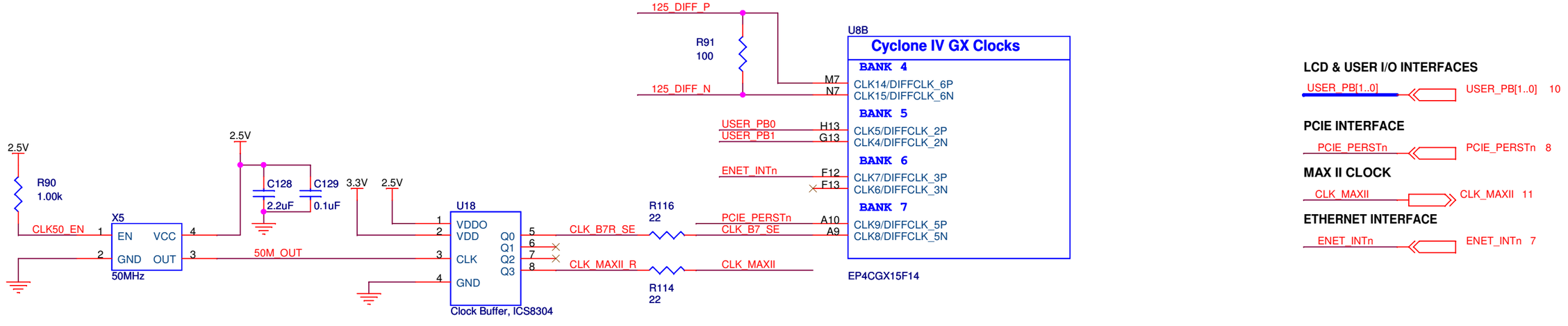
Cyclone IV GX Banks & Clock





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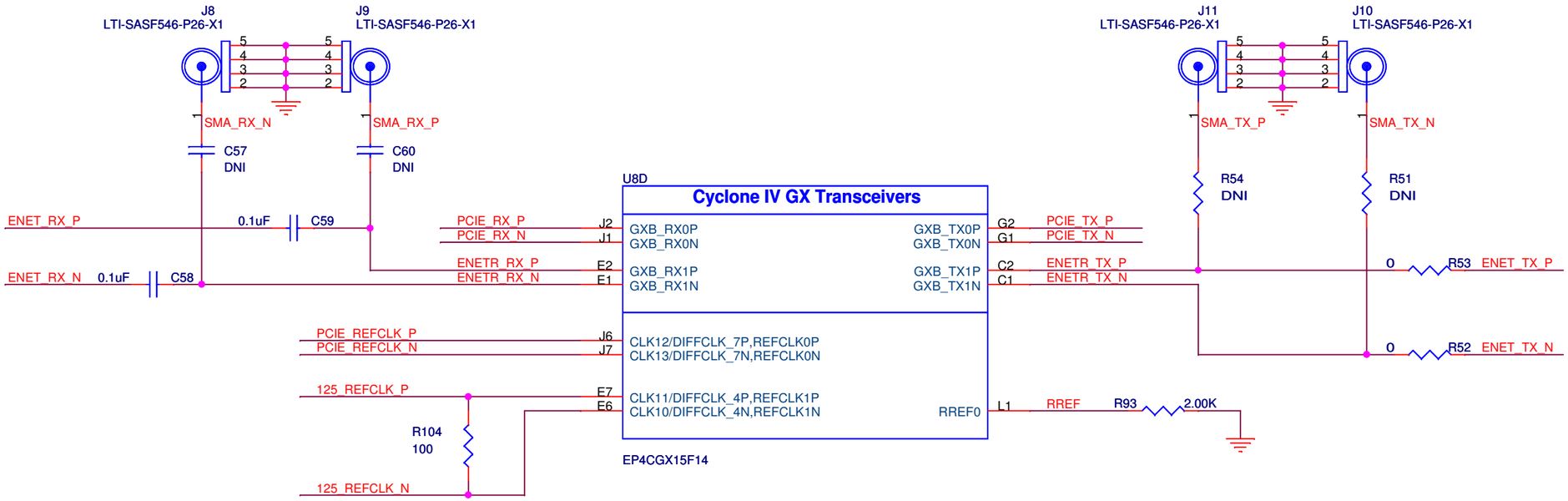
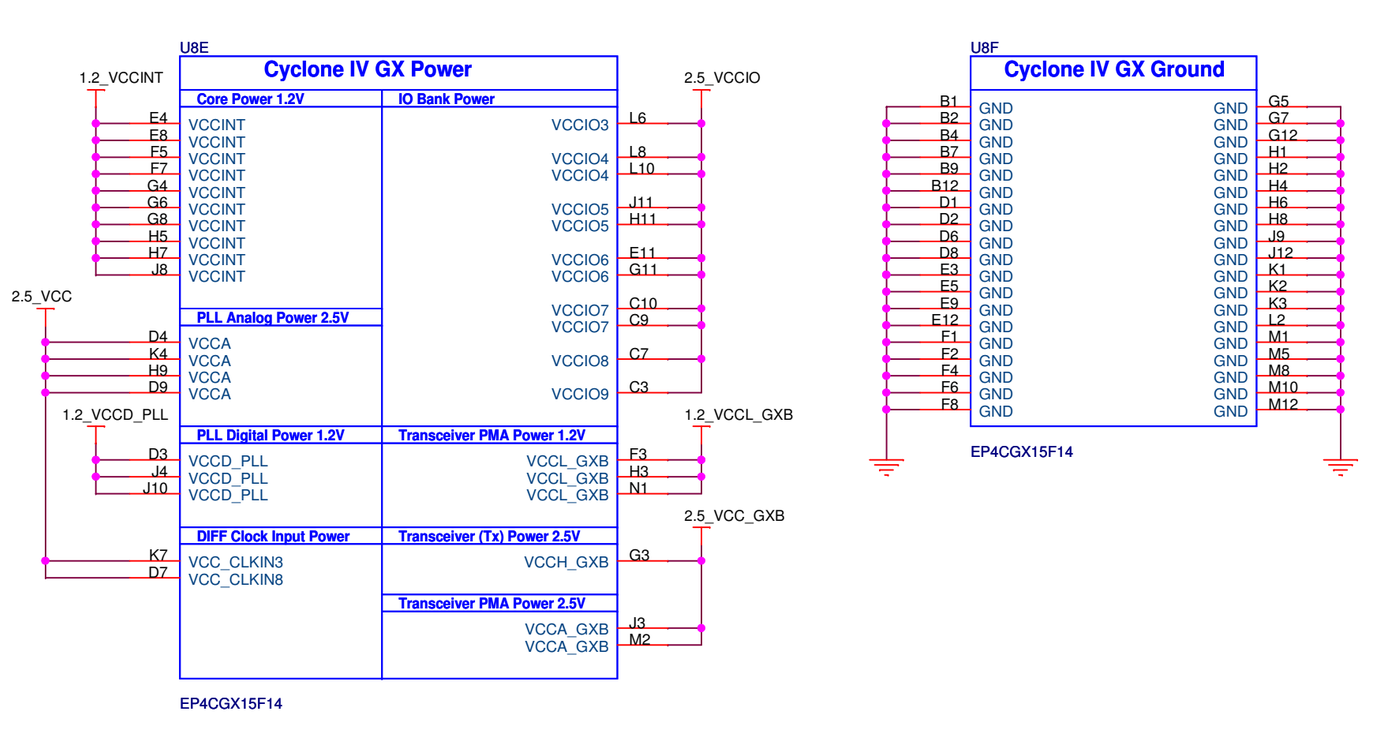
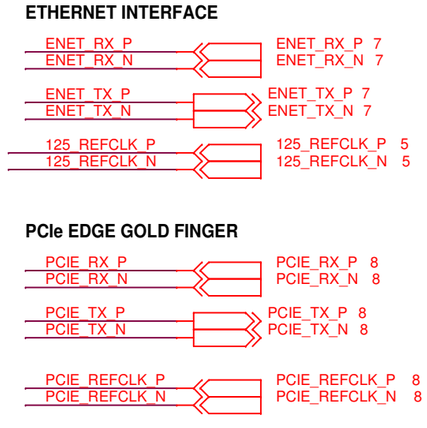
Cyclone IV GX Transceivers I/O and Power







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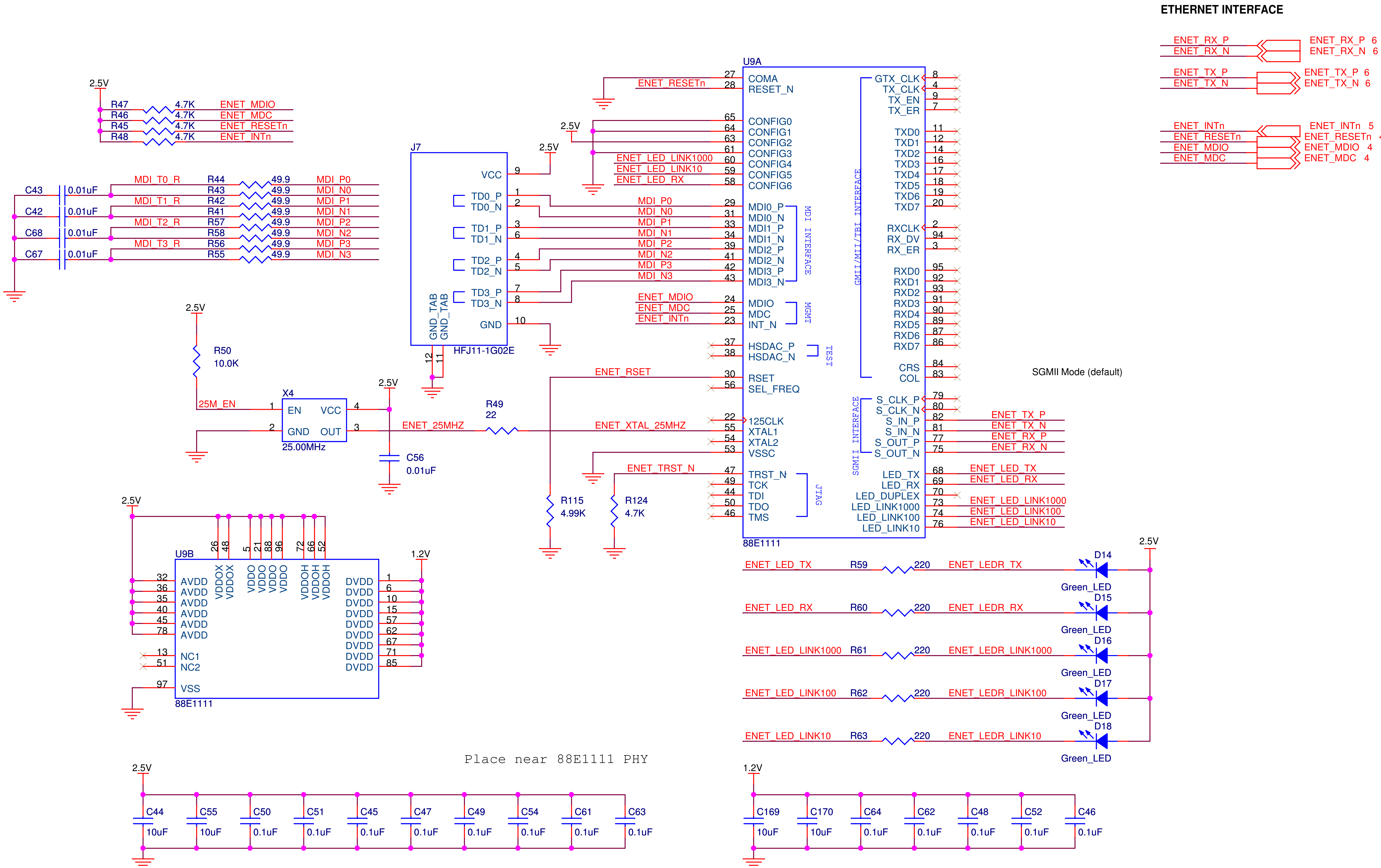
10/100/1000 Ethernet



ETHERNET INTERFACE
ENET_RX_P 6
ENET_RX_N 6
ENET_TX_P 6
ENET_TX_N 6
ENET_INTn 5
ENET_RESETn 4
ENET_MDIO 4
ENET_MDC 4
SGMII Mode (default)
2.5V
R47 4.7K ENET_MDIO
R46 4.7K ENET_MDC
R45 4.7K ENET_RESETn
R48 4.7K ENET_INTn
C43 0.01uF MDI_T0_R R44 49.9 MDI_P0
R43 49.9 MDI_N0
C42 0.01uF MDI_T1_R R42 49.9 MDI_P1
R41 49.9 MDI_N1
C68 0.01uF MDI_T2_R R57 49.9 MDI_P2
R58 49.9 MDI_N2
C67 0.01uF MDI_T3_R R56 49.9 MDI_P3
R55 49.9 MDI_N3
J7
VCC
TD0_P
TD0_N
TD1_P
TD1_N
TD2_P
TD2_N
TD3_P
TD3_N
GND
GND_TAB
GND_TAB
HFJ11-1G02E
U9A
COMA
RESET_N
CONFIG0
CONFIG1
CONFIG2
CONFIG3
CONFIG4
CONFIG5
CONFIG6
ENET_LED_LINK1000
ENET_LED_LINK10
ENET_LED_RX
MDI0_P
MDI0_N
MDI1_P
MDI1_N
MDI2_P
MDI2_N
MDI3_P
MDI3_N
MDI INTERFACE
MDIO
MDC
INT_N
MGMT
HSDAC_P
HSDAC_N
TEST
RSET
SEL_FREQ
ENET_RSET
125CLK
XTAL1
XTAL2
VSSC
ENET_XTAL_25MHZ
TRST_N
TCK
TDI
TDO
TMS
ENET_TRST_N
JTAG
GTX_CLK
TX_CLK
TX_EN
TX_ER
TXD0
TXD1
TXD2
TXD3
TXD4
TXD5
TXD6
TXD7
RXCLK
RX_DV
RX_ER
RXD0
RXD1
RXD2
RXD3
RXD4
RXD5
RXD6
RXD7
CRS
COL
GMII/MII/TBI INTERFACE
S_CLK_P
S_CLK_N
S_IN_P
S_IN_N
S_OUT_P
S_OUT_N
SGMII INTERFACE
LED_TX
LED_RX
LED_DUPLEX
LED_LINK1000
LED_LINK100
LED_LINK10
ENET_LED_TX
ENET_LED_RX
ENET_LED_LINK1000
ENET_LED_LINK100
ENET_LED_LINK10
88E1111
R50 10.0K
25M_EN
X4
EN VCC
GND OUT
25.00MHz
C56 0.01uF
ENET_25MHZ
R49 22
R115 4.99K
R124 4.7K
U9B
AVDD
VDDOX
VDDO
VDDOH
DVDD
NC1
NC2
VSS
88E1111
1.2V
ENET_LED_TX R59 220 ENET_LEDR_TX D14 Green_LED
ENET_LED_RX R60 220 ENET_LEDR_RX D15 Green_LED
ENET_LED_LINK1000 R61 220 ENET_LEDR_LINK1000 D16 Green_LED
ENET_LED_LINK100 R62 220 ENET_LEDR_LINK100 D17 Green_LED
ENET_LED_LINK10 R63 220 ENET_LEDR_LINK10 D18 Green_LED
Place near 88E1111 PHY
C44 10uF
C55 10uF
C50 0.1uF
C51 0.1uF
C45 0.1uF
C47 0.1uF
C49 0.1uF
C54 0.1uF
C61 0.1uF
C63 0.1uF
C169 10uF
C170 10uF
C64 0.1uF
C62 0.1uF
C48 0.1uF
C52 0.1uF
C46 0.1uF

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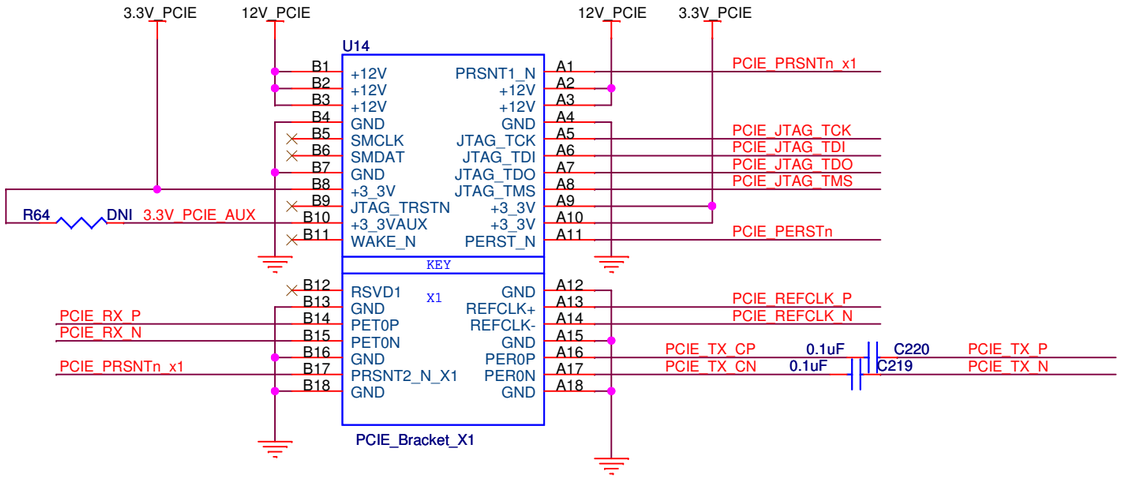
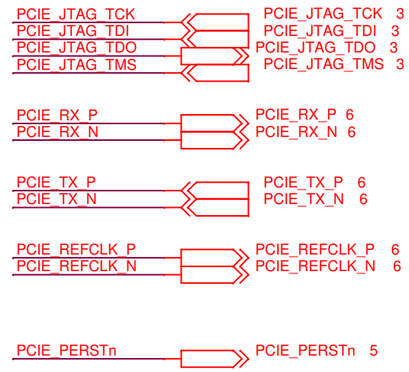
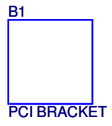
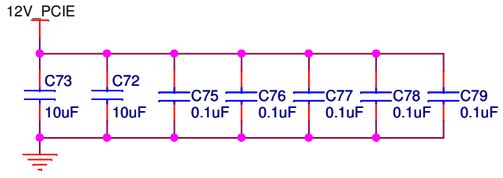
PCI Express Edge Connector

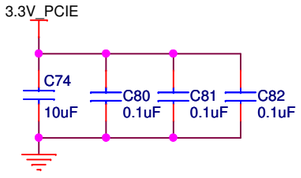


PCIe EDGE GOLD FINGER









Title
Cyclone IV GX FPGA Development Kit Board

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SRAM & FLASH

FSM BUS

FSML_D[15:0]

FSML_A[23:0]

FLASH & SRAM INTERFACE

FSML_D[15:0]	FSML_D[15:0] 4,10,11
FSML_A[23:0]	FSML_A[23:0] 4,10,11
SRAM_BWan	SRAM_BWan 4,11
SRAM_BWbn	SRAM_BWbn 4,11
FSML_WEn	FSML_WEn 4,11
FSML_OEn	FSML_OEn 4,11
SRAM_CEn	SRAM_CEn 4,11
SRAM_ADSCn	SRAM_ADSCn 11
SRAM_ADSPn	SRAM_ADSPn 11
SRAM_ADVn	SRAM_ADVn 11
SRAM_CLK	SRAM_CLK 4,11
FLASH_CEn	FLASH_CEn 4,11

U12 — IS61VPS102418A-250TQL SSRAM

2.5V → VDD: 15, 41, 65, 91

2.5V → VDDQ: 4, 11, 20, 27, 54, 61, 70, 77

FSML_A1	37	A0	
FSML_A2	36	A1	
FSML_A3	32	A2	
FSML_A4	33	A3	
FSML_A5	34	A4	
FSML_A6	35	A5	
FSML_A7	42	A6	
FSML_A8	43	A7	
FSML_A9	44	A8	
FSML_A10	45	A9	
FSML_A11	46	A10	
FSML_A12	47	A11	
FSML_A13	48	A12	
FSML_A14	49	A13	
FSML_A15	50	A14	
FSML_A16	80	A15	
FSML_A17	81	A16	
FSML_A18	82	A17	
FSML_A19	99	A18	
FSML_A20	100	A19	
SRAM_CLK	89	CLK	
FSML_OEn	86	OE_n	
SRAM_CEn	98	CE1_n	
SRAM_CE2	97	CE2	
SRAM_CE3n	92	CE3_n	
SRAM_MODE	31	MODE	
SRAM_BWan	93	BWA_n	
SRAM_BWbn	94	BWB_n	
FSML_WEn	87	BWE_n	
SRAM_GWn	88	GW_n	
SRAM_ADSCn	85	ADSC_n	
SRAM_ADSPn	84	ADSP_n	
SRAM_ADVn	83	ADV_n	
SRAM_ZZ	64	ZZ	

DQ0	58	FSML_D0	
DQ1	59	FSML_D1	
DQ2	62	FSML_D2	
DQ3	63	FSML_D3	
DQ4	68	FSML_D4	
DQ5	69	FSML_D5	
DQ6	72	FSML_D6	
DQ7	73	FSML_D7	
DQ8	8	FSML_D8	
DQ9	9	FSML_D9	
DQ10	12	FSML_D10	
DQ11	13	FSML_D11	
DQ12	18	FSML_D12	
DQ13	19	FSML_D13	
DQ14	22	FSML_D14	
DQ15	23	FSML_D15	
DQPA	74		
DQPB	24		
NC1	1		
NC2	2		
NC3	3		
NC4	6		
NC5	7		
NC6	14		
NC7	16		
NC8	25		
NC9	28		
NC10	29		
NC11	30		
NC12	38		
NC13	39	FSML_A21	
NC14	51		
NC15	52		
NC16	53		
NC17	56		
NC18	57		
NC19	66		
NC20	75		
NC21	78		
NC22	79		
NC23	95		
NC24	96		

VSS: 5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90

SRAM, IS61VPS102418A-250TQL

2.5V → R132, R133, R134, R100 — 10.0K

2.5V → R135, R126, R136, R127, R118 — 10.0K

FLASH 128Mb (8M X 16)

U11 — JS28FxxxP33BF FLASH

2.5V → VPP 43, VCC 33, VCCQ 38

FSML_A1	29	A1	
FSML_A2	25	A2	
FSML_A3	24	A3	
FSML_A4	23	A4	
FSML_A5	22	A5	
FSML_A6	21	A6	
FSML_A7	20	A7	
FSML_A8	19	A8	
FSML_A9	8	A9	
FSML_A10	7	A10	
FSML_A11	6	A11	
FSML_A12	5	A12	
FSML_A13	4	A13	
FSML_A14	3	A14	
FSML_A15	2	A15	
FSML_A16	1	A16	
FSML_A17	55	A17	
FSML_A18	18	A18	
FSML_A19	17	A19	
FSML_A20	16	A20	
FSML_A21	11	A21	
FSML_A22	10	A22(64M)	
FSML_A23	9	NC/A23(128M)	

		D0	34 FSML_D0
		D1	36 FSML_D1
		D2	39 FSML_D2
		D3	41 FSML_D3
		D4	47 FSML_D4
		D5	49 FSML_D5
		D6	51 FSML_D6
		D7	53 FSML_D7
		D8	35 FSML_D8
		D9	37 FSML_D9
		D10	40 FSML_D10
		D11	42 FSML_D11
		D12	48 FSML_D12
		D13	50 FSML_D13
		D14	52 FSML_D14
		D15	54 FSML_D15
		WAIT	56
		VSS	12
		VSS	28
		VSS	31
		RFU0	13
		RFU1	26
		RFU2	27

2.5V → CLK 45

R137	10.0K	FLASH_RESETn	RESET# 44
R138	10.0K	FLASH_CEn	CE# 30
		FSML_OEn	OE# 32
		FSML_WEn	WE# 14
R103	10.0K	FLASH_WPn	ADV# 46, WP# 15

Flash, JS28FxxxP33BF

2.5V → C69 10uF, C53 10uF, C209 0.1uF, C201 0.1uF, C178 0.1uF, C207 0.1uF, C160 4.7nF, C159 0.1uF, C158 0.1uF, C200 0.1uF, C208 0.1uF, C184 0.1uF

2.5V → C210 10uF, C213 0.1uF, C137 10uF, C161 0.1uF, C162 0.1uF, C212 0.1uF, C211 0.1uF, C214 0.1uF

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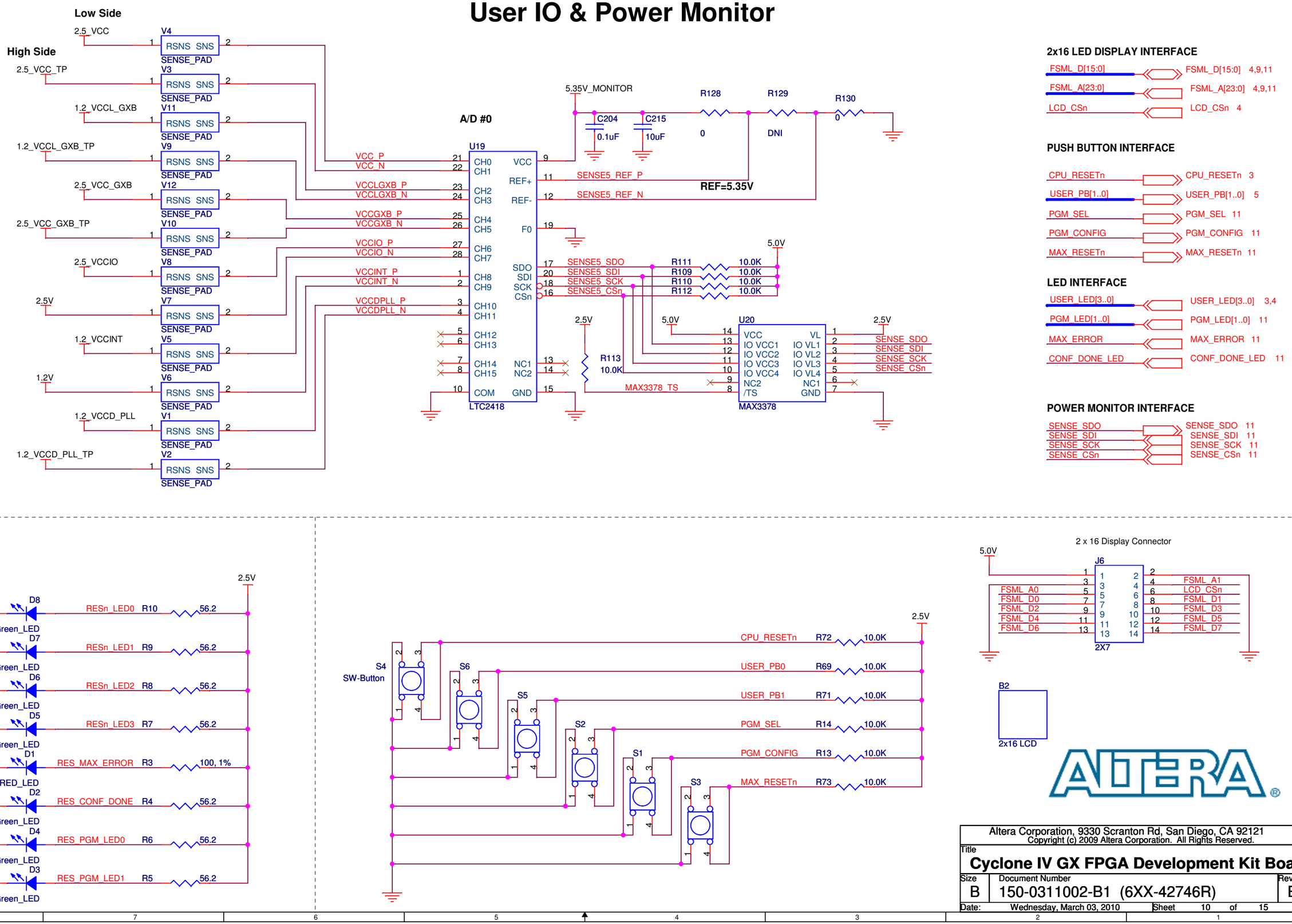
User IO & Power Monitor



2x16 LED DISPLAY INTERFACE

FSML_D[15:0]	FSML_D[15:0]	4,9,11
FSML_A[23:0]	FSML_A[23:0]	4,9,11
LCD_CSn	LCD_CSn	4

PUSH BUTTON INTERFACE

CPU_RESETn	CPU_RESETn	3
USER_PB[1..0]	USER_PB[1..0]	5
PGM_SEL	PGM_SEL	11
PGM_CONFIG	PGM_CONFIG	11
MAX_RESETn	MAX_RESETn	11

LED INTERFACE

USER_LED[3..0]	USER_LED[3..0]	3,4
PGM_LED[1..0]	PGM_LED[1..0]	11
MAX_ERROR	MAX_ERROR	11
CONF_DONE_LED	CONF_DONE_LED	11

POWER MONITOR INTERFACE

SENSE_SDO	SENSE_SDO	11
SENSE_SDI	SENSE_SDI	11
SENSE_SCK	SENSE_SCK	11
SENSE_CSn	SENSE_CSn	11

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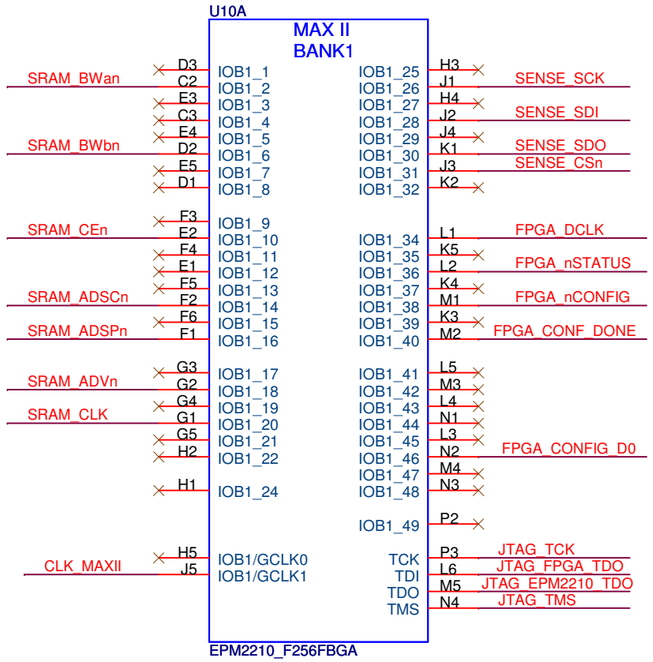
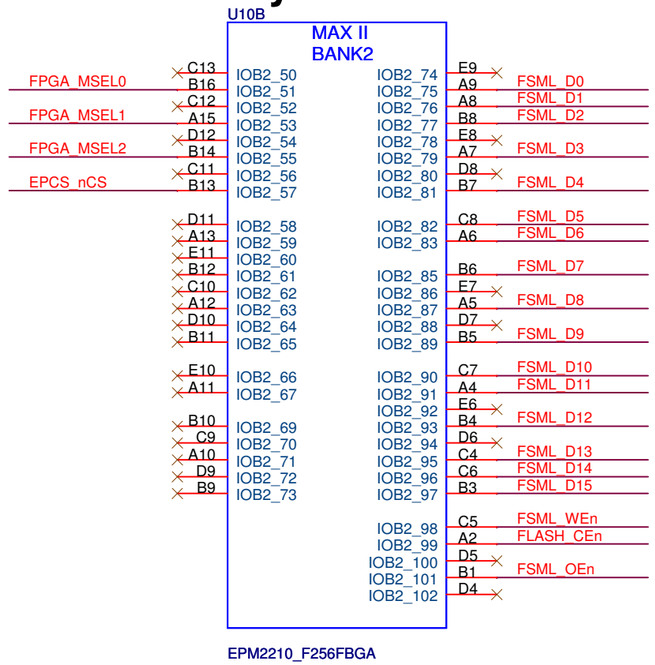
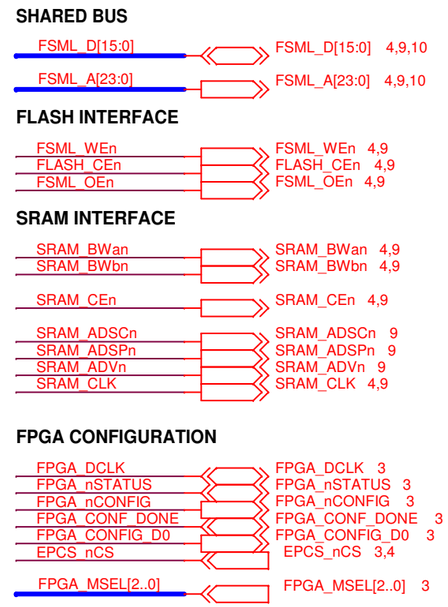
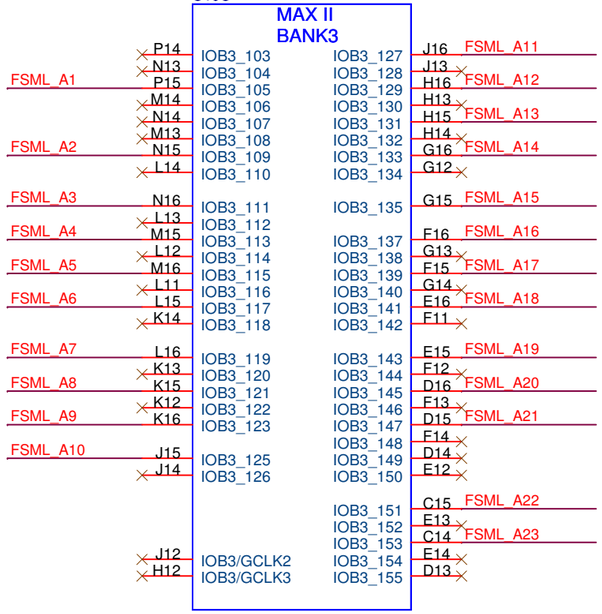
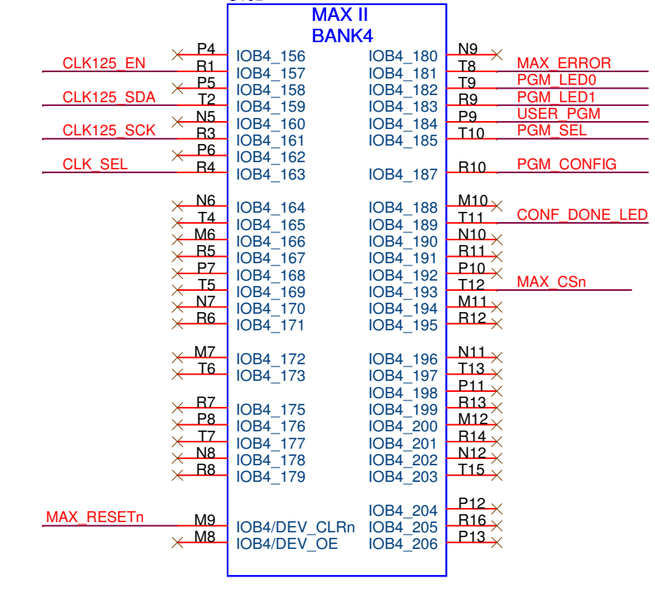
EPM2210 System Controller

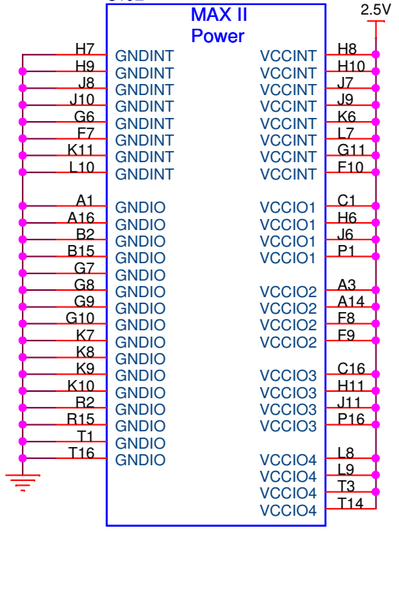




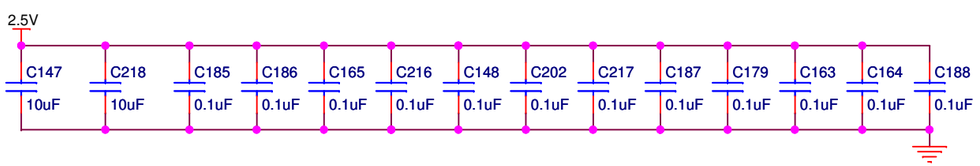








Place near MAX II



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Embedded USB Blaster

USB

J5
USB TYPE-B
USB_CON_5V
L3
BLM21PG331SN1
5V_USB
C35
10uF

U7
SN65220DBV
NC1 A
NC2 B
GNDGND
USB_DM_R
USB_DP_R
R39 27
R38 27
USB_DM
USB_DP

5V_USB
R87
470
USB_AVCC
C124
0.1uF
C145
33nF
5V_USB
2.5V_USB
C144
0.1uF

U5
FT245BL
3V3OUT
AVCC
VCC1
VCC2
VCC-IO
USB_3V3
USBDM
USBDP
RSTOUT#
R95 1.5K
USB_RSTn
XTIN
XTOUT
USB_XTAL1
USB_XTAL2
RESET#
R92 10.0K
USB_RESETn
EECS
EESK
EEDATA
TEST
GND1
GND2
AGND
D0 USB_D0
D1 USB_D1
D2 USB_D2
D3 USB_D3
D4 USB_D4
D5 USB_D5
D6 USB_D6
D7 USB_D7
RD# USB_RDn
WR USB_WR
TXE# USB_TXEn
RXF# USB_RXFn
SI/WU USB_SI_WU
PWREN# USB_PWR_ENn
2.5V_USB
R94
1.00k

C6 18pF USB_XTAL1
X3
CRYSTAL, 6MHz, SMD
C5 18pF USB_XTAL2

5V_USB
DECOUPLING CAPS
C36 10uF
C134 0.1uF
C123 0.1uF

5V_USB
U16
AT93C46DN-SH-B
CS VCC
SK NC1
DIN NC2
DOUT GND
R88
2.2K
USB_EEDATA
R40 10.0K

2.5V_USB
X2
24MHz
EN VCC
GND OUT
C3
0.01uF
CLKIN_24MHZ
C4
0.01uF
2.5V_USB
C146
10uF

2.5V_USB
J13
DNI
R68 1.00K USB_MAX_TCK
R67 1.00K USB_MAX_TDO
USB_MAX_TMS
USB_MAX_TDI
USB_JTAG_PW 0 R80
USB_JTAG_GND 0 R79
2.5V_USB

U4A
MAX II
BANK1
EPM240M100
USB_RXFn
CLKIN_24MHZ
USB_RESETn
IOB1_1 J7
IOB1_2 K10
IOB1_3 K3
IOB1_4 K4
IOB1_5 K5
IOB1_6 K6
IOB1_7 K7
IOB1_8 K9
IOB1_9 L1
IOB1_10 L10 JTAG_BLASTER_TDO
IOB1_11 L11
IOB1_12 L2
IOB1_13 L3 USB_SI_WU
IOB1_14 L4 USB_LED
IOB1_15 L5 USB_DISABLEn
IOB1_16 L6
IOB1_17
IOB1_18
IOB1_19
IOB1_20
IOB1_21
IOB1_22
IOB1_23
IOB1_24
IOB1_25
IOB1_26
IOB1_27
IOB1_28
IOB1_29
IOB1_30
IOB1_31
IOB1_32
IOB1_33 L7
IOB1_34 L9 JTAG_TCK
IOB1/CLK0 K1 USB_MAX_TCK
IOB1/CLK1 J2 USB_MAX_TDI
TCK K2 USB_MAX_TDO
TDI J1 USB_MAX_TMS
TDO
TMS
IOB1/DEV_CLRn
IOB1/DEV_OE

2.5V_USB
R37
56.2
RES_USB_LED
D13
Green_LED

USB BLASTER INTERFACE
JTAG_TCK
JTAG_TMS
JTAG_BLASTER_TDI
JTAG_BLASTER_TDO
JTAG_TCK 3,11
JTAG_TMS 3,11
JTAG_BLASTER_TDI 3
JTAG_BLASTER_TDO 3
USB_DISABLEn
USB_DISABLEn 3

U4B
MAX II
BANK2
EPM240M100
USB_TXEn A1
USB_D1 A10
USB_D0 A11
USB_WR A2
USB_RDn A3
USB_D7 A4
USB_D6 A5
USB_D5 A6
USB_D4 A7
USB_D3 A8
USB_D2 A9
IOB2_35 B5
IOB2_36 B6
IOB2_37 B7
IOB2_38 B8
IOB2_39 B9
IOB2_40 C10
IOB2_41 C11
IOB2_42 C5
IOB2_43 C6
IOB2_44 C7
IOB2_45 D10
IOB2_46 D11 USB_PWR_ENn
IOB2_47 D9
IOB2_48 E10
IOB2_49 E11 USB_EECS
IOB2_50 F11 USB_EESK
IOB2_51
IOB2_52
IOB2_53
IOB2_54
IOB2_55
IOB2_56
IOB2_57
IOB2_58
IOB2_59
IOB2_60
IOB2_61
IOB2_62
IOB2_63
IOB2_64
IOB2_65
IOB2_66
IOB2_67 F9
IOB2_68 G10
IOB2_69 H10
IOB2_70 H11 EEDATA
IOB2_71 H9
IOB2_72 J10
IOB2/CLK2 J11 JTAG_TMS
IOB2/CLK3 K11 JTAG_BLASTER_TDI
IOB2_73
IOB2_74

U4C
MAX II
Power
EPM240M100
GNDIO D5
GNDIO D7
GNDIO E4
GNDIO E8
GNDIO G4
GNDIO G8
GNDIO H5
GNDIO H7
VCCINT E9
VCCINT G3
VCCIO1 E3
VCCIO1 J4
VCCIO1 J8
VCCIO2 C4
VCCIO2 C8
VCCIO2 G9
2.5V_USB

2.5V_USB
PLACE NEAR MAX II
C101 0.1uF
C102 0.1uF
C125 0.1uF
C110 0.1uF
C111 0.1uF

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Power - 2.5V and 1.2V Output

9V - 16V DC Input

J4 CONN JACK PWR

DC_INPUT

D19 FM540

C1 10uF

12V_PCIE

D9 MBRS340

DC_MAIN

U2 FDS6575

C22 47uf, C25 10uF, C24 0.1uF, C23 0.1uF

R1 10.0K, R2 10.0K, CTL

U1 LTC4412 — VIN, GND, CTL, SENSE, GATE, STAT — Power Controller, LTC4412

GATE

CONDITION	DESCRIPTION
DC INPUT = ON PCIE = OFF	- CTL of LTC4412 go LOW and TURN ON the MOSFET, DC INPUT flow through to DC MAIN. - D9 MBRS340 used to prevent DC MAIN flow back to 12V PCIE
DC INPUT = OFF PCIE = ON OR DC INPUT = ON PCIE = ON	- Logical HIGH on CTL forces the gate to source voltage of the primary P-channel MOSFET power switch to a small voltage (VGOFF). - This will turn the MOSFET off and no current will flow from the primary power input at VIN if the MOSFET is configured so that the drain to source diode does not forward bias. - VGS of MOSFET go HIGH and disable the junction. DC INPUT will be blocked while 12V PCIE flow through DC MAIN

LT3510_SHDn — LT3510_SHDn 14

5.0V, C112 10uF, D20 BAT54AW

U3 LT3510 — VIN1, SHDN, BST1, SW1, IND1, VOUT1, PG1, FB1, VC1, SS/TRACK1, GND, VIN2, RT/SYNC, BST2, SW2, IND2, VOUT2, PG2, FB2, VC2, SS/TRACK2 — Regulator, LT3510

R28 120k, R12 10.0K, R30 4.02K, R29 8.06k, D11 MBRS340, C39 1000PF VC1_C, R31 24.9k, C34 0.1uF, C38 1000PF VC2_C, R25 24.9k, D10 MBRS340, R26 16.9k, R27 8.06k, R11 10.0K

C93 0.1uF, L2 4.7uH, C94 0.1uF, L1 8.2uH

DC_MAIN: C12 10uF, C15 10uF, C14 0.1uF, C13 0.1uF

1.2_VCCINT: R74 0.003, C91 10uF, C86 10uF

1.2V

1.2_VCCL_GXB: R82 0.003, C103 10uF

1.2_VCCL_GXB_TP: BLM21PG331SN1 L6

1.2_VCCD_PLL: R65 0.003, C83 10uF

1.2_VCCD_PLL_TP: BLM21PG331SN1 L4

C85 10uF, C84 10uF

2.5V: R75 0.003, C92 10uF — 2.5_VCCIO

2.5_VCC_GXB_TP: L7 BLM21PG331SN1, R83 0.003, C104 10uF — 2.5_VCC_GXB

2.5_VCC_TP: L5 BLM21PG331SN1, R66 0.003, C90 10uF — 2.5_VCC

C89 10uF, C87 10uF, C88 10uF

5.0V: R36 1.00k, BLUE_PU, D12 BLUE LED

ALTERA

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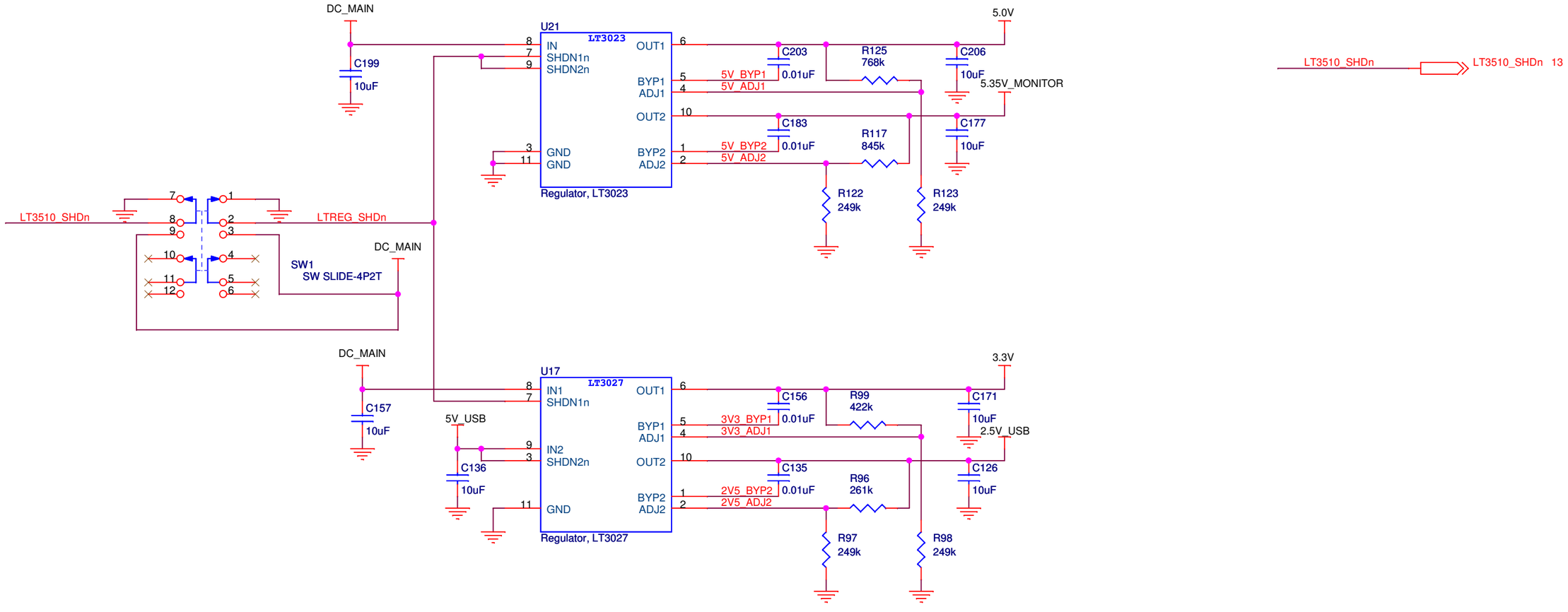
Power - 5.0V, 5.35V, 3.3V and 2.5V Output



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Cyclone IV GX FPGA Development Kit Board

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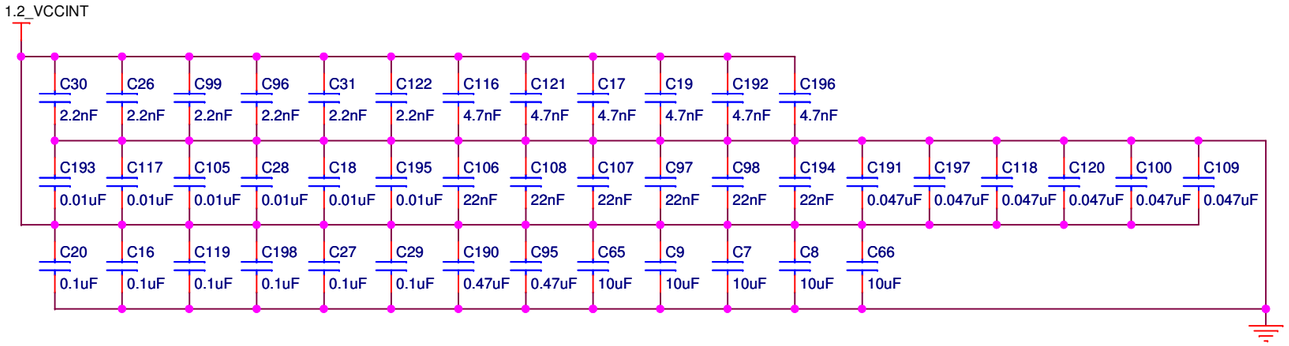
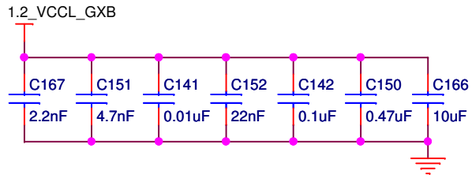
Cyclone IV GX Decoupling

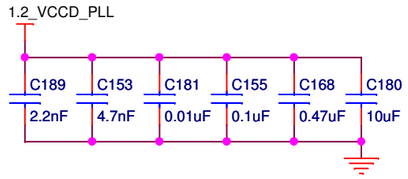
Cyclone IV GX VCCINT



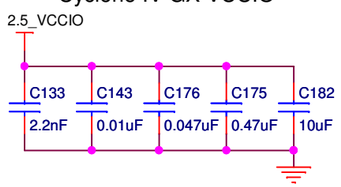
Cyclone IV GX VCCL GXB



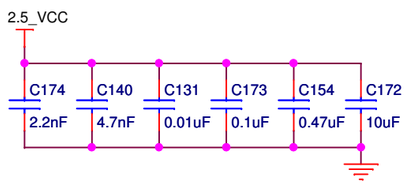
Cyclone IV GX VCCD PLL



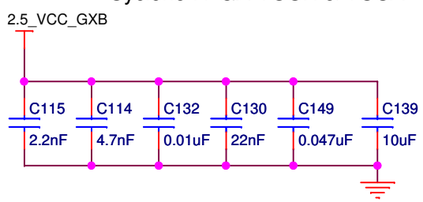
Cyclone IV GX VCCIO

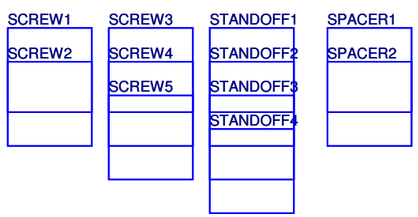


Cyclone IV GX VCCA PLL and VCC CLKIN



Cyclone IV GX VCCH & VCCA





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