Cyclone IV GX Clocks

Cyclone IV GX Clocks

Bank 3A
- PCLK1: CLKOUT1
- PCLK2: CLKOUT2
- PCLK3: CLKOUT3
- PCLK4: CLKOUT4
- PCLK5: CLKOUT5
- PCLK6: CLKOUT6
- PCLK7: CLKOUT7
- PCLK8: CLKOUT8

Bank 3B
- PCLK1: CLKOUT1
- PCLK2: CLKOUT2
- PCLK3: CLKOUT3
- PCLK4: CLKOUT4
- PCLK5: CLKOUT5
- PCLK6: CLKOUT6
- PCLK7: CLKOUT7
- PCLK8: CLKOUT8

Bank 4
- PCLK1: CLKOUT1
- PCLK2: CLKOUT2
- PCLK3: CLKOUT3
- PCLK4: CLKOUT4
- PCLK5: CLKOUT5
- PCLK6: CLKOUT6
- PCLK7: CLKOUT7
- PCLK8: CLKOUT8

Bank 5
- PCLK1: CLKOUT1
- PCLK2: CLKOUT2
- PCLK3: CLKOUT3
- PCLK4: CLKOUT4
- PCLK5: CLKOUT5
- PCLK6: CLKOUT6
- PCLK7: CLKOUT7
- PCLK8: CLKOUT8

Bank 6
- PCLK1: CLKOUT1
- PCLK2: CLKOUT2
- PCLK3: CLKOUT3
- PCLK4: CLKOUT4
- PCLK5: CLKOUT5
- PCLK6: CLKOUT6
- PCLK7: CLKOUT7
- PCLK8: CLKOUT8

Bank 7
- PCLK1: CLKOUT1
- PCLK2: CLKOUT2
- PCLK3: CLKOUT3
- PCLK4: CLKOUT4
- PCLK5: CLKOUT5
- PCLK6: CLKOUT6
- PCLK7: CLKOUT7
- PCLK8: CLKOUT8

Bank 8A
- PCLK1: CLKOUT1
- PCLK2: CLKOUT2
- PCLK3: CLKOUT3
- PCLK4: CLKOUT4
- PCLK5: CLKOUT5
- PCLK6: CLKOUT6
- PCLK7: CLKOUT7
- PCLK8: CLKOUT8

Bank 8B
- PCLK1: CLKOUT1
- PCLK2: CLKOUT2
- PCLK3: CLKOUT3
- PCLK4: CLKOUT4
- PCLK5: CLKOUT5
- PCLK6: CLKOUT6
- PCLK7: CLKOUT7
- PCLK8: CLKOUT8
General Clock Circuitry

Clock Enable

From EPM2210

NIOs CPU Clock

From EPM2210 and DIP SW1

LVPECL INPUT CLOCK

CLKA_SEL Settings:

Setting | SWx, DIP4
---------|---------
High    | PCLKp/n
Low     | CLKn/n

CLOCK INTERFACE

From EPM2210

To NIOS CPU Clock

From EPM2210 and DIP SW1

To Board Settings DIP Switch

From EPM2210

To FPGA and EPM2210

CLOCK INTERFACE

From EPM2210

User Factory

Cyclone IV GX FPGA Development Kit Board

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assign ssram_gwn = 1'b1; // HIGH Global Write Enable—Writes all bytes; active low
assign ssram_adv = 1'b1; // HIGH
assign ssram_adscn = 1'b0; // LOW
assign ssram_adspn = 1'b1; // HIGH
10/100/1000 Ethernet

RGMII Mode (default)

removed ENET_IN_TX signal.

removed ENET_IN_RX signals.

removed ENET_IN_CLK signal. Attached to ground.

removed ENET_RX activities with r445 and D6.

removed ENET_RX_CLK and ENET_RX_CLK signals.

removed ENET_LED_ACTIVITY with r445 and D6.

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Power 1, (2.5V, 1.2V and 12V)
Power 3, (DDR2 (VREF/VTT), 5.0V, 1.8V FPGA VCCIO, 1.1V Ethernet)
FPGA Decoupling

Place 6 vias minimum on each X2Y cap.