Cyclone III F780 Development Kit Host
Block Diagram

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Current Sense

Place (1) 0.1uF near VDD of ADG725.
Place (2) 0.1uF and (1) 1.0uF near V+ of INA271.
Place (1) 0.1uF and (1) 1.0uF near V+ of AD7940.

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Version Number:
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Date: Saturday, May 28, 2011
150-0310703-03
Rev D-3
Cyclone III Power
10/100/1000 Ethernet
High Speed Mezzanine (HSM) Interface
By default all of the data signal on the HSMC’s are single ended. 100 Ohm resistors should be installed between the P/N pairs in order to use differential signals.

High Speed Mezzanine (HSM) Termination

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**HSMA PORT A**
- HSMA_CLK_IN_P[2:1]
- HSMA_CLK_IN_N[2:1]
- HSMA_RX_D_P[16:0]
- HSMA_RX_D_N[16:0]
- HSMA_CLK_IN_P[2:1] 7,14
- HSMA_CLK_IN_N[2:1] 7,14
- HSMA_RX_D_P[16:0] 14,18
- HSMA_RX_D_N[16:0] 14,18

**HSMB PORT A**
- HSMB_CLK_IN_P[2:1]
- HSMB_CLK_IN_N[2:1]
- HSMB_RX_D_P[16:0]
- HSMB_RX_D_N[16:0]
- HSMB_CLK_IN_P[2:1] 7,14
- HSMB_CLK_IN_N[2:1] 7,14
- HSMB_RX_D_P[16:0] 14,18
- HSMB_RX_D_N[16:0] 14,18

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**HSMA PORT B**
- HSMA_CLK_IN_P[2:1]
- HSMA_CLK_IN_N[2:1]
- HSMA_RX_D_P[16:0]
- HSMA_RX_D_N[16:0]
- HSMA_CLK_IN_P[2:1] 7,14
- HSMA_CLK_IN_N[2:1] 7,14
- HSMA_RX_D_P[16:0] 14,18
- HSMA_RX_D_N[16:0] 14,18

**HSMB PORT B**
- HSMB_CLK_IN_P[2:1]
- HSMB_CLK_IN_N[2:1]
- HSMB_RX_D_P[16:0]
- HSMB_RX_D_N[16:0]
- HSMB_CLK_IN_P[2:1] 7,14
- HSMB_CLK_IN_N[2:1] 7,14
- HSMB_RX_D_P[16:0] 14,18
- HSMB_RX_D_N[16:0] 14,18
Cyclone III Configuration

USB Blaster Programming Header

2.5V

2.5V

JTAG CYCLONE III OR MAXII SELECT

MAX II JTAG CHAIN OR JTAG PINS SELECT 2.5V

JTAG REFERENCE

JUMPER 1 will be used to select between a direct JTAG connection to the FPGA or the Micro. By default it will select a direct connection to the FPGA. JUMPER 2 will select to configure with the JTAG II (JTAG) header. By default it will select to configure with the IN.

PASSIVE SERIAL STANDARD: MSEL[3:0]=0000
PASSIVE SERIAL FAST: MSEL[3:0]=1100
MSEL pins have internal 5kOhm pull-downs.

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REV: D-3
Decoupling