

# Arria 10 SoC FPGA Development Kit Board

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REV	DATE	PAGES	DESCRIPTION
A1		All	INITIAL REVISION A RELEASE
A1.1		22	Change RGMII reference clock source, pull up to 1v8
		40	DP clock netname is changed
		42	LED resistors are changed to 100ohm
		6,52,57	Change ED8101 I2C address to 0X0E and 0X10
		55,68,69	Change DMP3098L to DMG2305UX,
		28	Change netnames
		45	Change Header to 0.1inch header
		55	Add logic to turn off A10 power when MAXV need be reprogrammed.
		55,68	Change PMOS to NMOS for reducing ON resistance
		56	ADD two LDOs for U31
		51	ADD Linear LDOs for U24
		19	HPS DM alert bit positions are modified based on Quartus report
		38	Move Mictor trace JTAG into 1.8 Bank of Max2
		36	Connect 3V3 to BANK4
		05	Update Clock diagram
A2		21	Add 1K PULL UP resistors for MSEL[0..2], HPS.NPOR, HPS.NRST ( only in SCH)
		25	Change R98 and R99 to 1K ohm
		22	Change R367 and R378 to 4.7K ohm
		74	Change R646 pull up voltage to I01V8, Change R674 to 100K ohm
		51	Need install U74,install D44, R156, DNI R157 Based on FB 282099
		45	Change LCD address to 0x28
		56	Install D43
		60	Update the sense RC netowrk values based on FB 261730, add +-15% voltage adjustable range
		59	Update the sense RC netowrk values based on FB 261730
		66	Update the sense RC netowrk values based on FB 261730
		64	Update the sense RC netowrk values based on FB 261730
		63	Update the sense RC netowrk values based on FB 261730
		62	Update the sense RC netowrk values based on FB 261730
		54	Update the sense RC netowrk values based on FB 261730
		57	Change remote sensing point to FPGA pins
		60	Change R495 value from 240K to 226K for generating 1.03V output
		57	Change ED8101P01QI to ED8101P04QI for 0.95V output
		52	Change ED8101P02QI to ED8101P05QI for 0.95V output
		51,52,56,57	Change R5258, R5243, R5045 & R5055 from 2K to 1.5K based on FB302118
		22	Change Linear LDO from LTC3026 to LTC3026-1
A3		21	Change R676 to 22.0 ohm, and R679 to 0 ohm



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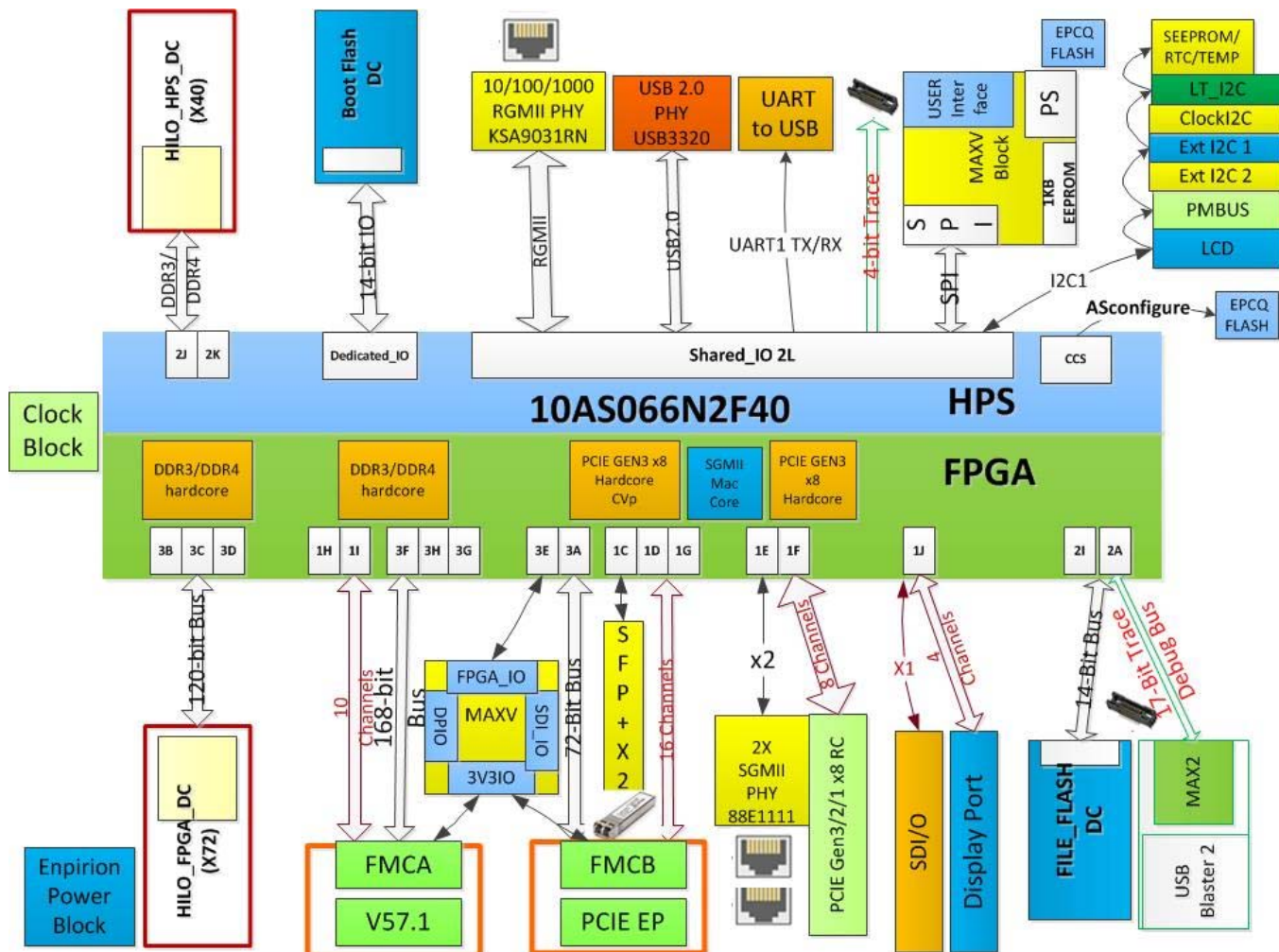
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# Arria 10 Dev Kit Block Diagram

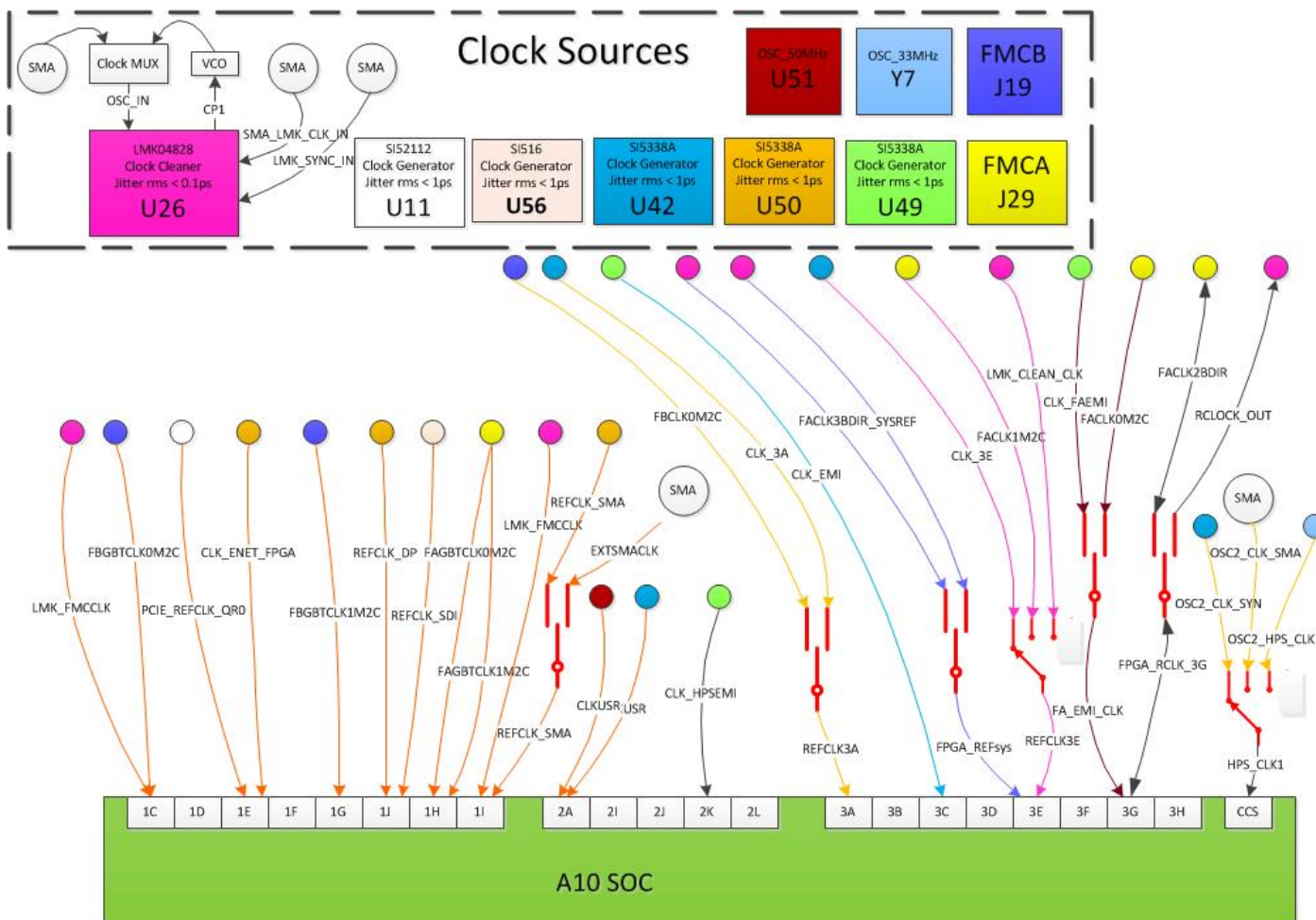


V57.1 Two FMC Slots



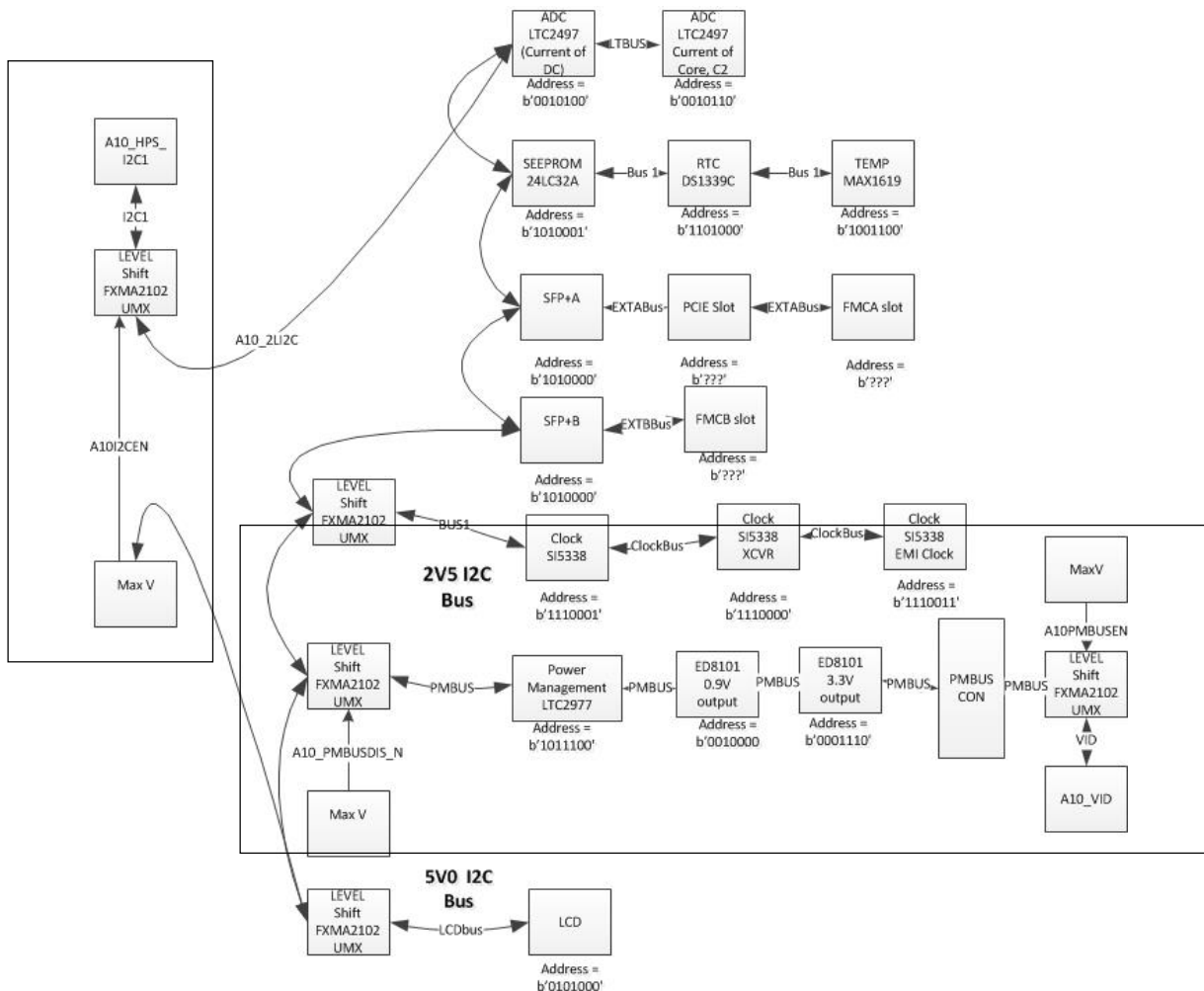
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# Arria 10 Dev Kit Clock Connection



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# Arria 10 Dev Kit I2C bus Connection

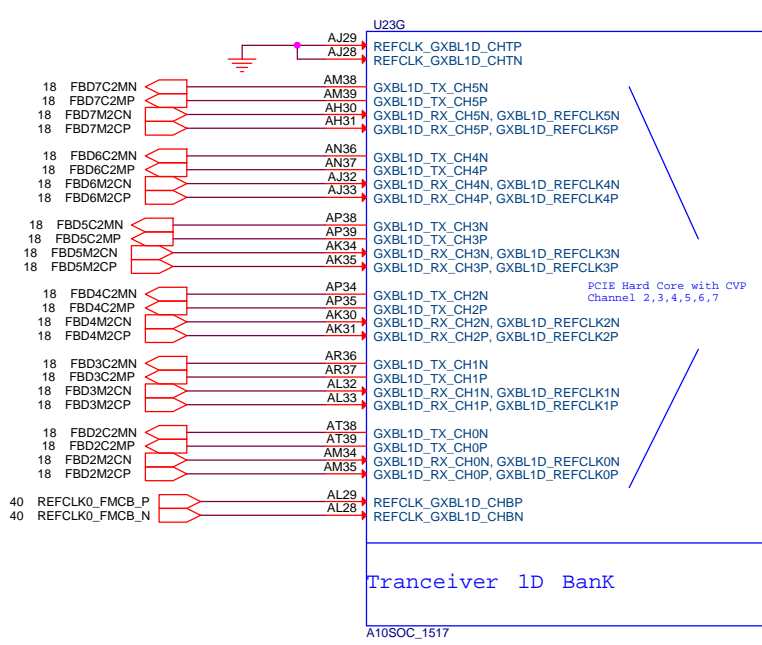
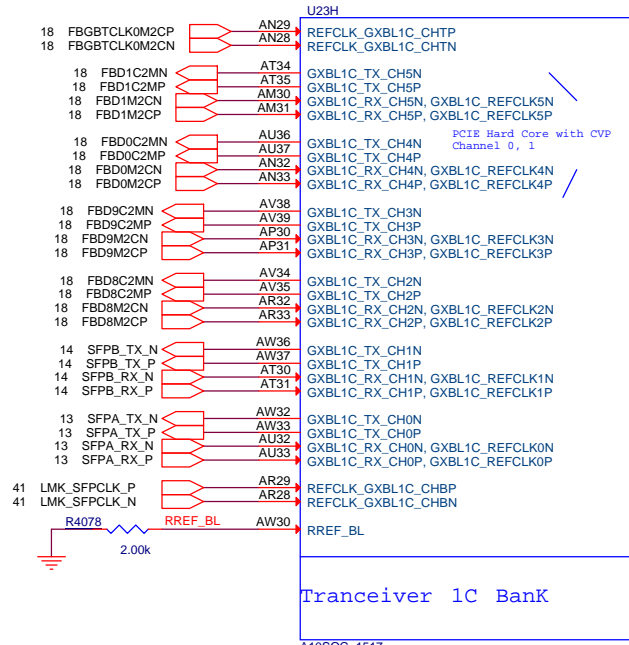


Application of two I2C masters in PMVID bus



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# FMCB (PCIE END-POINT) XCVRS & 2 x SFP + XCVRs



Application	Channel (Bank, number)
PCIE EP	(1C,4);(1C,5);(1D,0);(1D,1);(1D,2);(1D,3);(1D,4);(1D,5)
FMC B Slot DP Tranceiver [0:9]	(1C,2);(1C,3);(1C,4);(1C,5);(1D,0);(1D,1);(1D,2);(1D,3);(1D,4);(1D,5);
SFP+ 0 and 1	(1C,0);(1C,1)



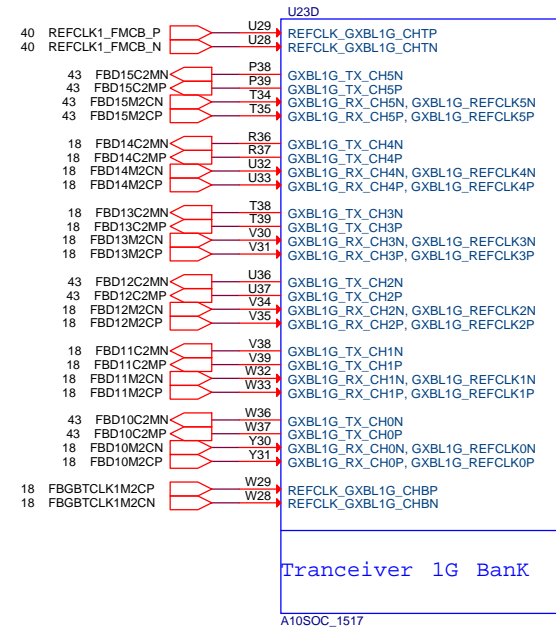
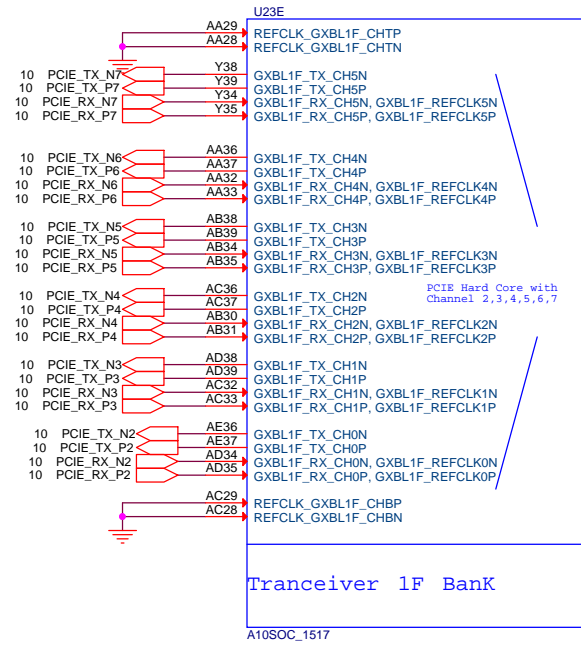
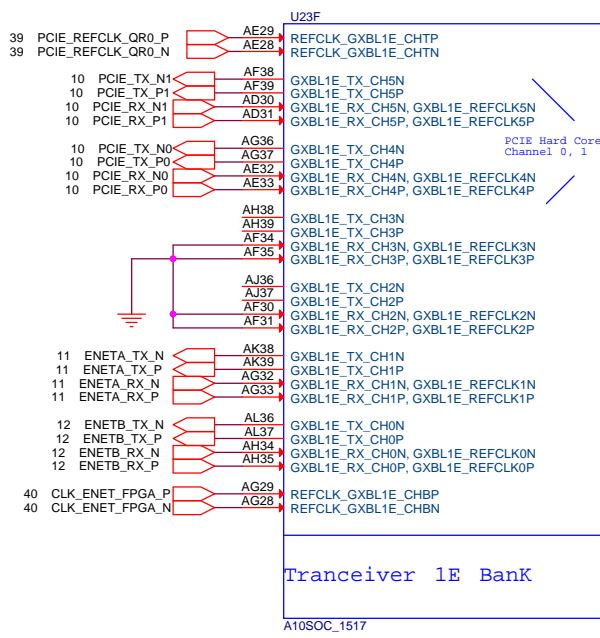
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# PCIE RC XCVRs & 2X SGMII XCVRs & FMCB XCVRs



Application	Channel (Bank, number)
PCIE RC	(1E, 4); (1E, 5); (1F, 0); (1F, 1); (1F, 2); (1F, 3); (1F, 4); (1F, 5)
FMC B Slot DP Transceiver [10:15]	(1G, 0); (1G, 1); (1G, 2); (1G, 3); (1G, 4); (1G, 5);
SGMII A and B	(1E, 0); (1E, 1)



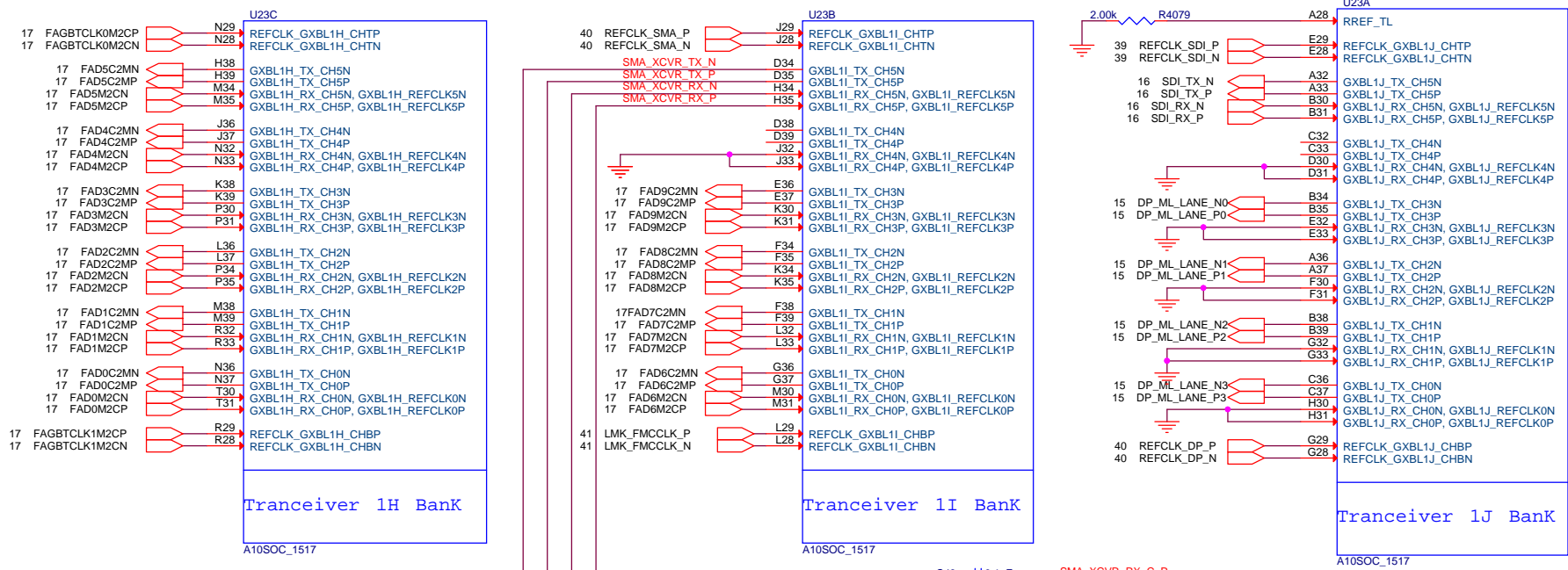
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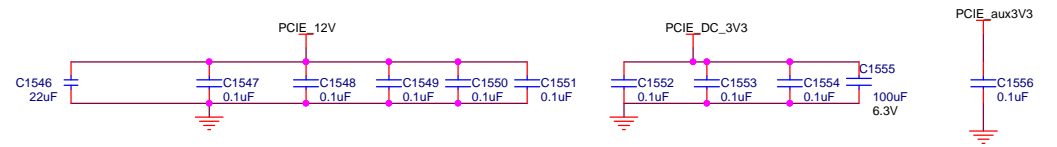
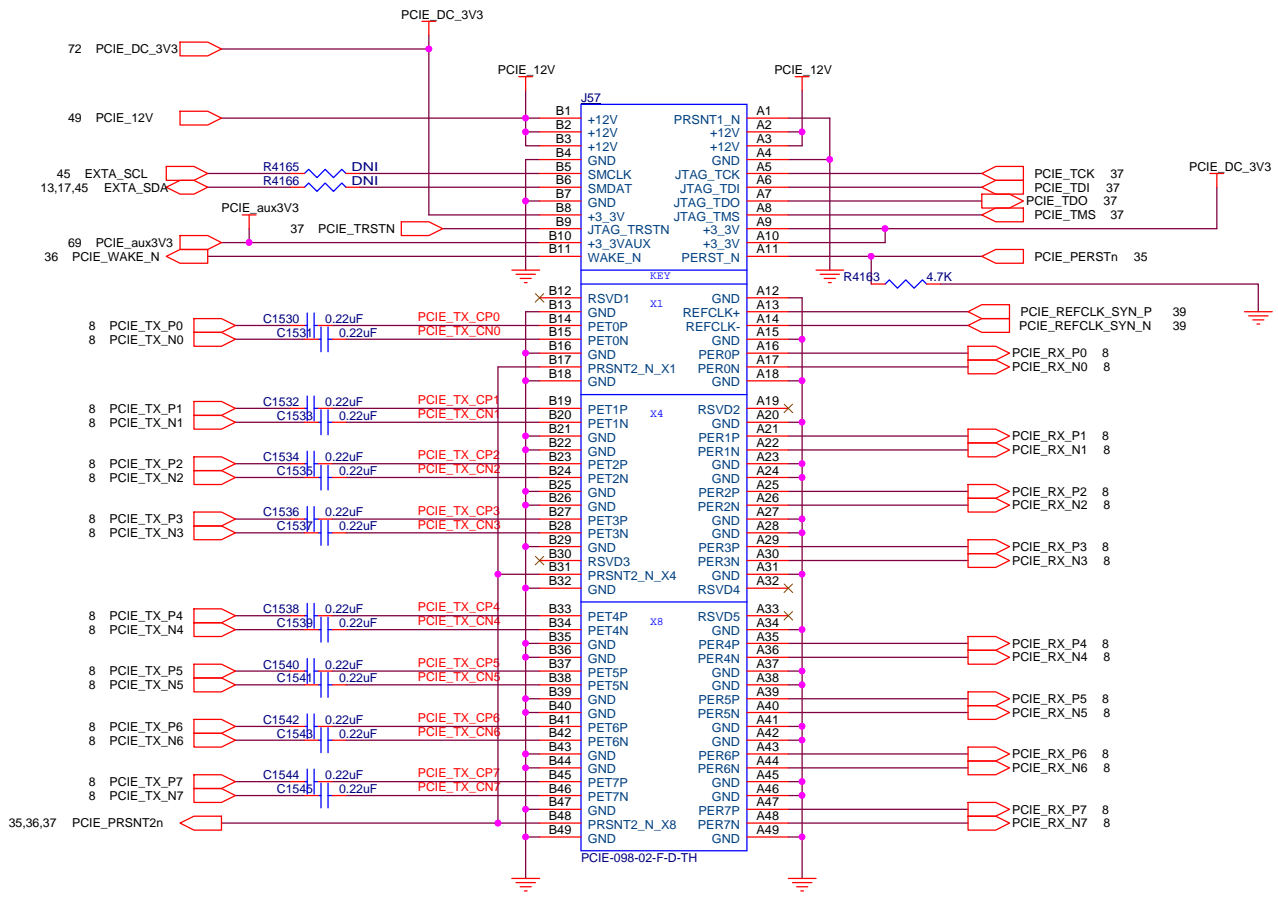
# DP & SDI & FMCA XCVRs & SMA XCVR



Application	Channel (Bank, number)
SMA	(1I, 5)
FMC A Slot DP Transceiver [0:9]	(1H, 0); (1H, 1); (1H, 2); (1H, 3); (1H, 4); (1H, 5); (1I, 0); (1I, 1); (1I, 2); (1I, 3);
SDI	(1J, 5)
Display Port	(1J, 0); (1J, 1); (1J, 2); (1J, 3)



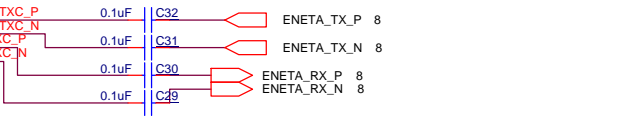
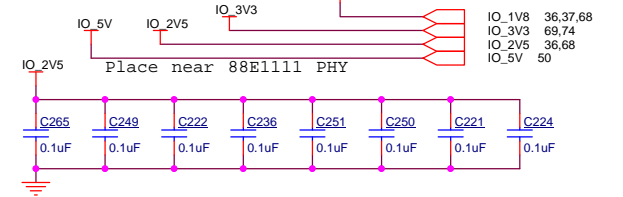
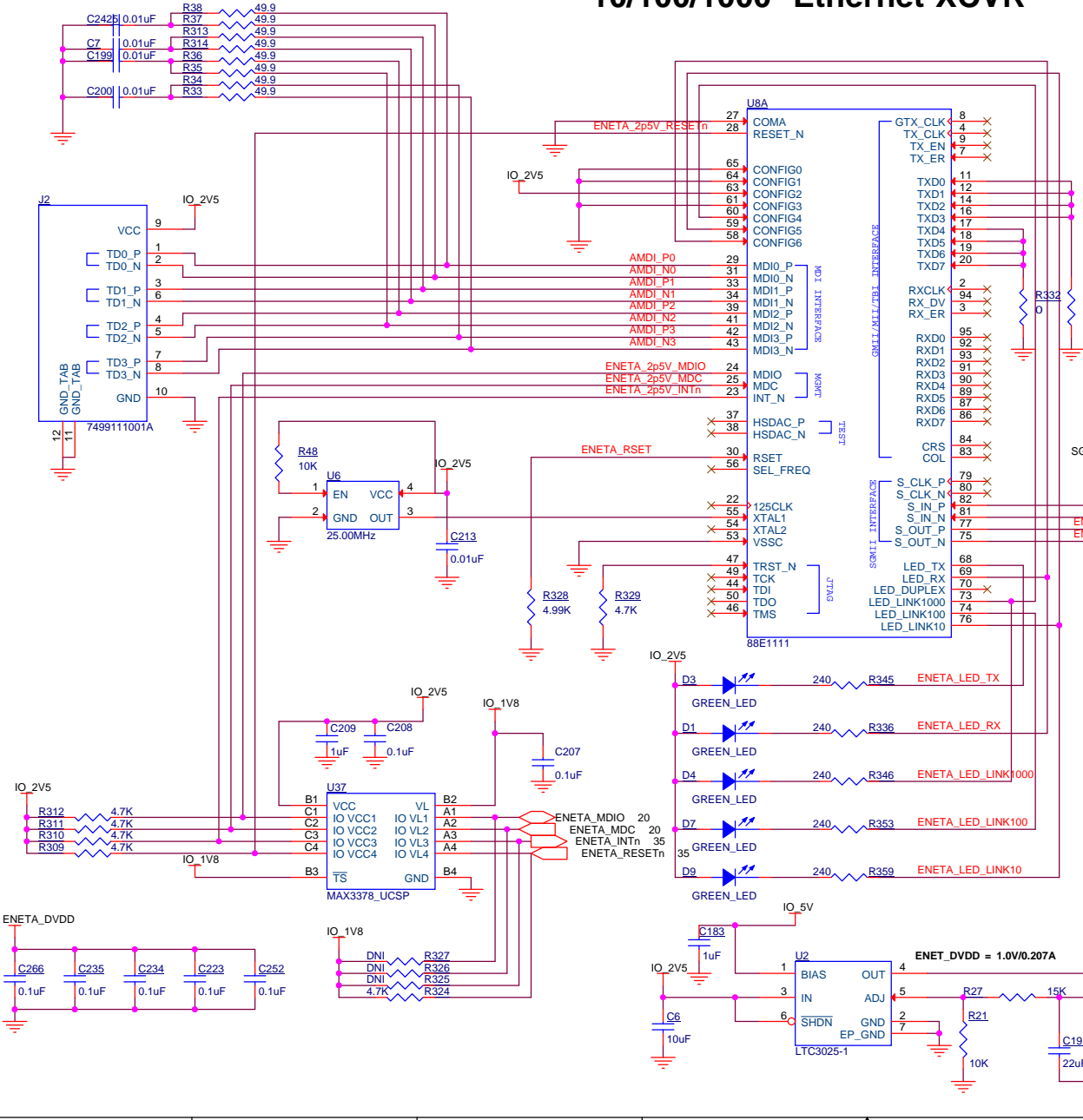
# PCI Express GEN3 X 8 Connector



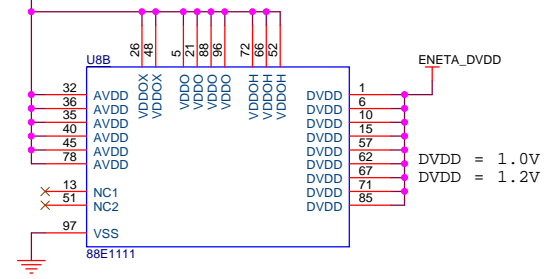
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# 10/100/1000 Ethernet XCVR

Pin	Pin Connection	Setting Bit[2:0]	Definition
CONFIG0	GND	000	MDIO PHY Address bit (2.0) = 000
CONFIG1	GND	000	Enable Pause, PHY Address bits (4.3) = 00
CONFIG2	VDDO (2.5V or 3.3V)	111	1110 = Auto-negotiate, advertise all capabilities, prefer Master 100BASE-x FULL-DUPLEX/Auto-Negotiation enabled, 100BASE-X half-duplex
CONFIG3	GND	000	Disable crossover, Enable 125CLK
CONFIG4	LED_LINK1000	100	Hardware Config Mode Reg (2.0) = 100 SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	LED_LIN10	110	Disable fiber/copper autoselect, disable sleep mode (enable energy detect), Hardware Config Mode Reg (3) = 0
CONFIG6	LED_RX	010	Select MDIO (over 2-wire serial), interrupt polarity = active low, 50-ohm termination for fiber



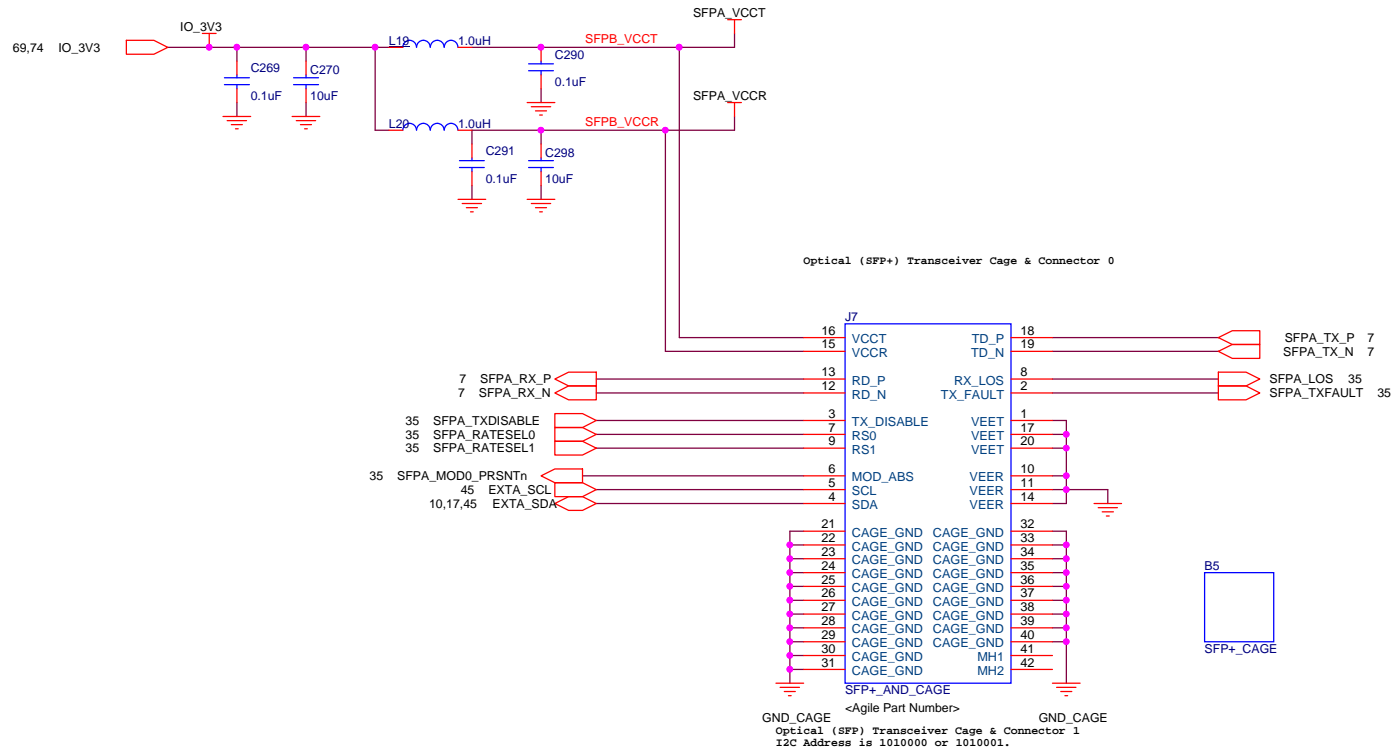
**88E1111-B2-CAA1C000 EOL**  
**88E1111-B2-NDC2C000 Replacement**



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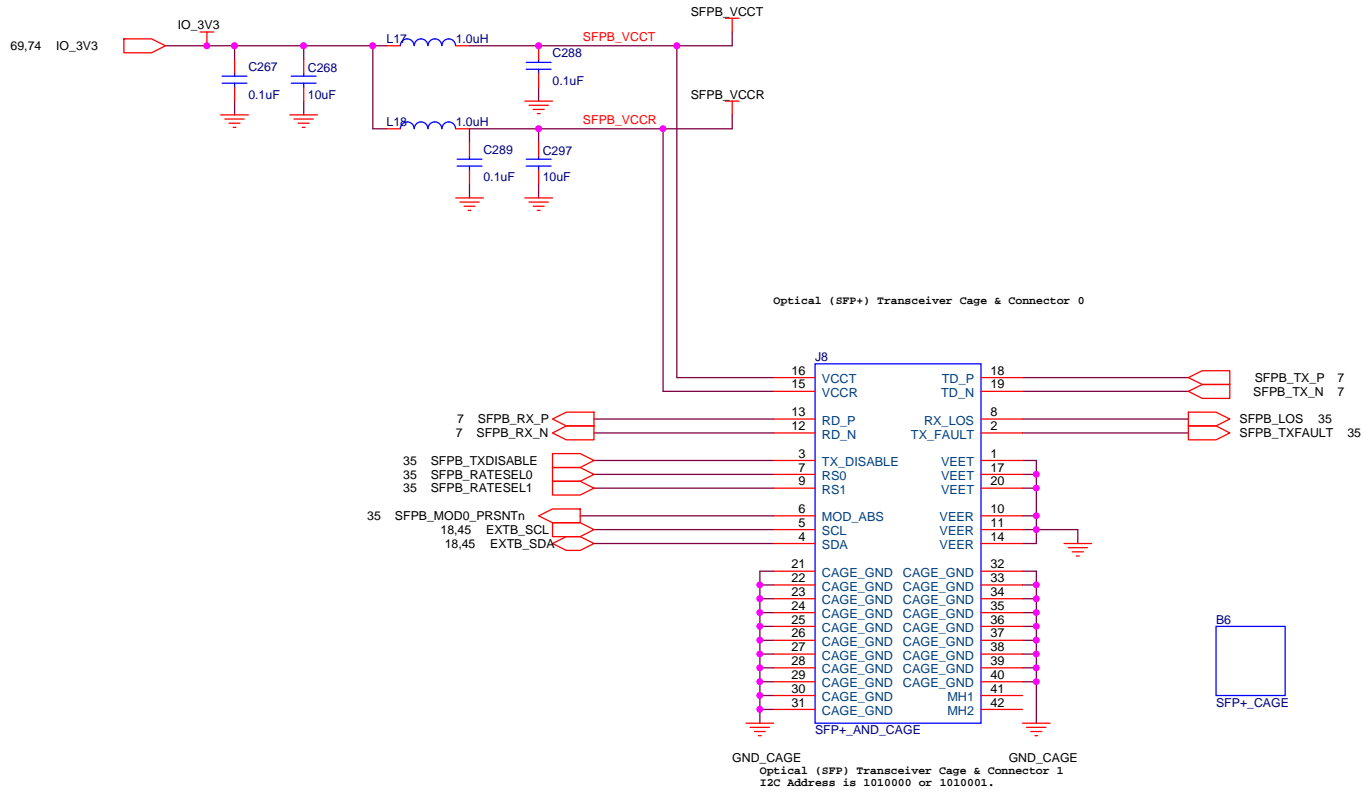


# Small Form Factor Pluggable Plus (SFP+) Port A



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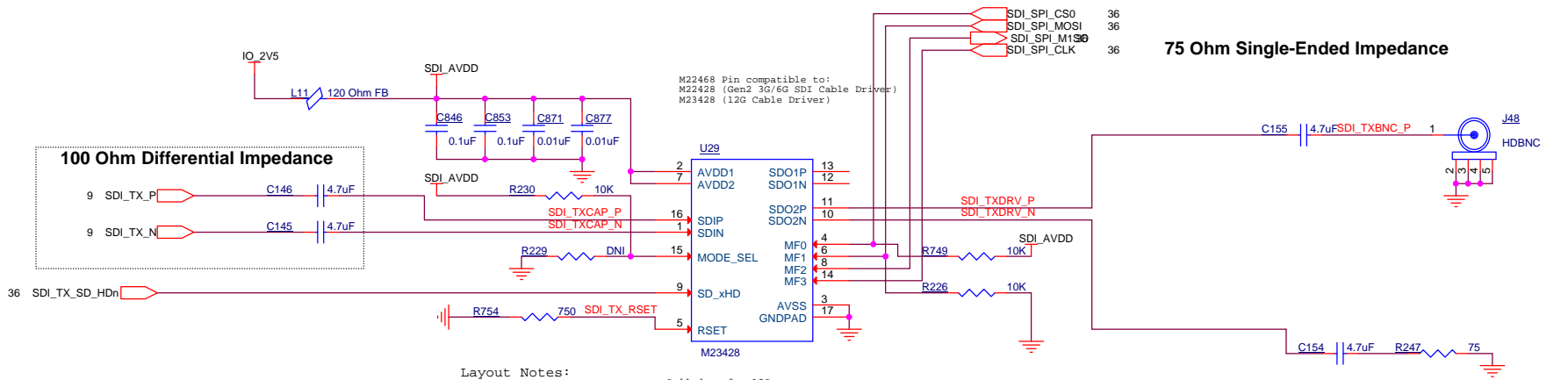
# Small Form Factor Pluggable Plus (SFP+) Port B



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# SDI Cable Driver, Equalizer, and SMB



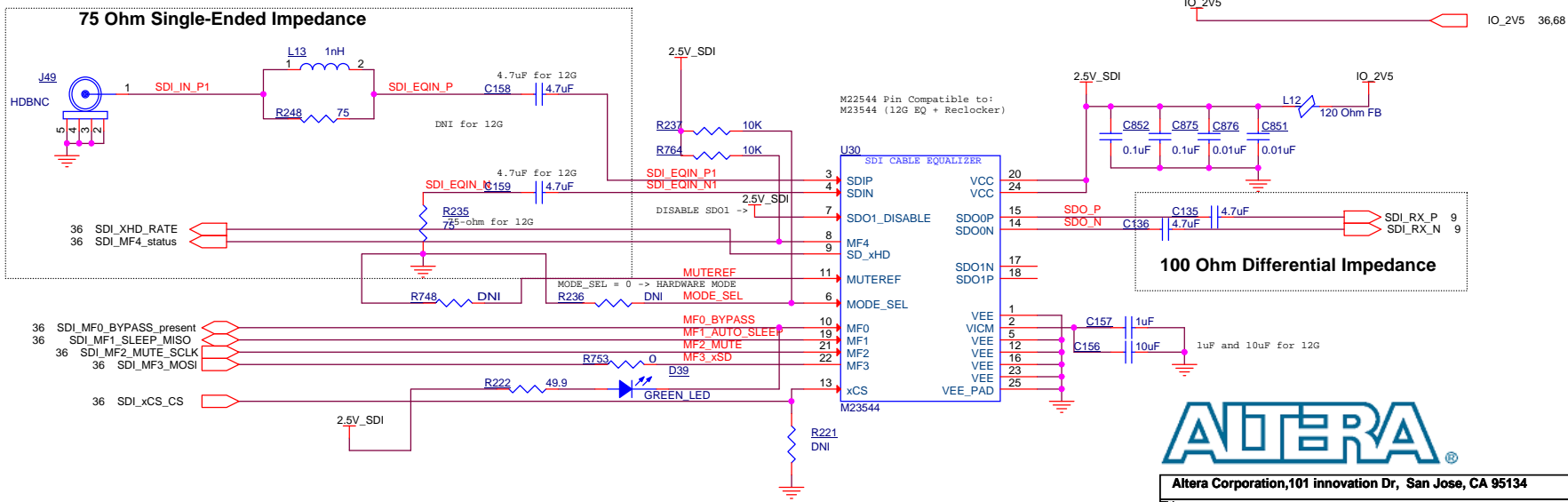
**100 Ohm Differential Impedance**

**75 Ohm Single-Ended Impedance**

Layout Notes:  
DNI for resistors and capacitors for GEN2 devices.  
Minimize stubs in layout.

Pull-down for 12G

Layout Notes (M23428) SDI Cable Driver:  
- The RSET resistor should be located close to pin 5.  
- Remove GND under pin 5 and the RSET resistor.  
- The 49.9-ohm resistors should be placed close to device pins 16 and 1 (SDIP/SDIN).



**75 Ohm Single-Ended Impedance**

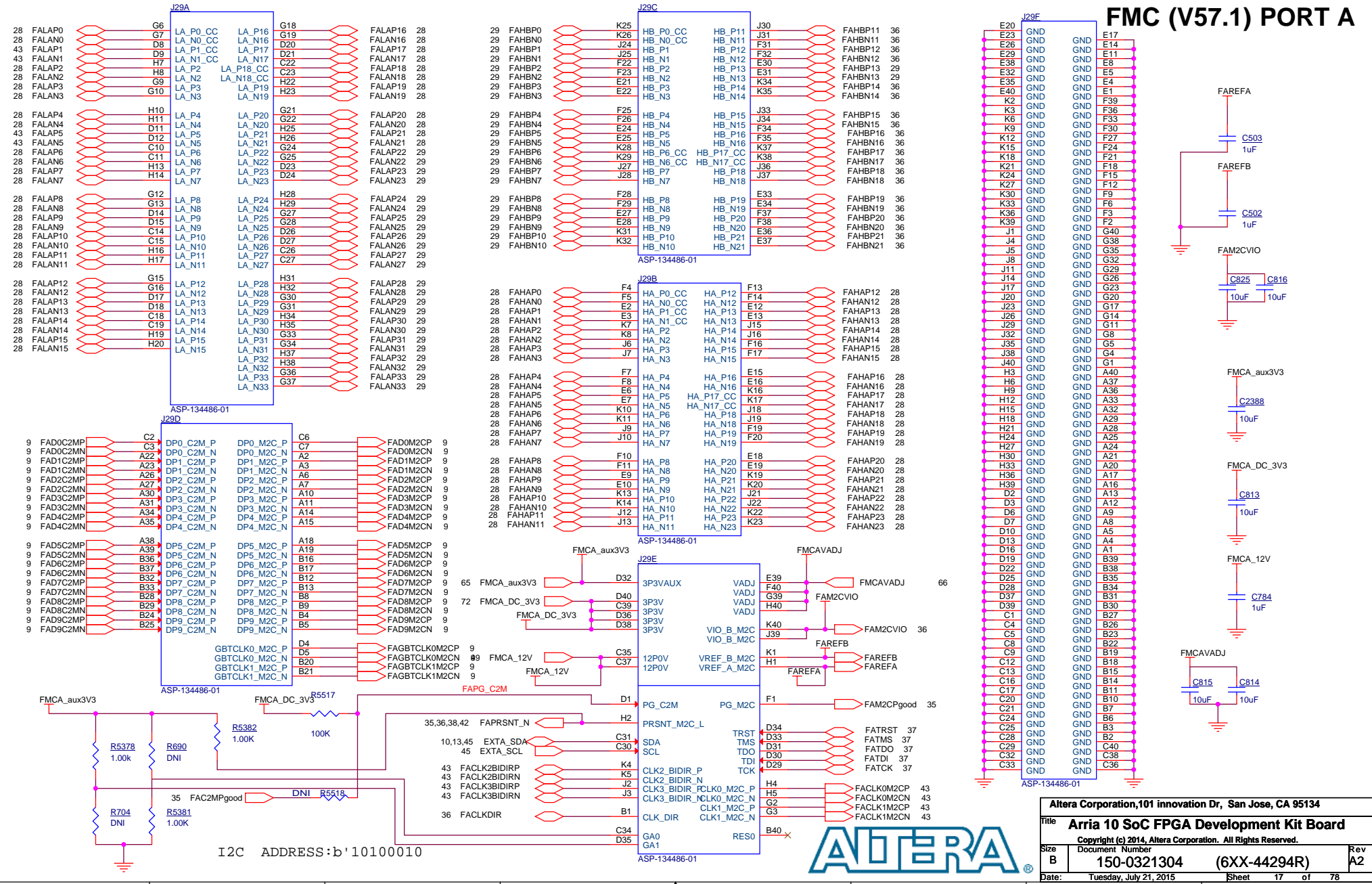
**100 Ohm Differential Impedance**

Layout Notes (M22544) SDI Cable Equalizer:  
- The AGC 33nF capacitor should be located close to the device pins 8 and 9 (AGC+/AGC-).  
- Clear GND under the AGC 33nF capacitor.



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# FMC (V57.1) PORT A



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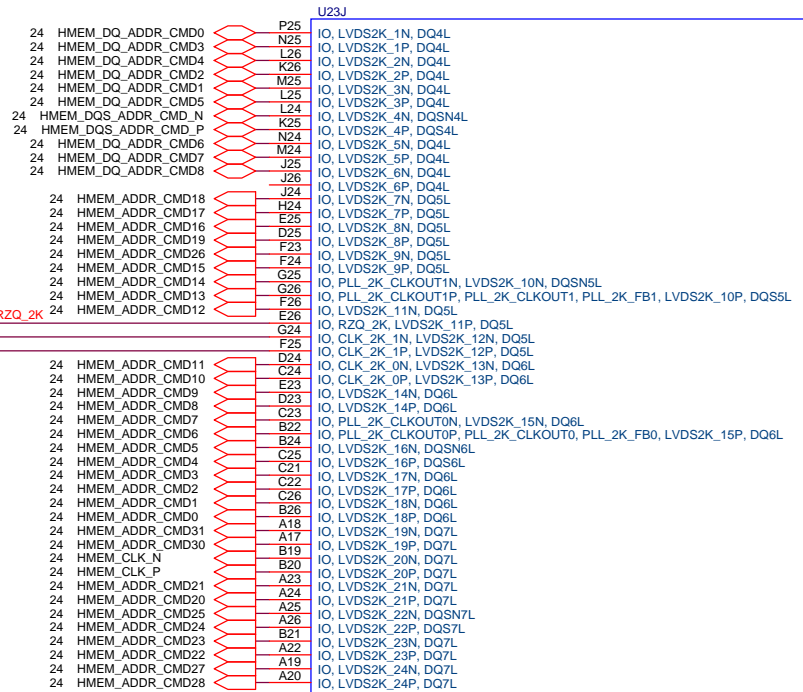
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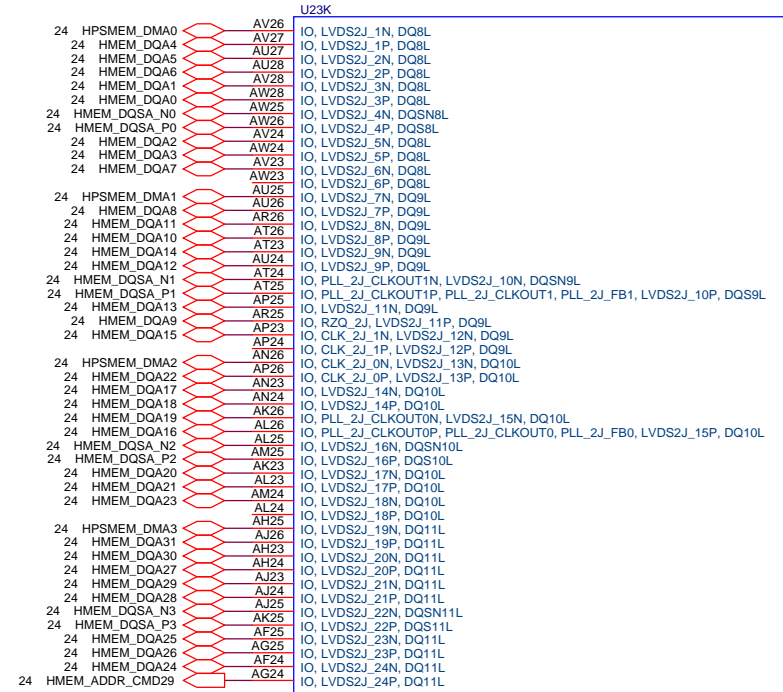


# HPS HILO DDR3/DDR4 IOS



IO BANK 2K, HPS Memory BANK

A10SOC\_1517



IO BANK 2J, HPS Memory BANK

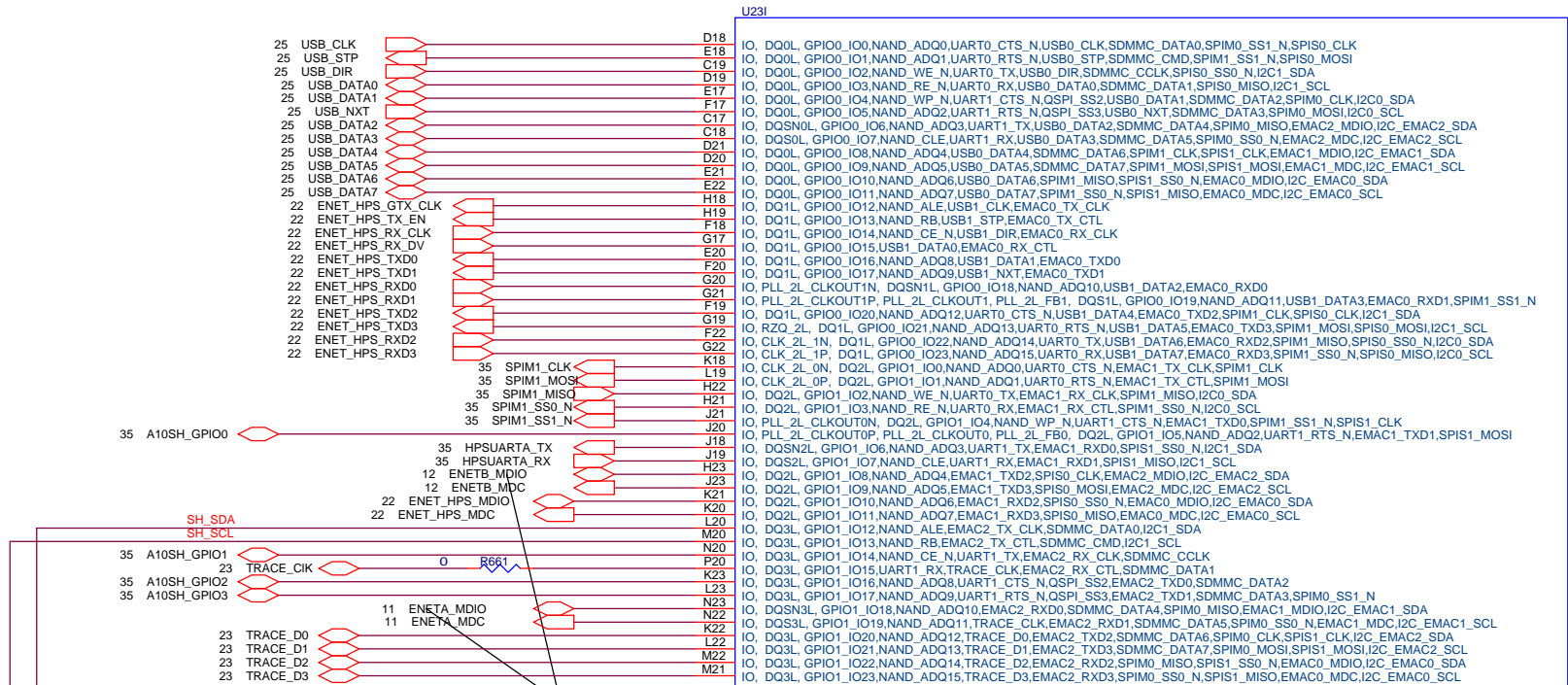
A10SOC\_1517

All HPS memory IO pin assignment must be same as Quartus'



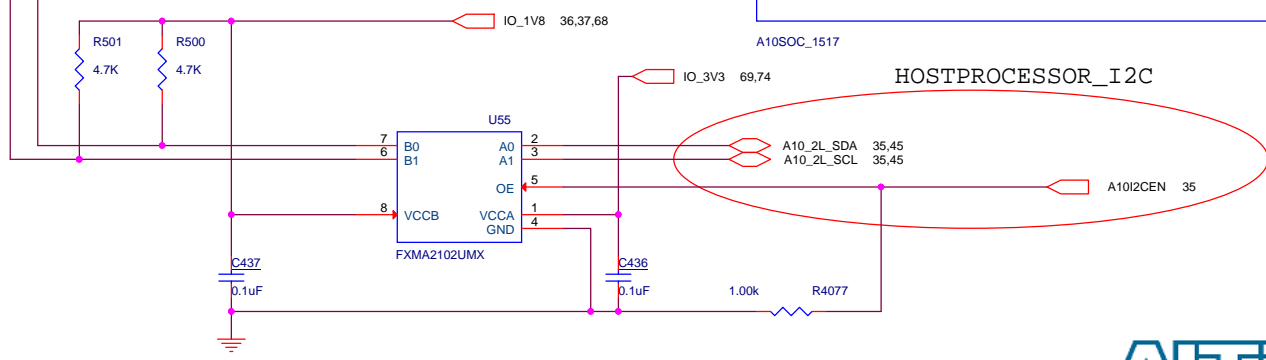
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# HPS Shared IOs



MDIO/MDIC and data ports need be routed into FPGA logic

IO BANK 2L, 3V0,2V5,1V8 BANK

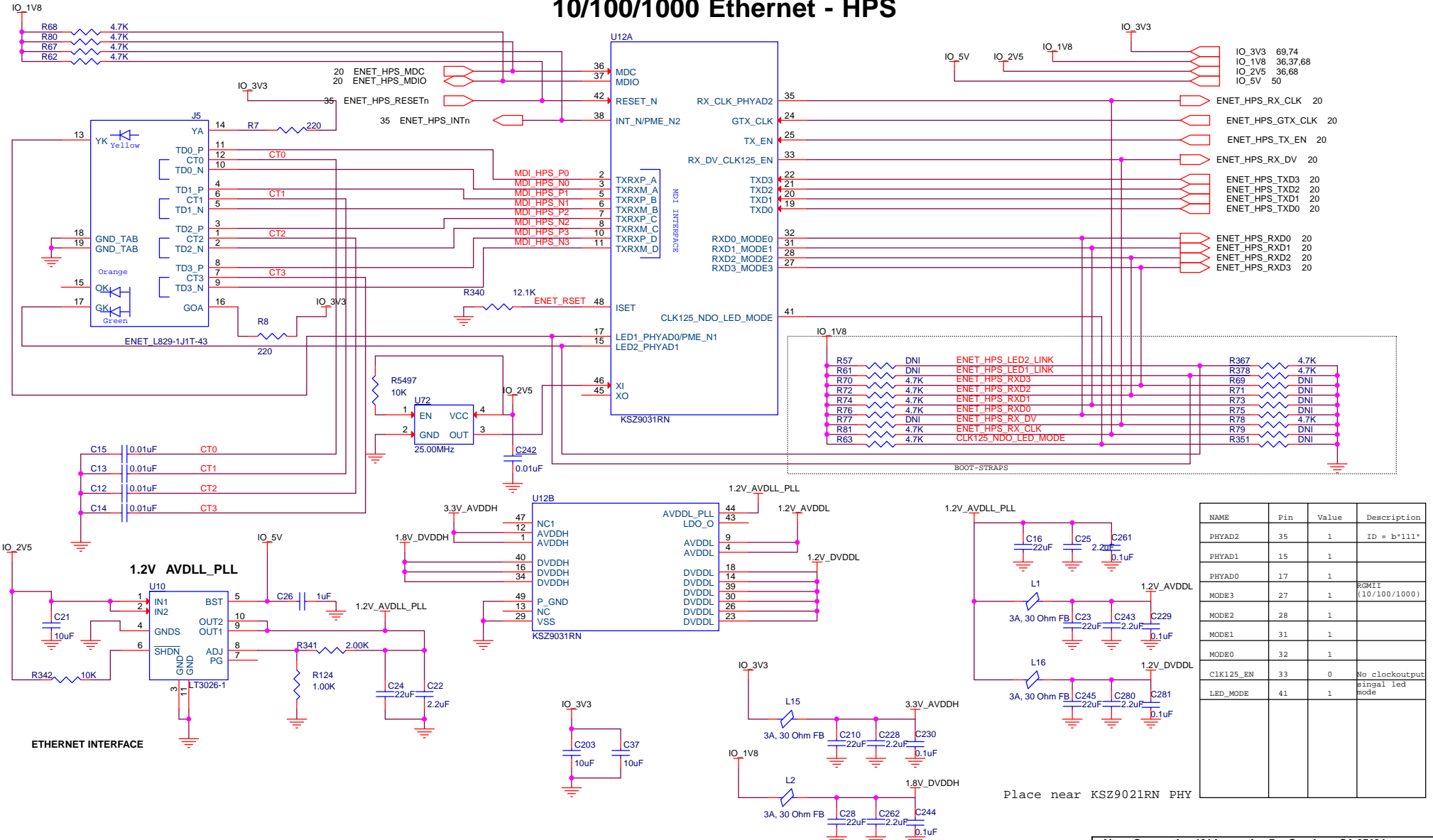


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# 10/100/1000 Ethernet - HPS



NAME	Pin	Value	Description
PHYAD2	35	1	ID = b*111*
PHYAD0	15	1	
PHYAD1	17	1	
MODE3	27	1	sgmii (10/100/1000)
MODE2	28	1	
MODE1	31	1	
MODE0	32	1	
CLK125_EN	33	0	No clockoutput singal led mode
LED_MODE	41	1	

Place near KCSZ9021RN PHY

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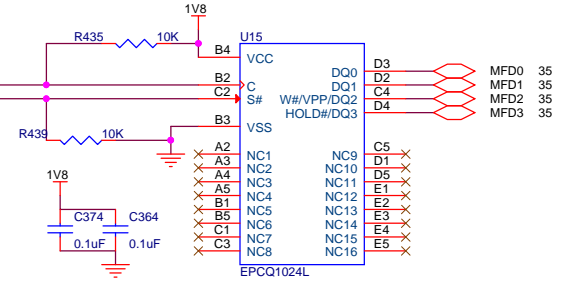
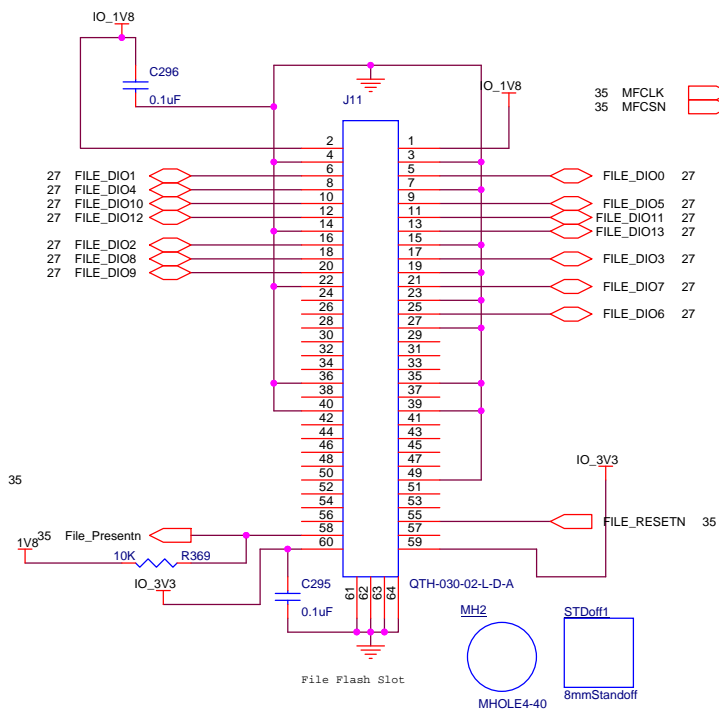
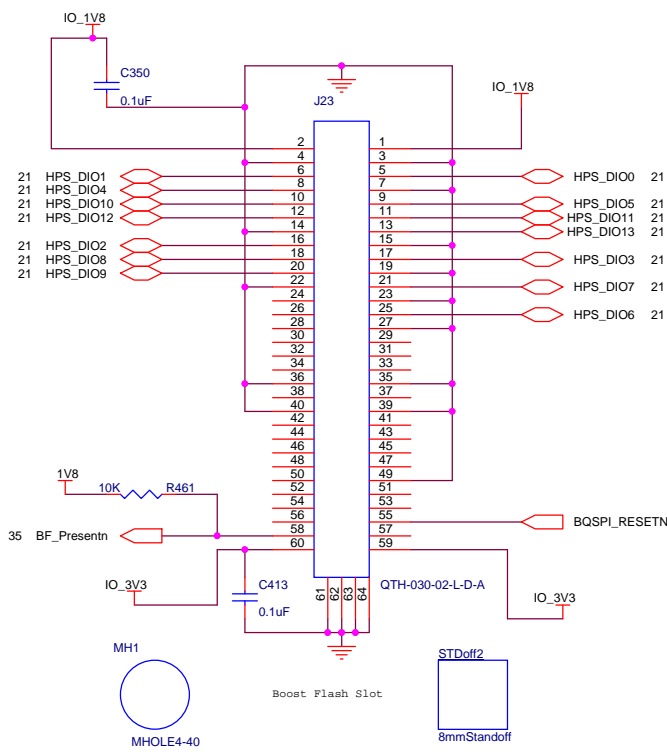
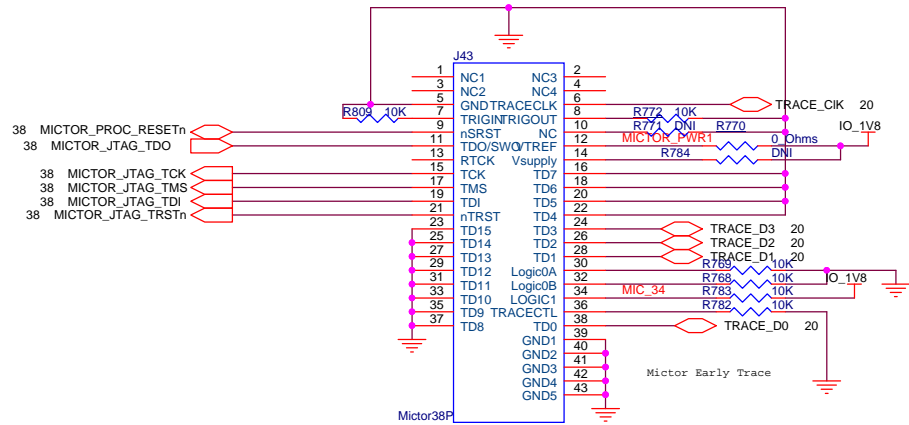
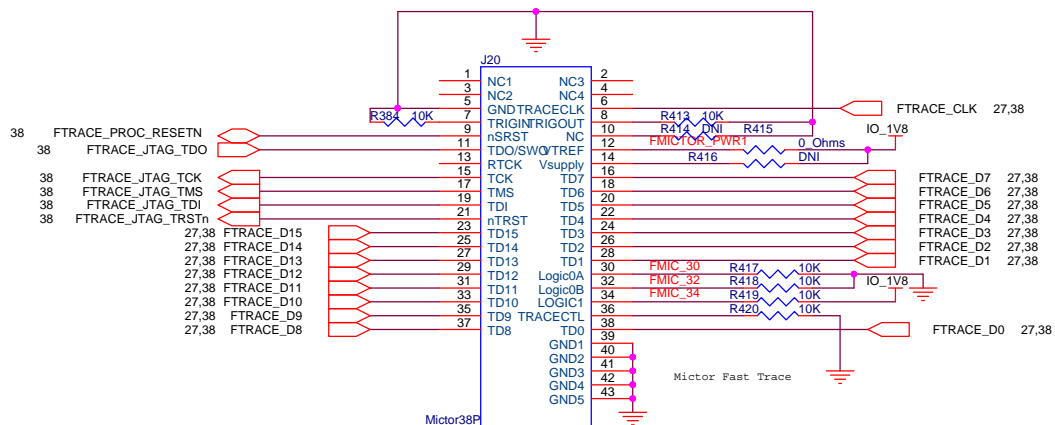
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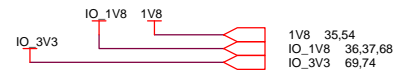
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# Connectors of Boot flash, file flash, early trace and fast trace



MAXV PS Flash



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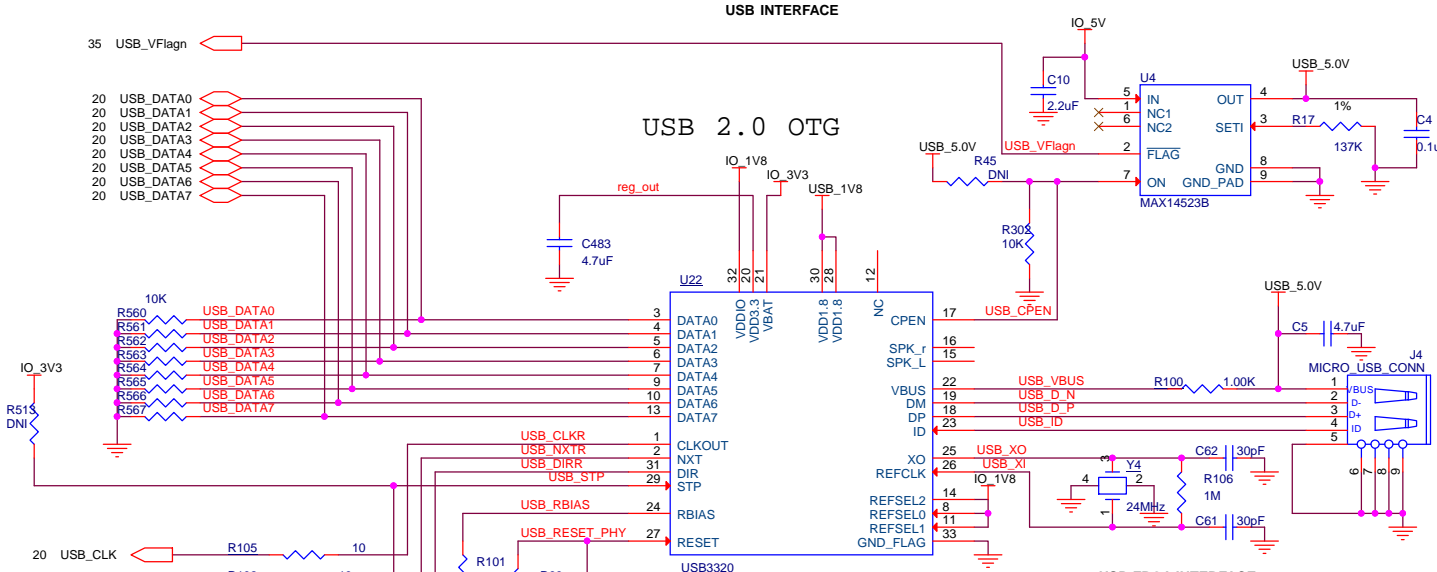


# USB Ports

Current limit for Rreseti of 137k is 1.013A

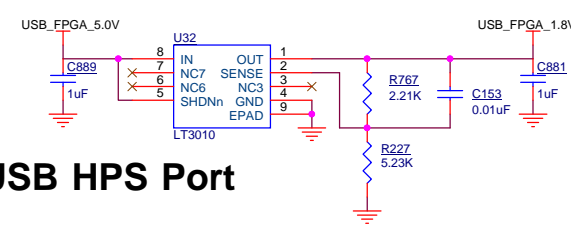
## USB INTERFACE

### USB 2.0 OTG

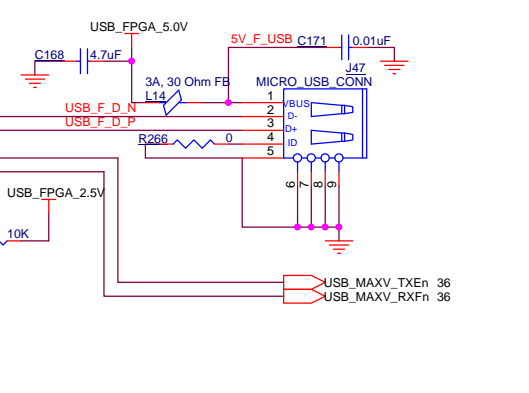


REFSEL[2:0] = 0X7, Reference Frequency = 24Mhz

## USB HPS Port



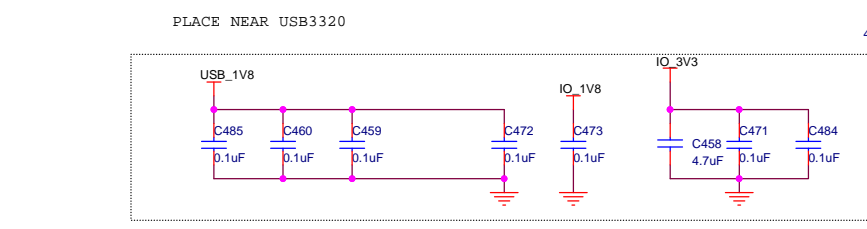
## USB TI GUI Port



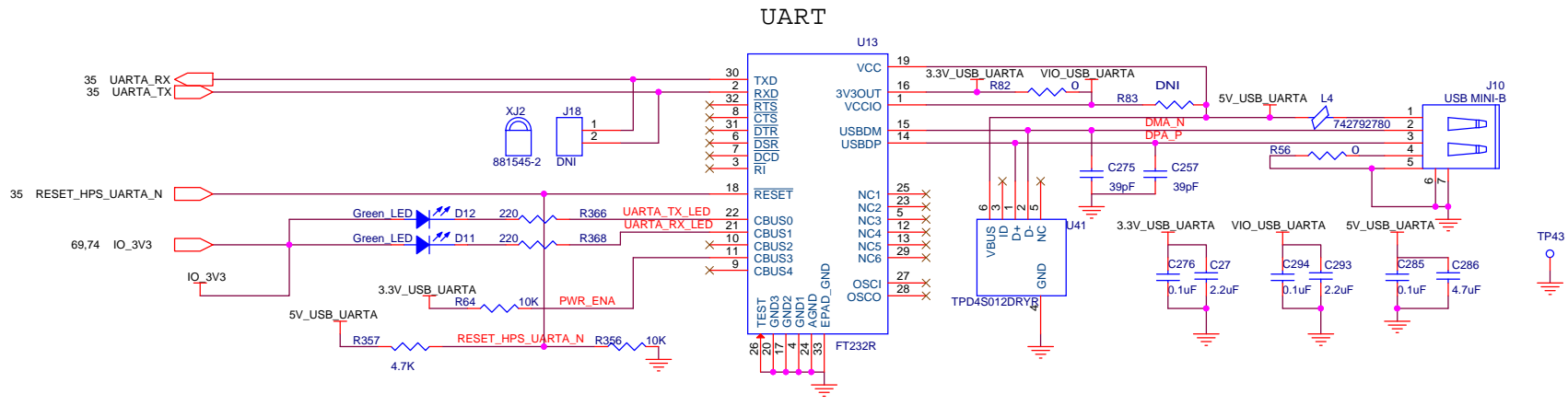
MAX USB



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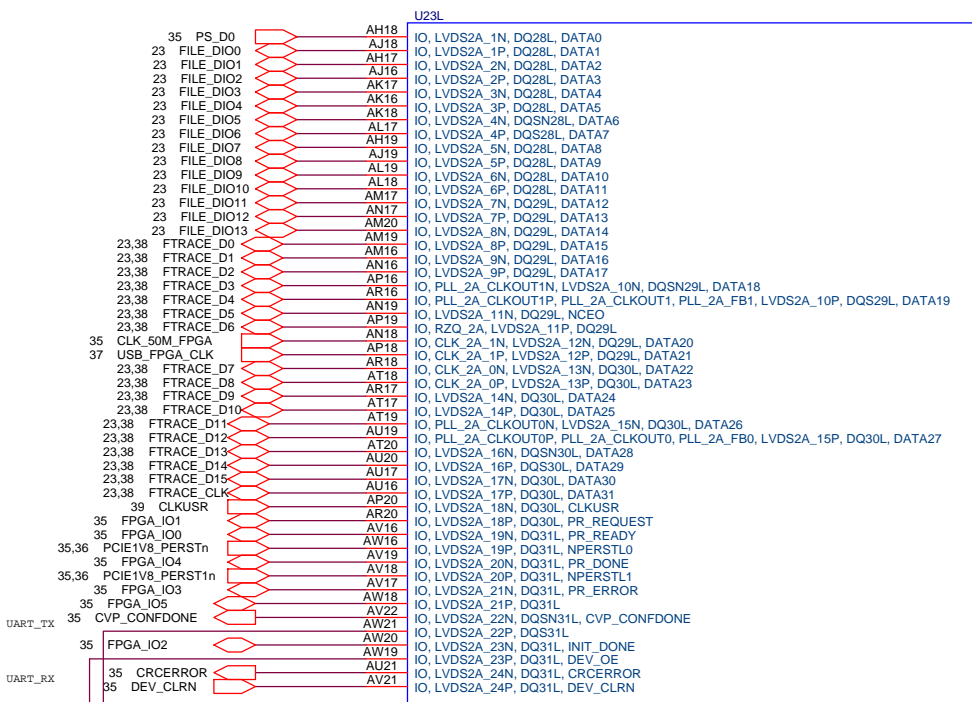


# UART to USB PORT

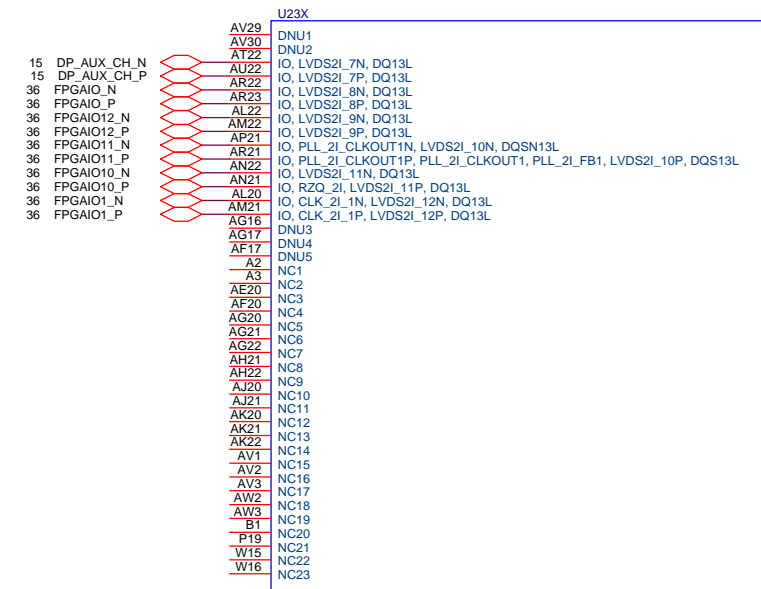


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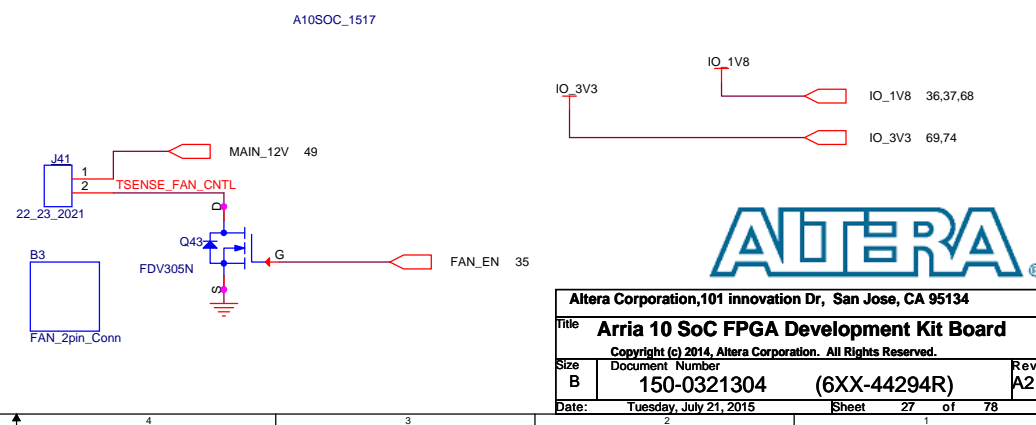
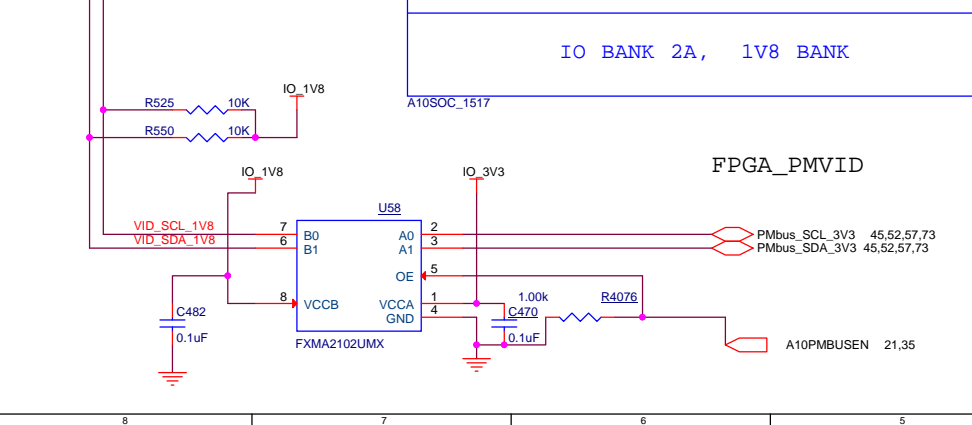
# FPBA 1.8V IOs for File Flash and Debug port



IO BANK 2A, 1V8 BANK

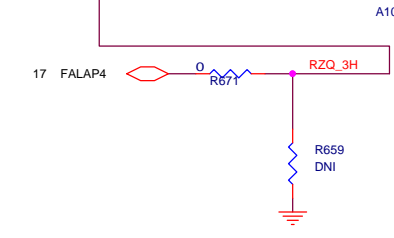
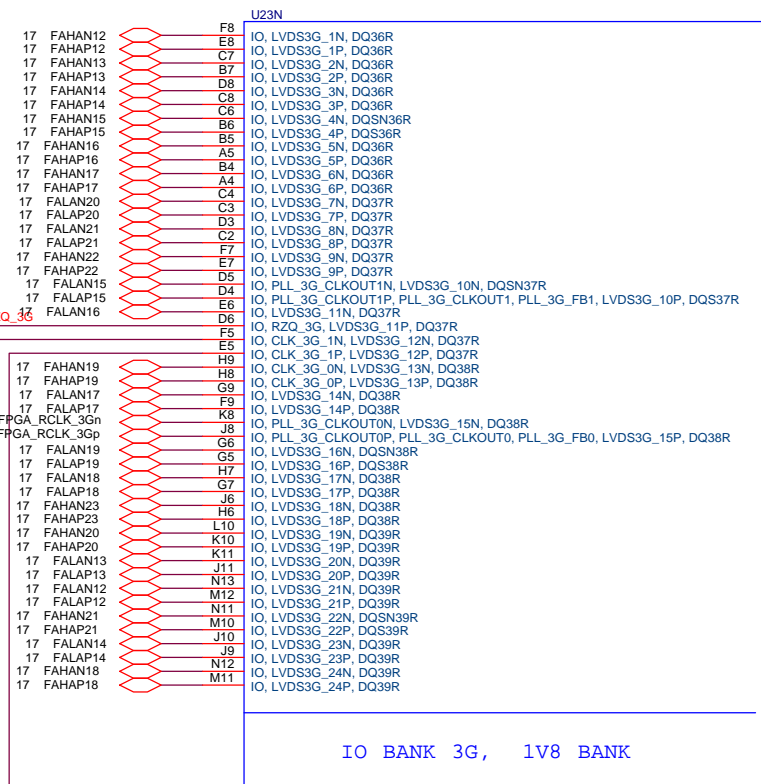
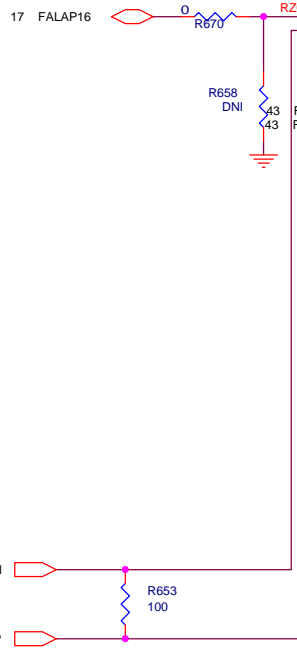


2I IO BANK, 1V8 BANK



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# FPGA IOs for LVDS links of FMC A Port

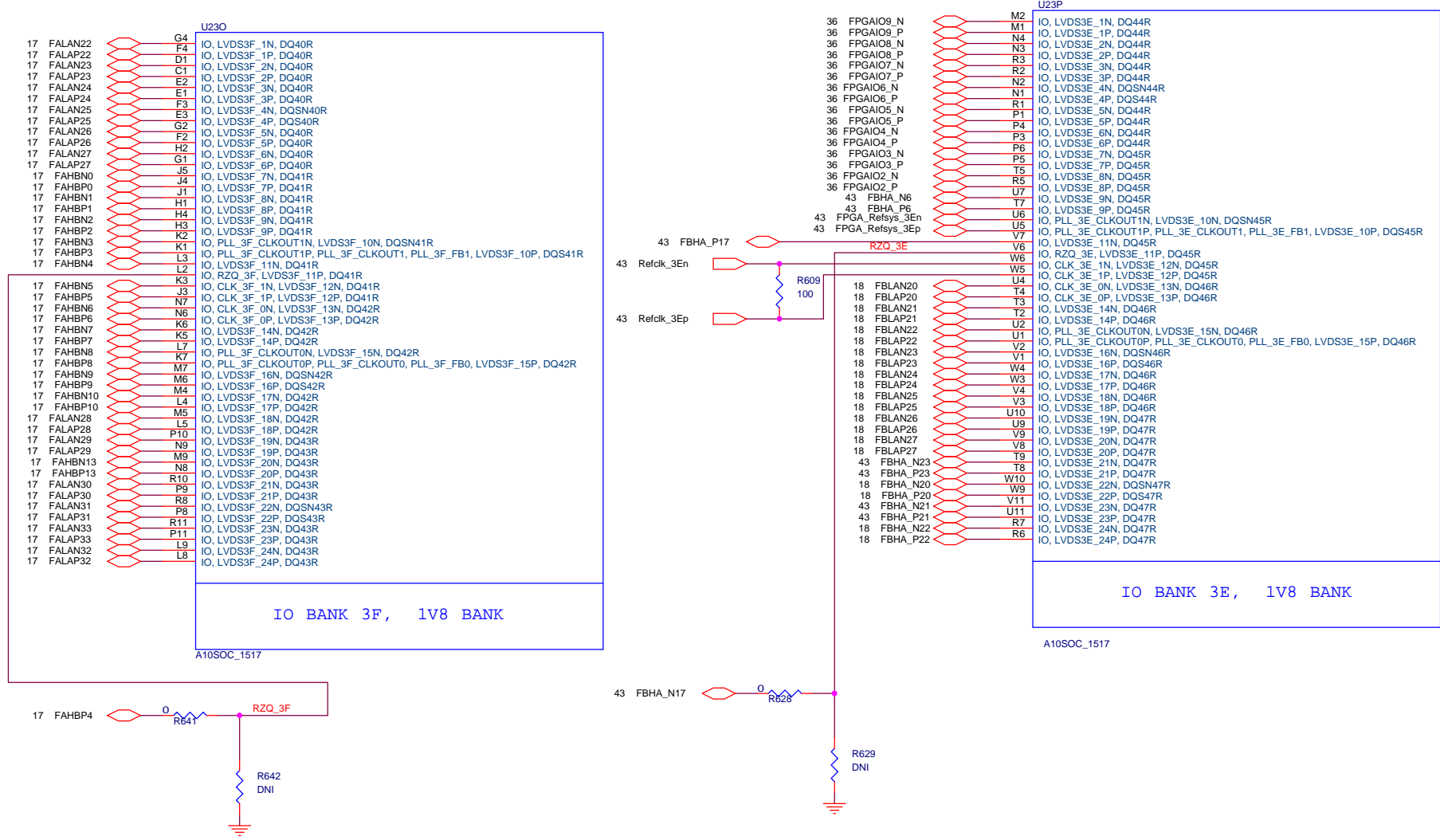


A10SOC\_1517



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# FPGA IOs for LVDS links of FMC A Port and FMC B Port



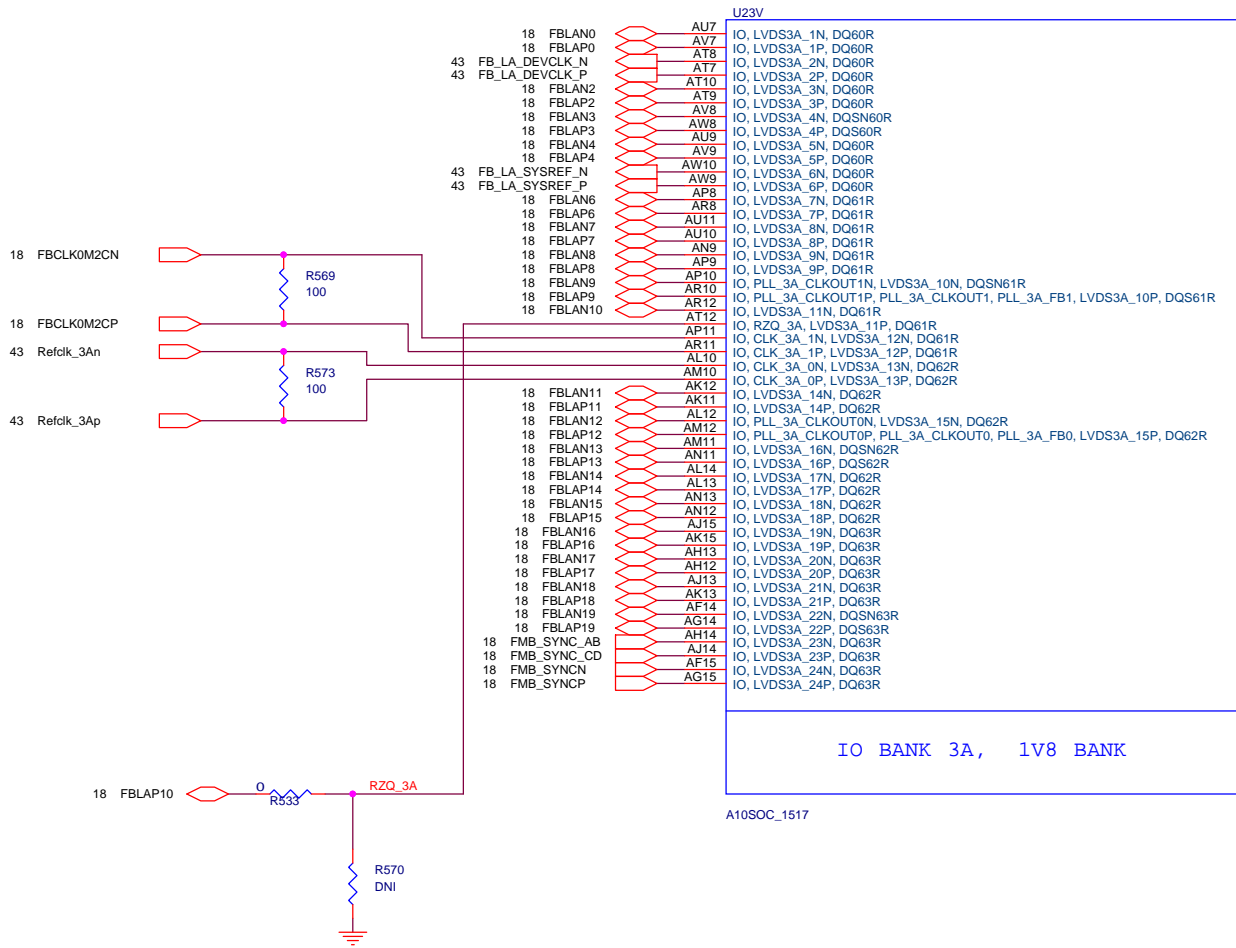
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# FPGA IOs for LVDS links of FMC B Port



IO BANK 3A, 1V8 BANK



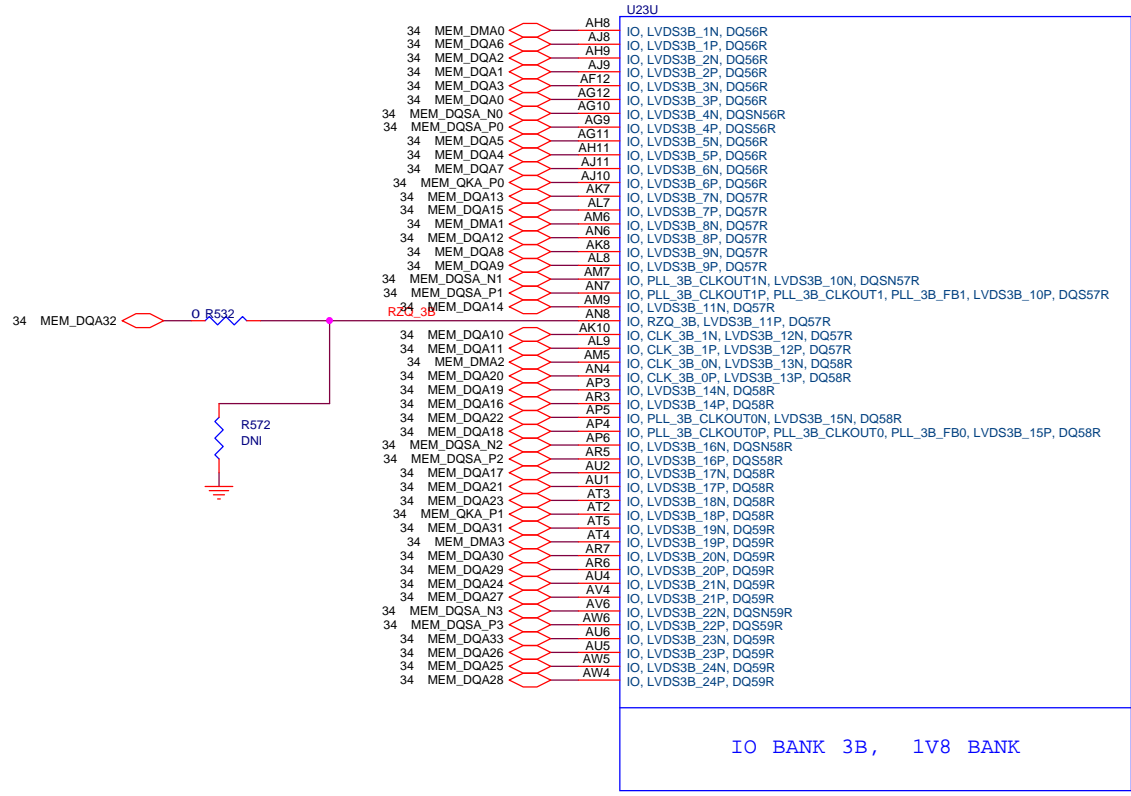
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# FPGA IOs for FPGA Memory Interface



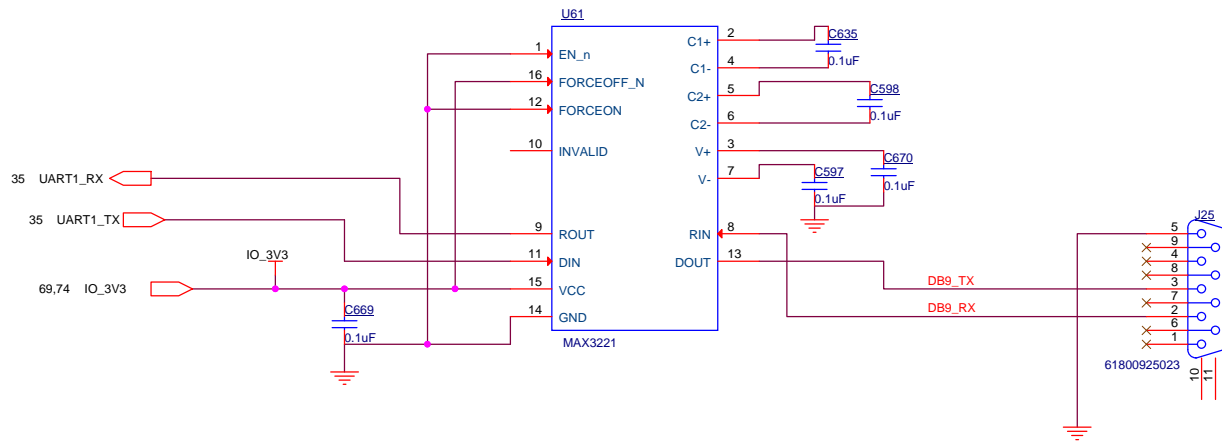
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# FPGA IOs for FPGA Memory Interface



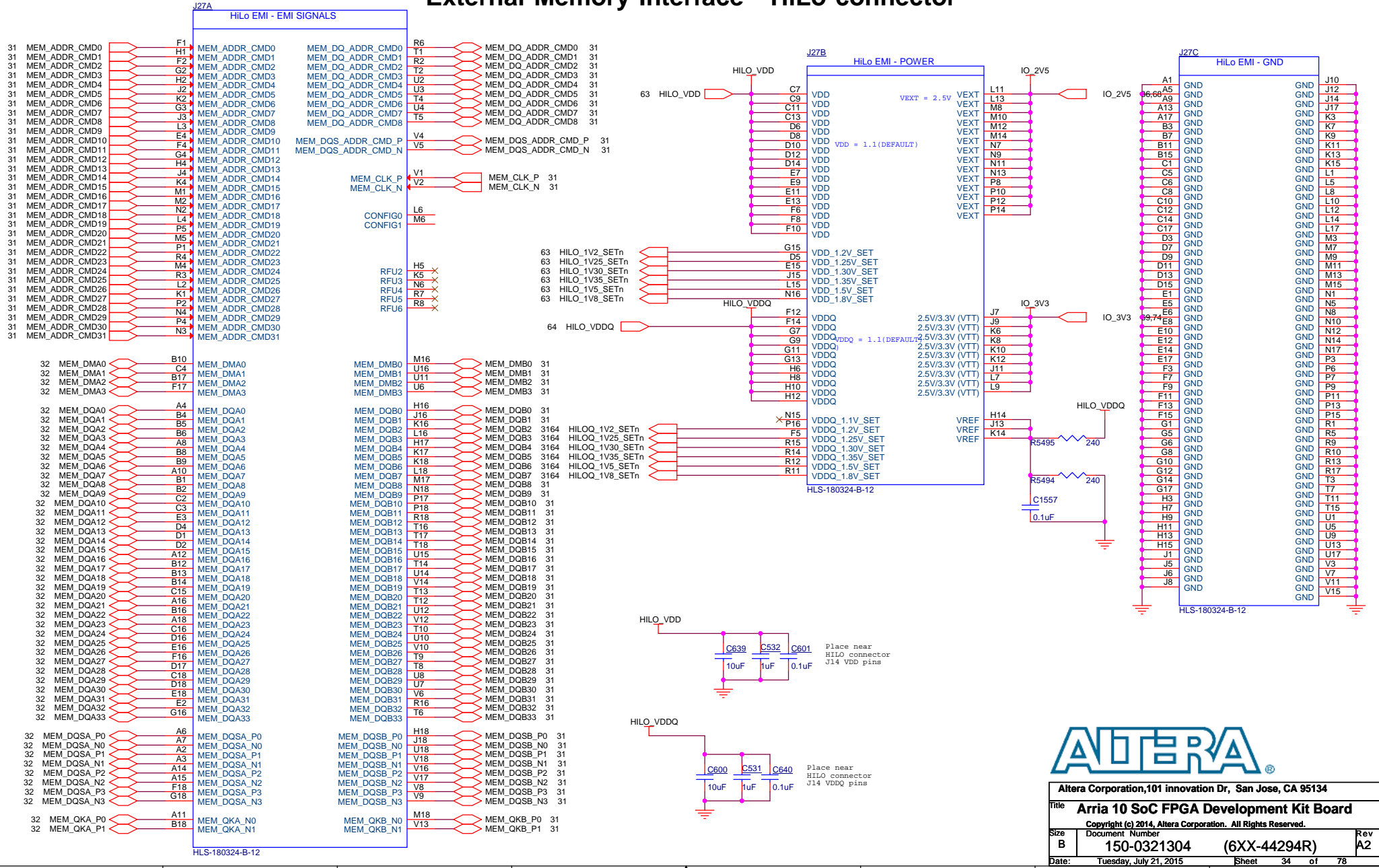
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# UART Port B



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# External Memory Interface - HiLo connector





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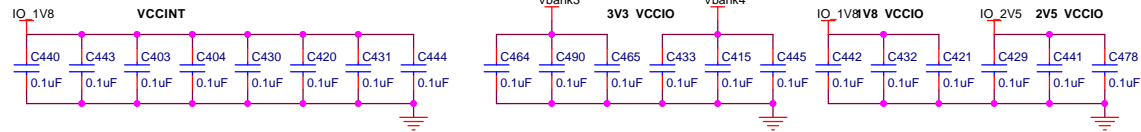
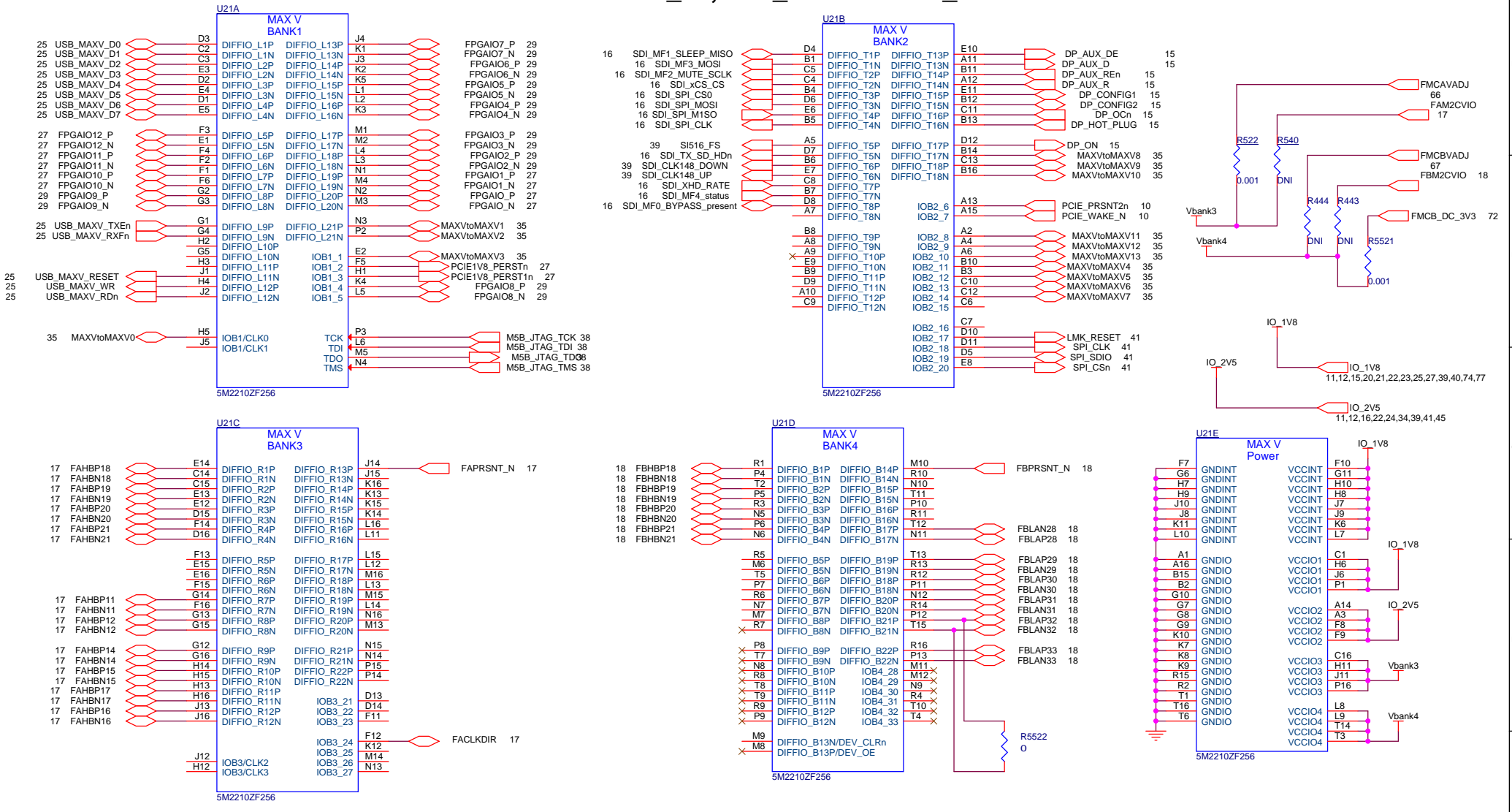
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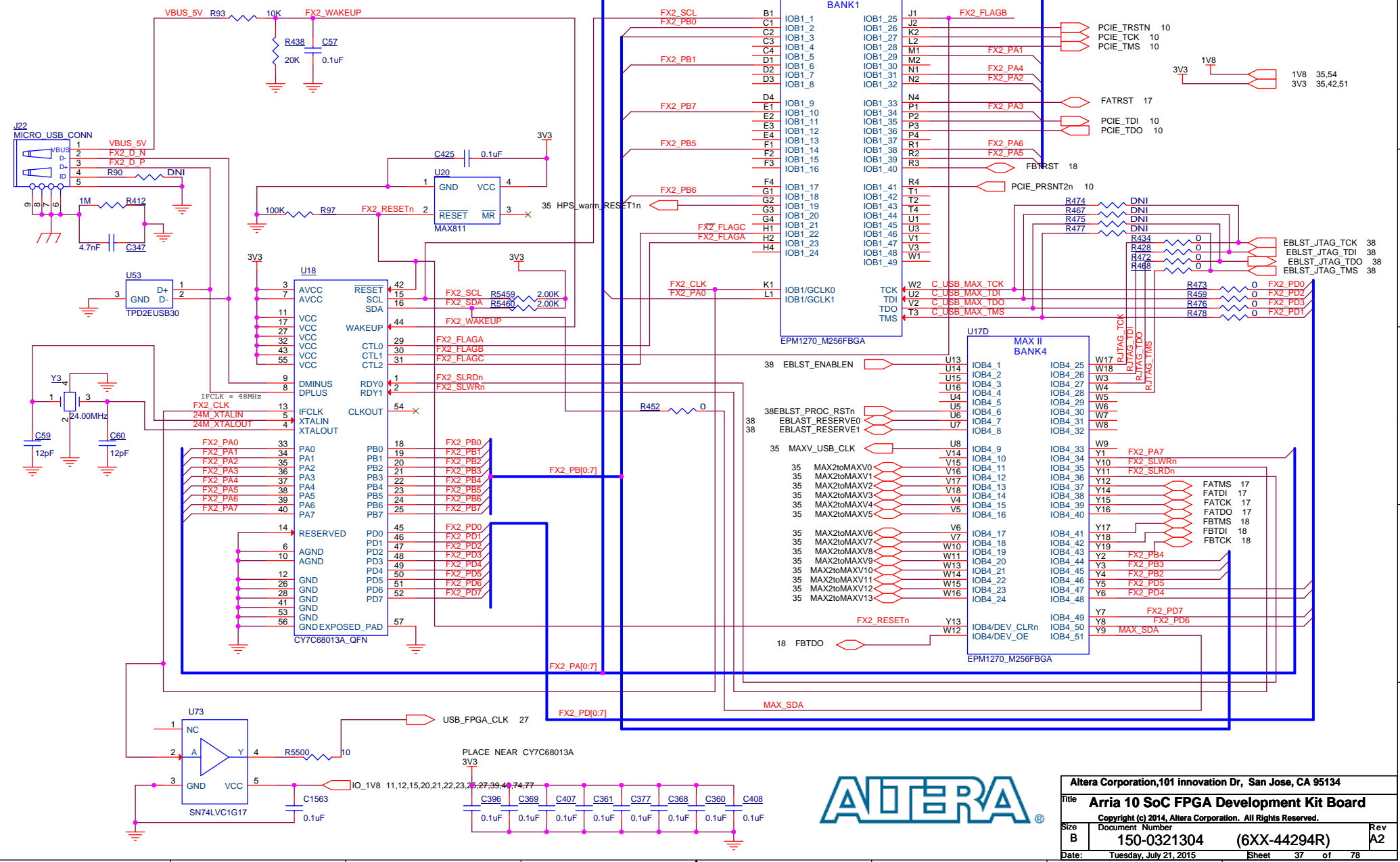


# FPGAIO for DP\_IO, SDI\_IO and FMC\_3V3IO



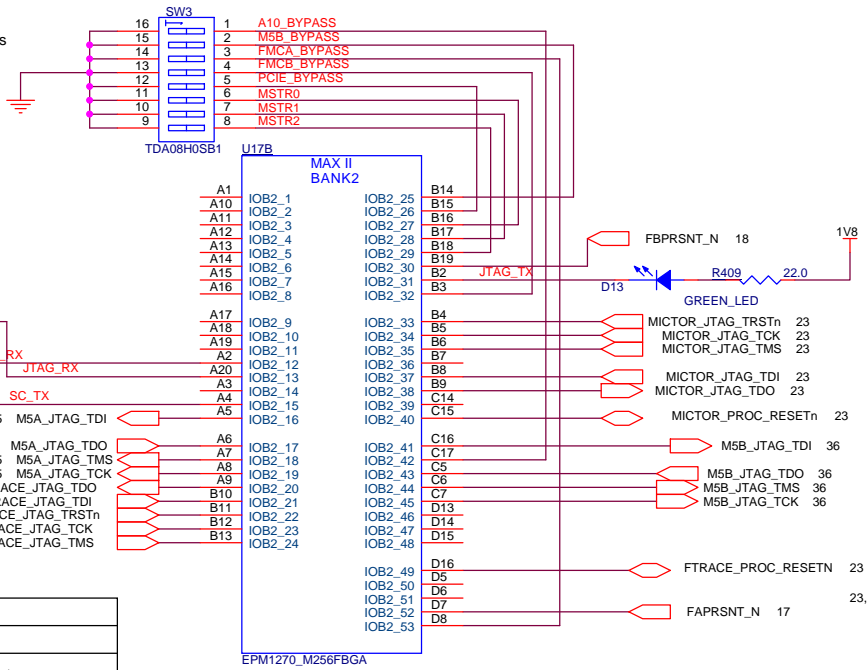
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# On-Board USB Blaster II - Part 1

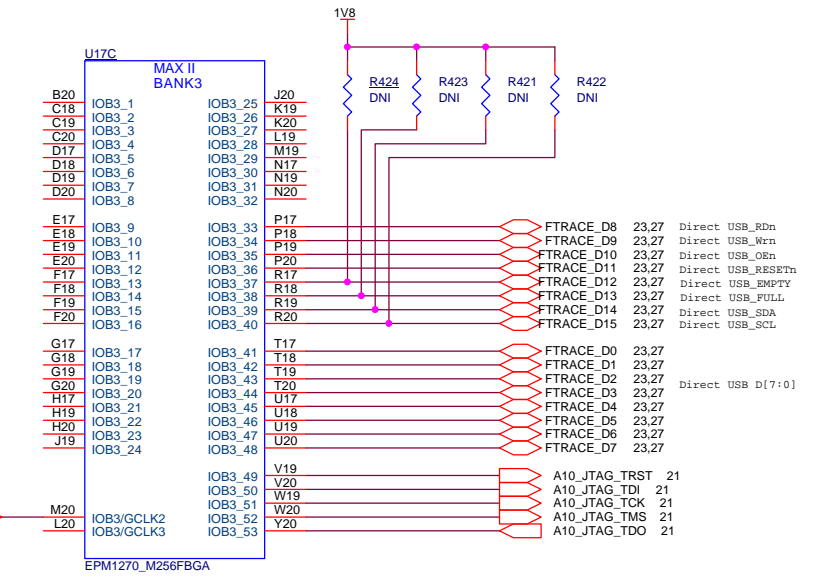


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Logic 0 = Device JTAG Bypass  
 Logic 1 = Device JTAG Enable



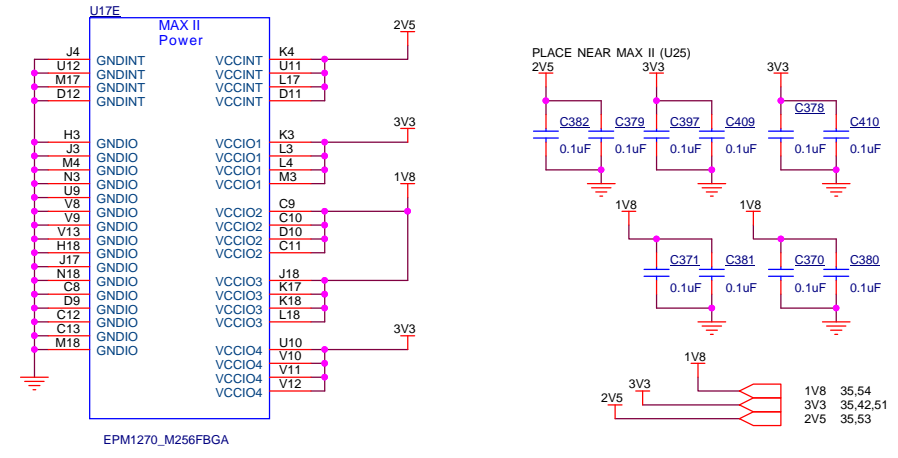
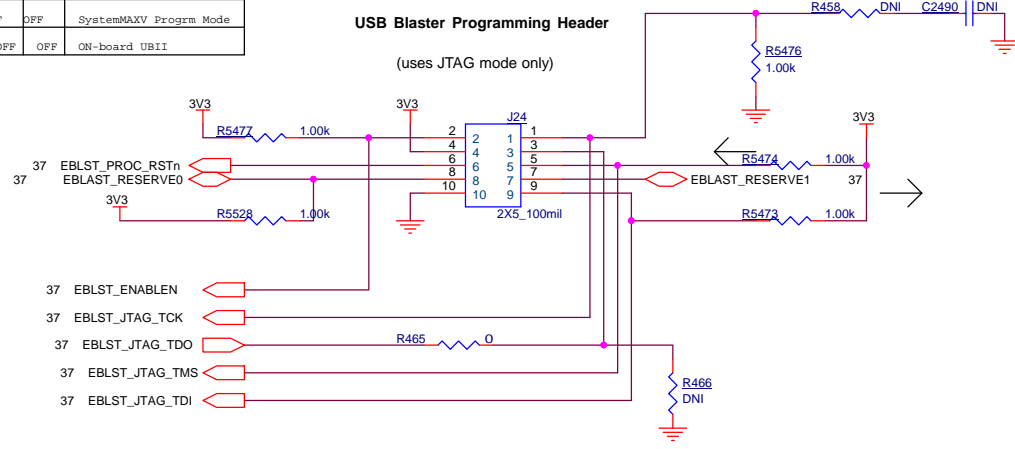
# On-Board USB Blaster II - Part 2



MSTR2	MSTR1	MSTR0	Mode
ON	ON	ON	BOOT
OFF	ON	ON	FMCA Master
ON	OFF	ON	FMCB Master
OFF	OFF	ON	Reserved
ON	ON	OFF	FTRACE Master
OFF	ON	OFF	GUI Test
ON	OFF	OFF	SystemMAXV Prog Mode
OFF	OFF	OFF	On-board UBII

## USB Blaster Programming Header

(uses JTAG mode only)



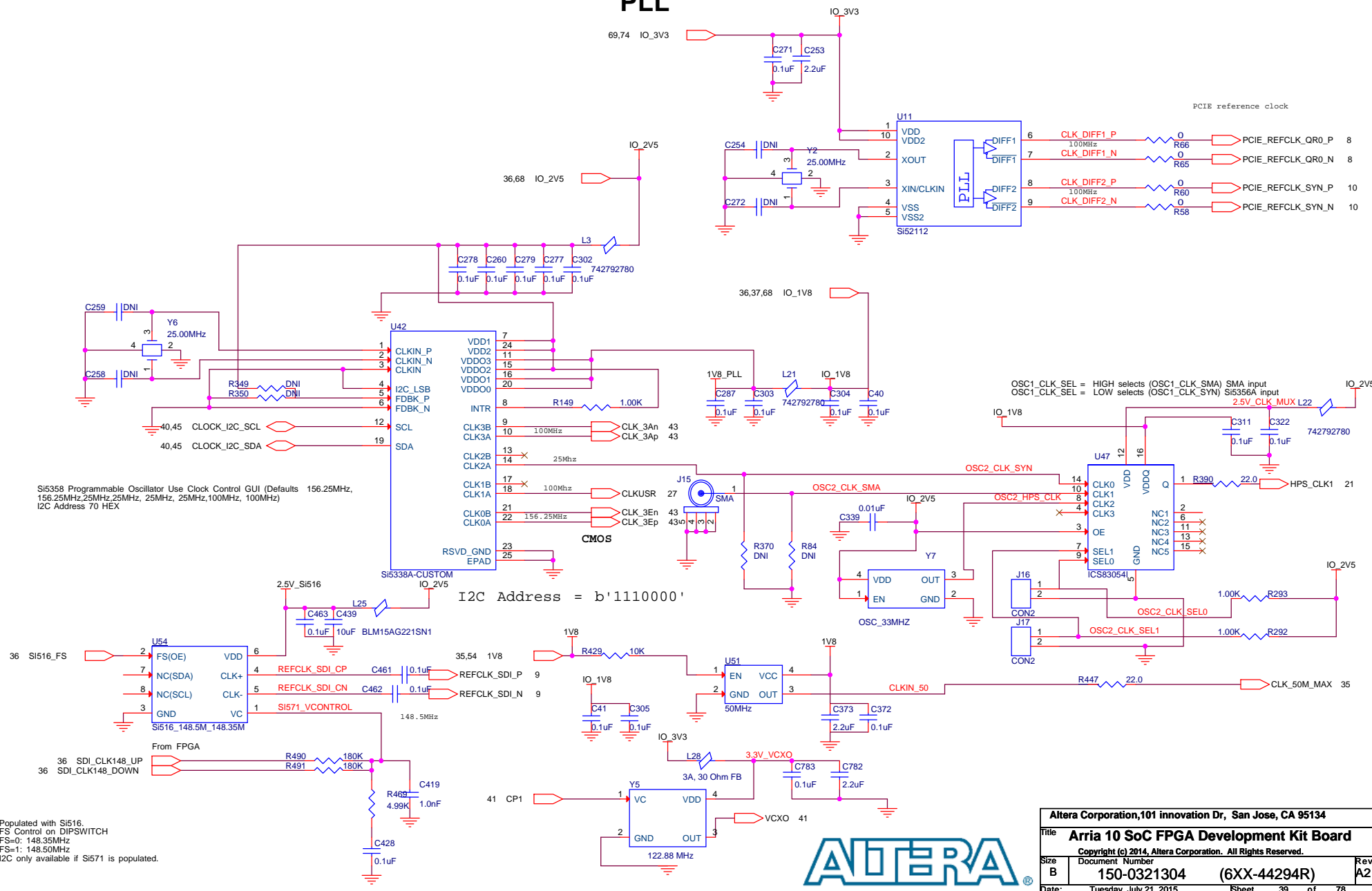
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# PLL



Si5358 Programmable Oscillator Use Clock Control GUI (Defaults 156.25MHz, 156.25MHz, 25MHz, 25MHz, 25MHz, 25MHz, 100MHz, 100MHz) I2C Address 70 HEX

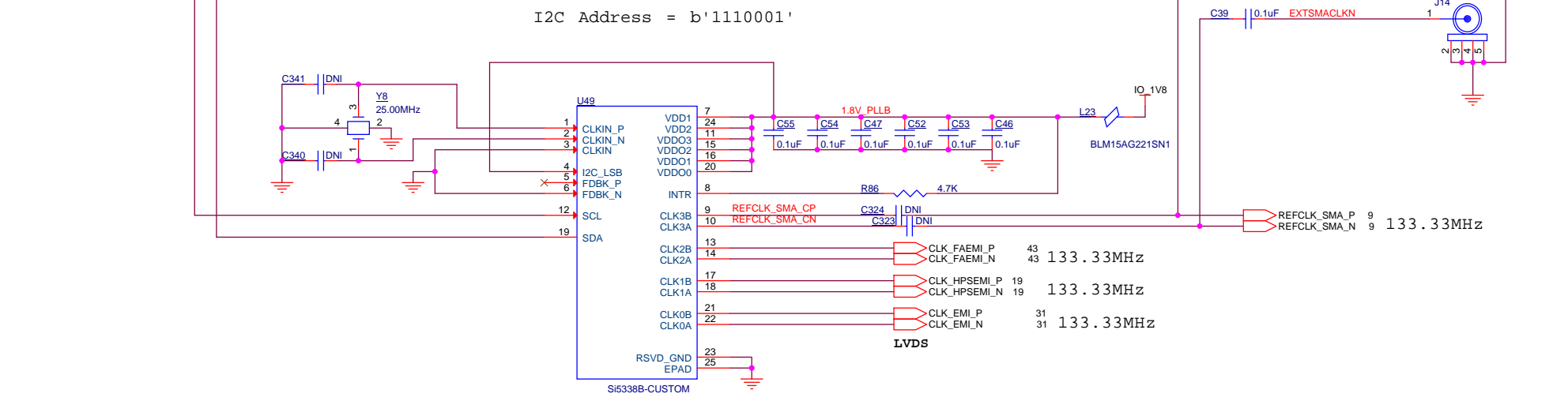
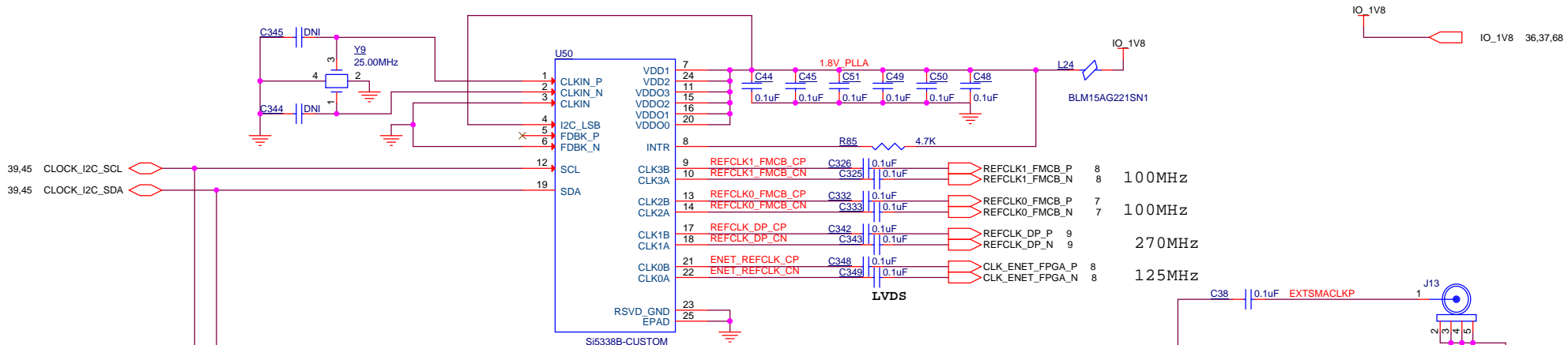
I2C Address = b'1110000'

Populated with Si516.  
FS Control on DIPSWITCH  
FS=0: 148.35MHz  
FS=1: 148.50MHz  
I2C only available if Si571 is populated.

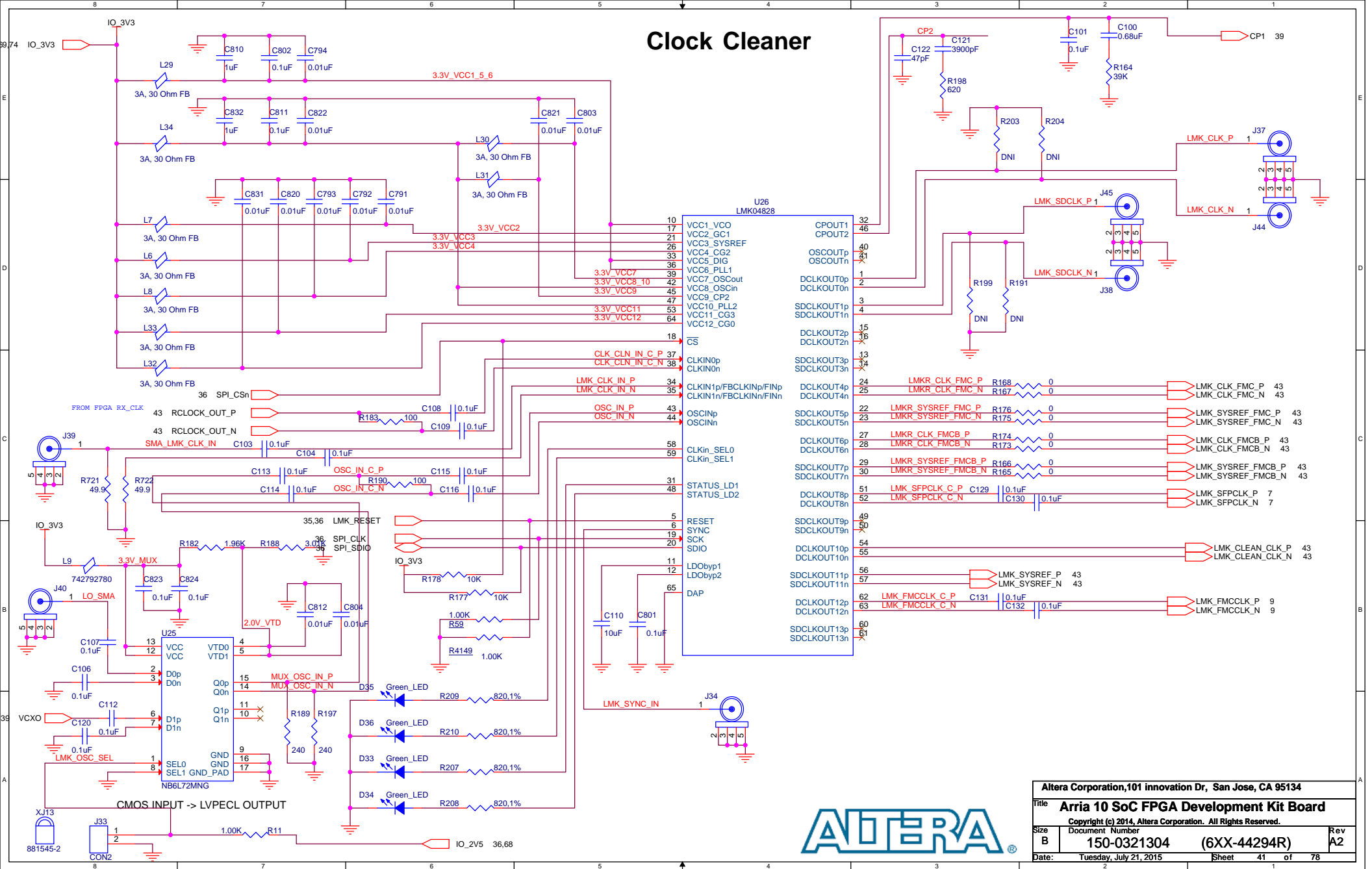
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# PLL (2)



# Clock Cleaner



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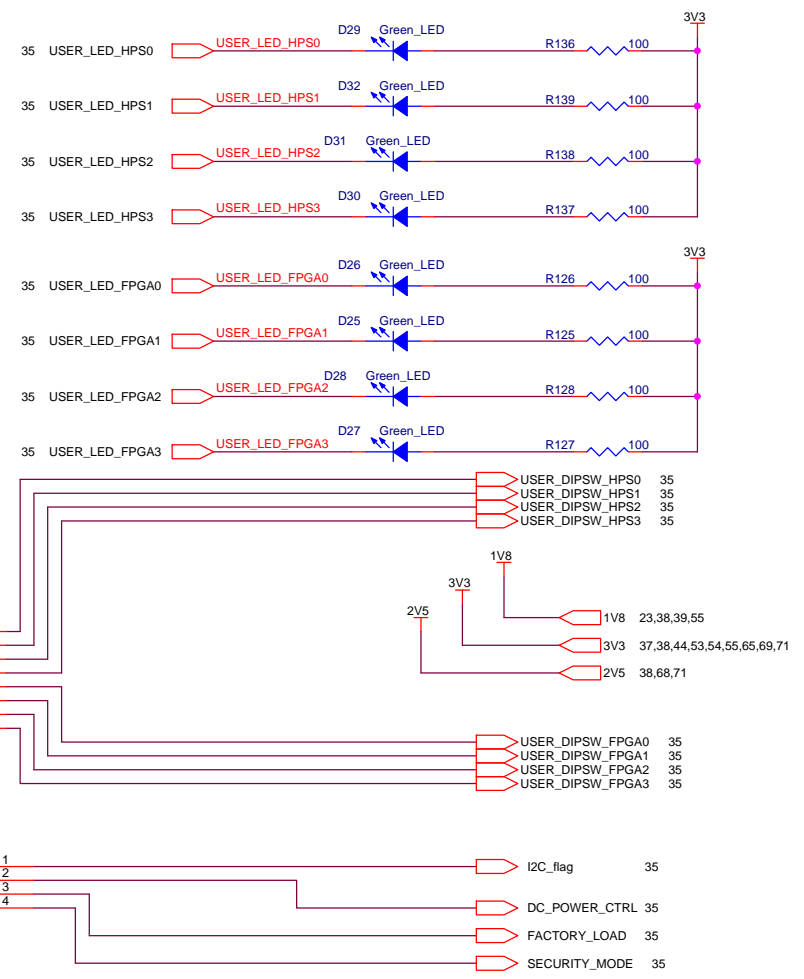
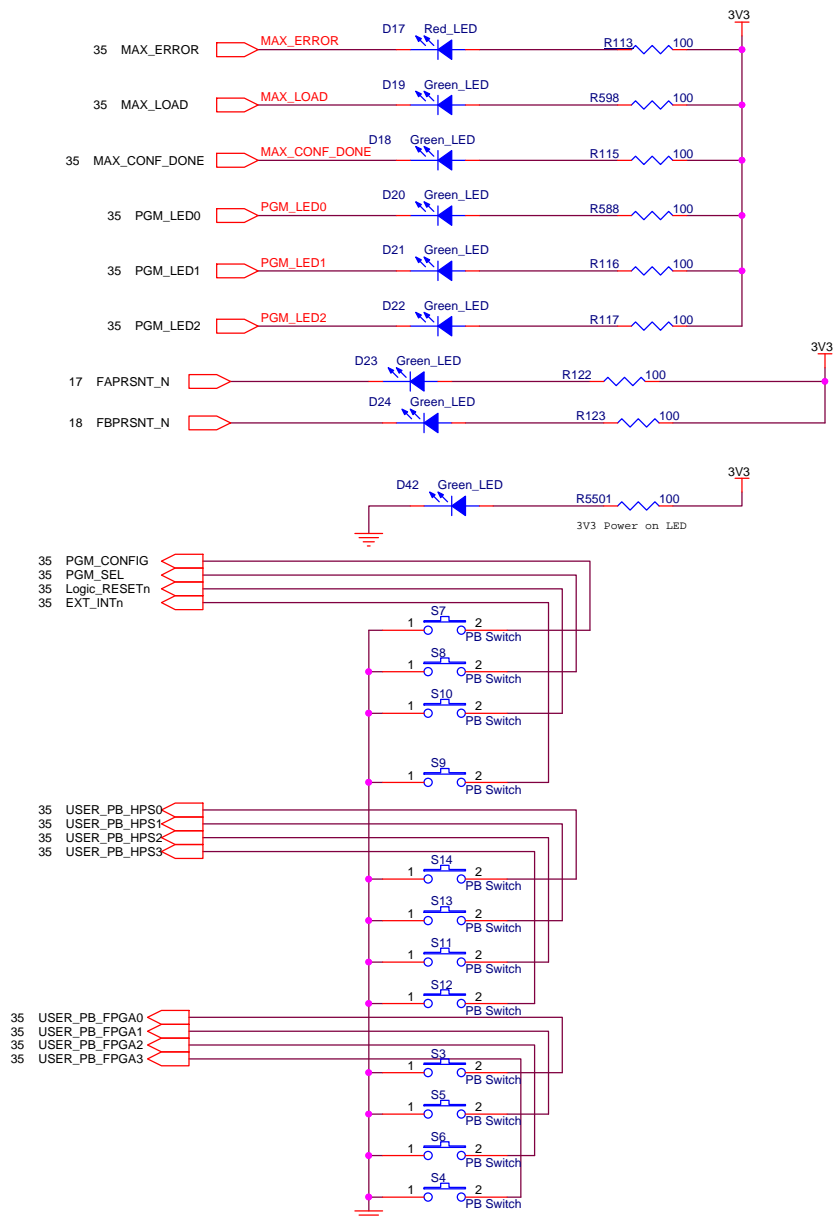
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# User I/O



REVA	SW1	Bit Definition
Bit1		I2C_flag
Bit2		Factory_load
Bit3		MSLE1
Bit4		MSLE0



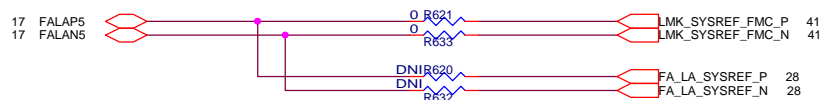
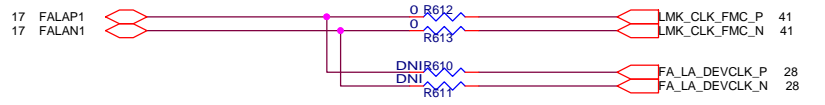
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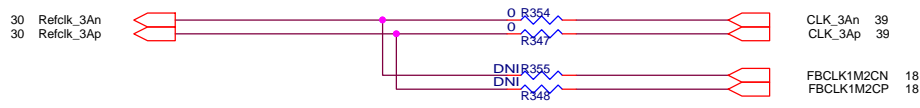
# Clock Resistor Mux



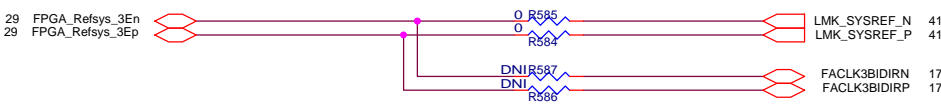
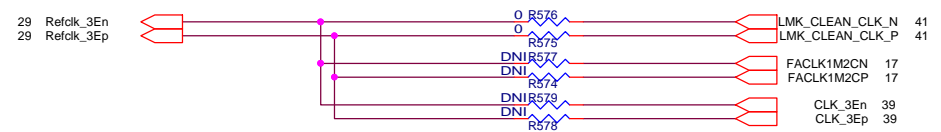
## FMC A Clock MUX for TI ADC FMC card



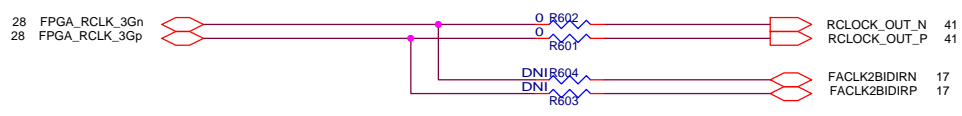
## FMC B Clock MUX for TI ADC FMC card



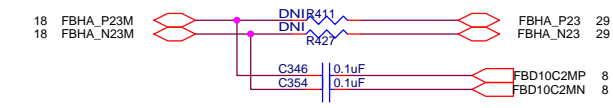
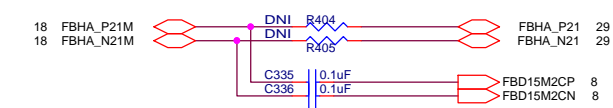
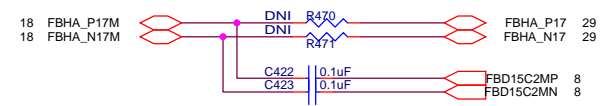
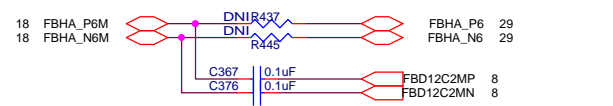
## Clock MUX for 3A Bank reference clock



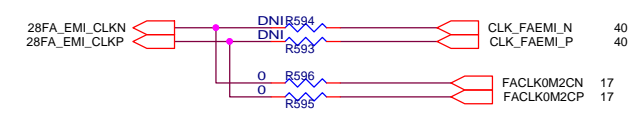
## Clock MUX for 3E Bank reference clock



## Clock MUX for 3G Bank reference clock



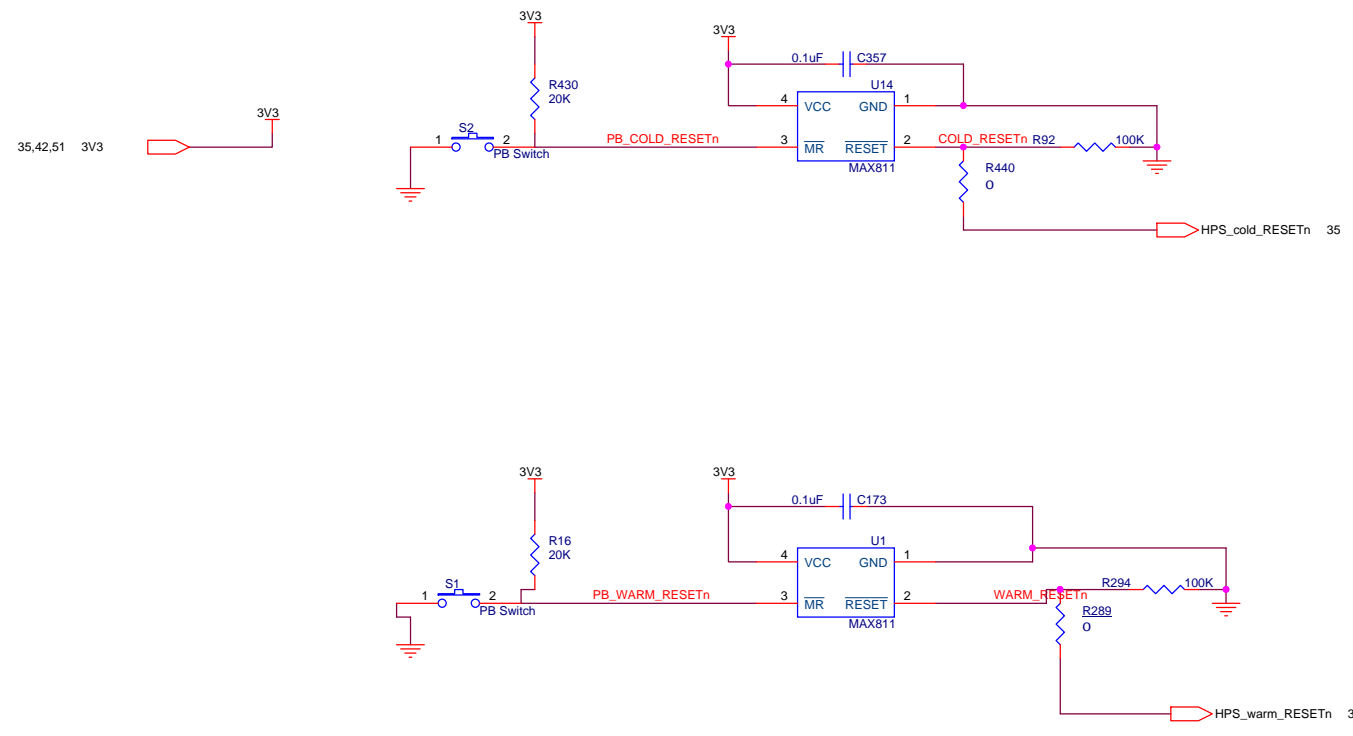
## MUX for supporting Altera FMC spec



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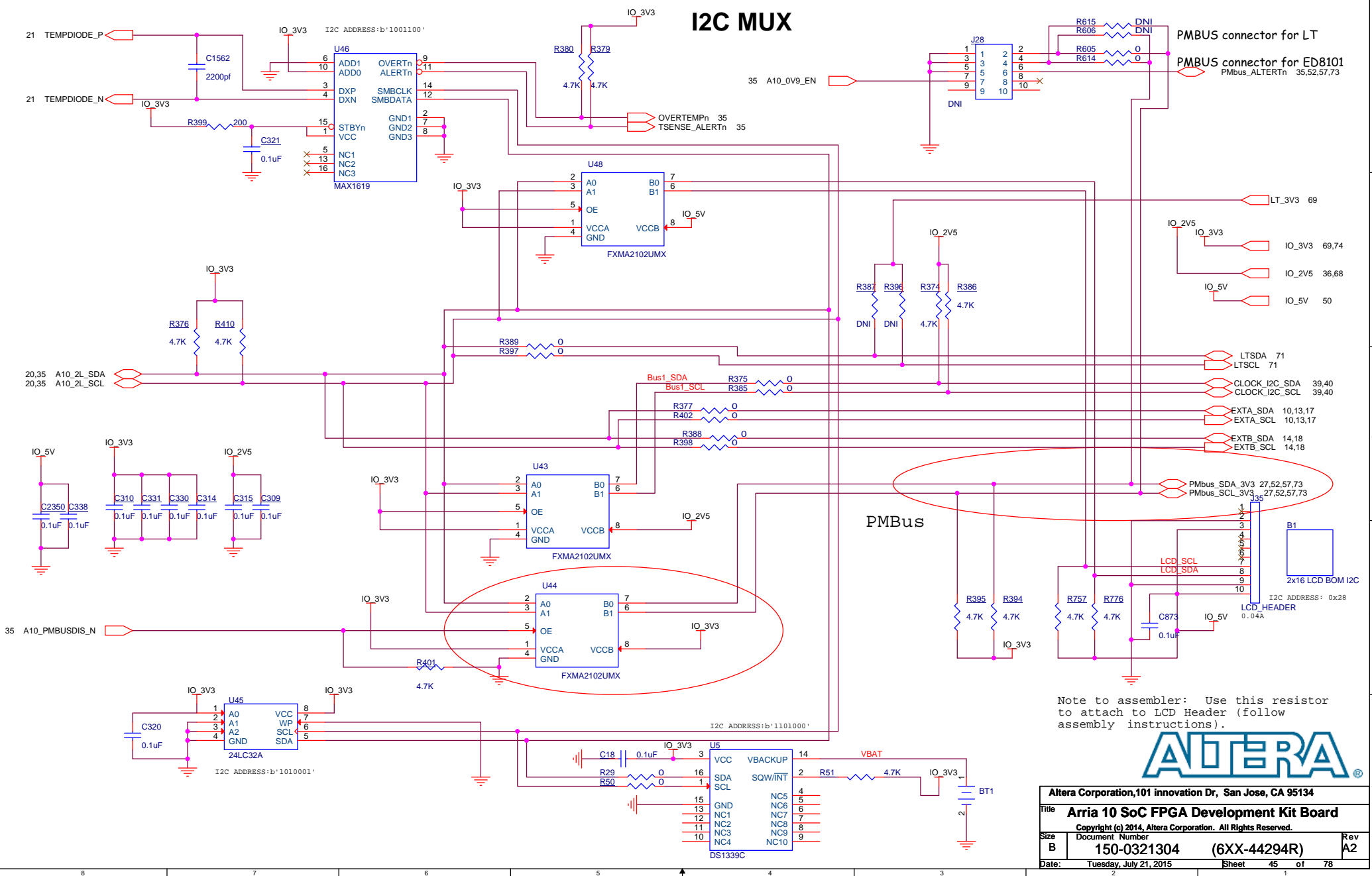
# Reset Circuit

## RESET CIRCUIT



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# I2C MUX



Note to assembler: Use this resistor to attach to LCD Header (follow assembly instructions).

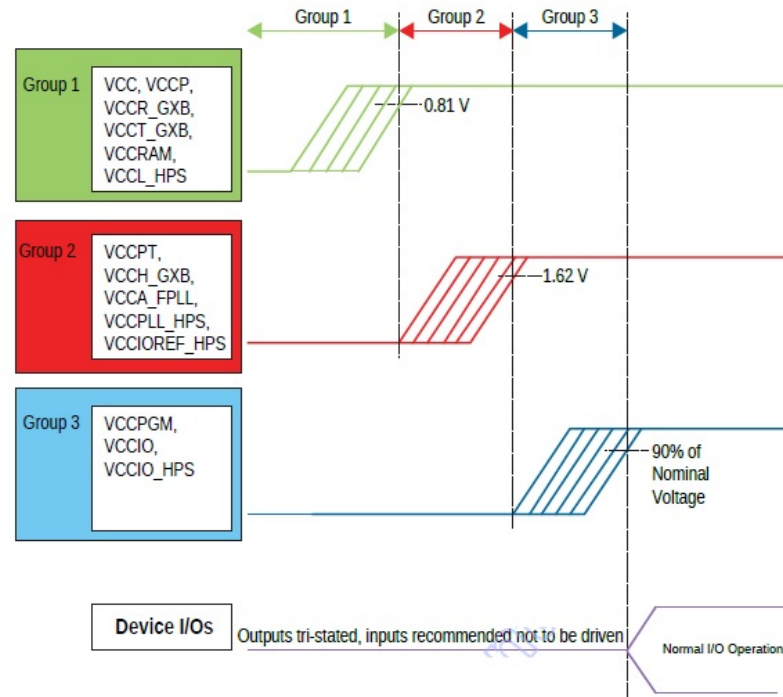


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# A10 SOC Power Sequence

Figure 1: Power-Up Sequence for Arria 10 Devices



1. If the VCC voltage level is different from VCCT\_GXB, VCCR\_GXB, and orVCCRAM, then ramp VCC first followed by VCCT\_GXB, VCCR\_GXB, and VCCRAM (In any order) within group 1
2. All Power rails must ramp completely to full rail voltage within the Tramp (0.2ms to 4ms)
- 3.VCCBAT (1.2-1.8V) can be powered up/down at any time and is not shown in the power sequence
- 4.The Power down sequence is the reverse of the power up sequence



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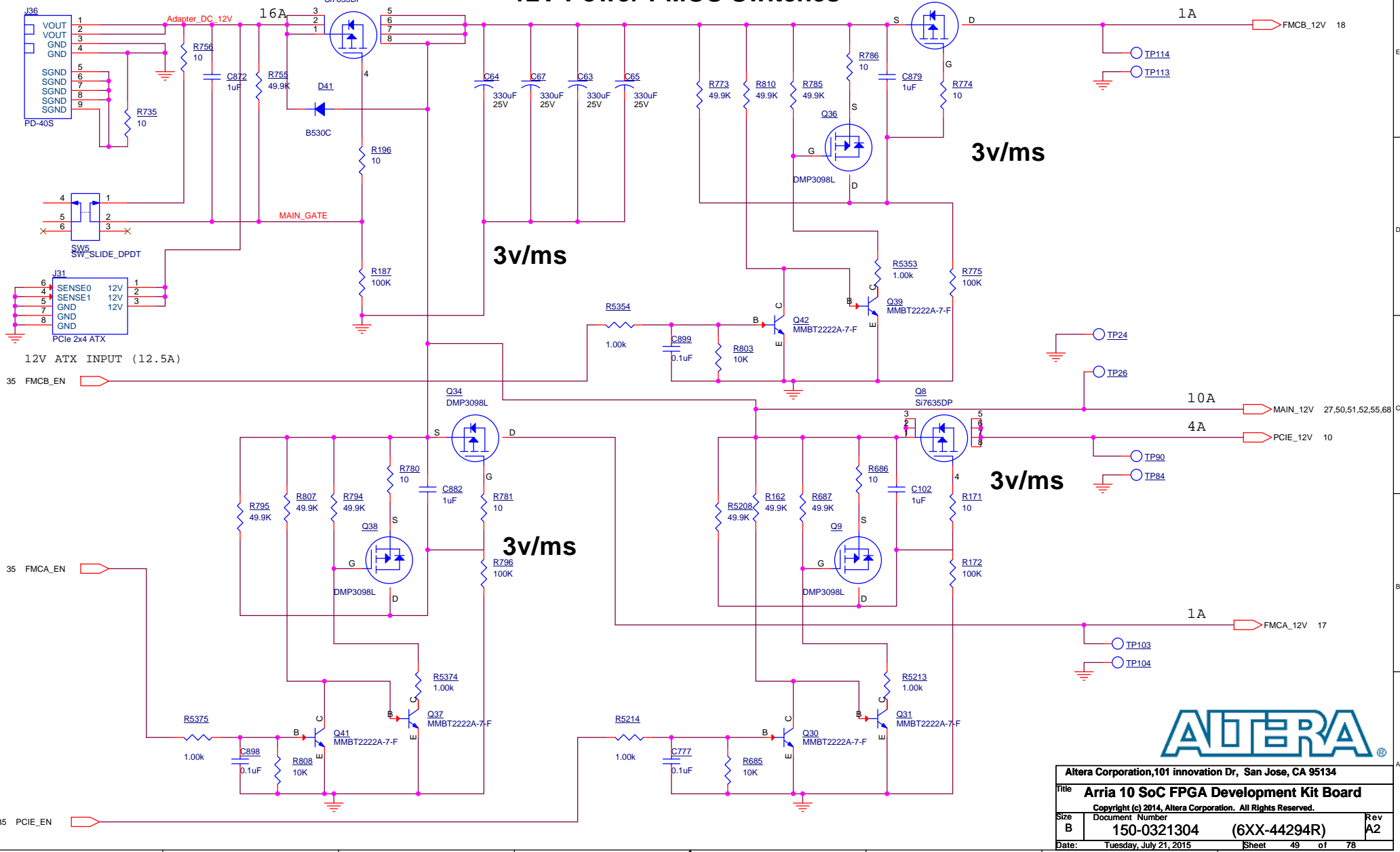
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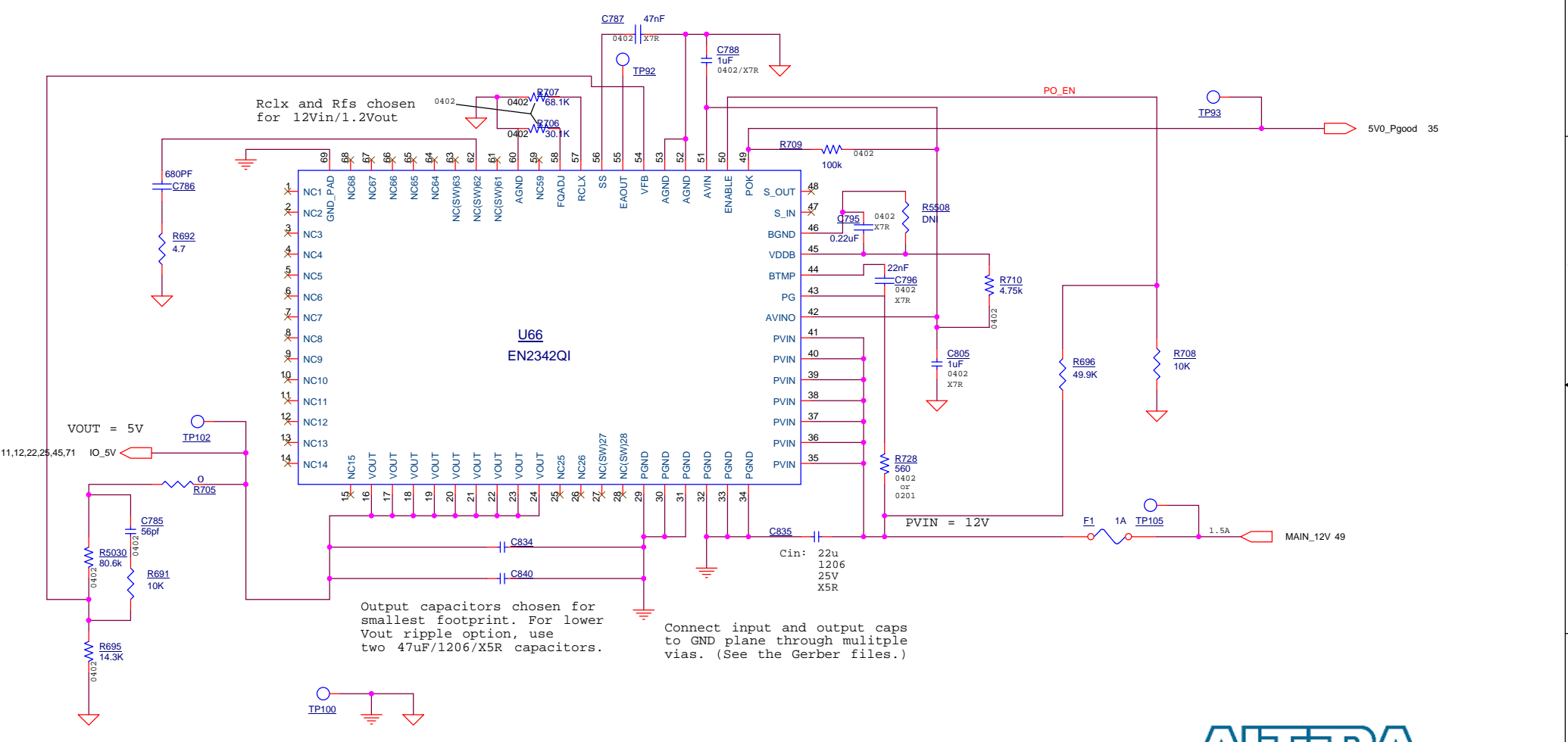
Input connector for  
200 Watt AC/DC Adapter

# 12V Power PMOS Switches



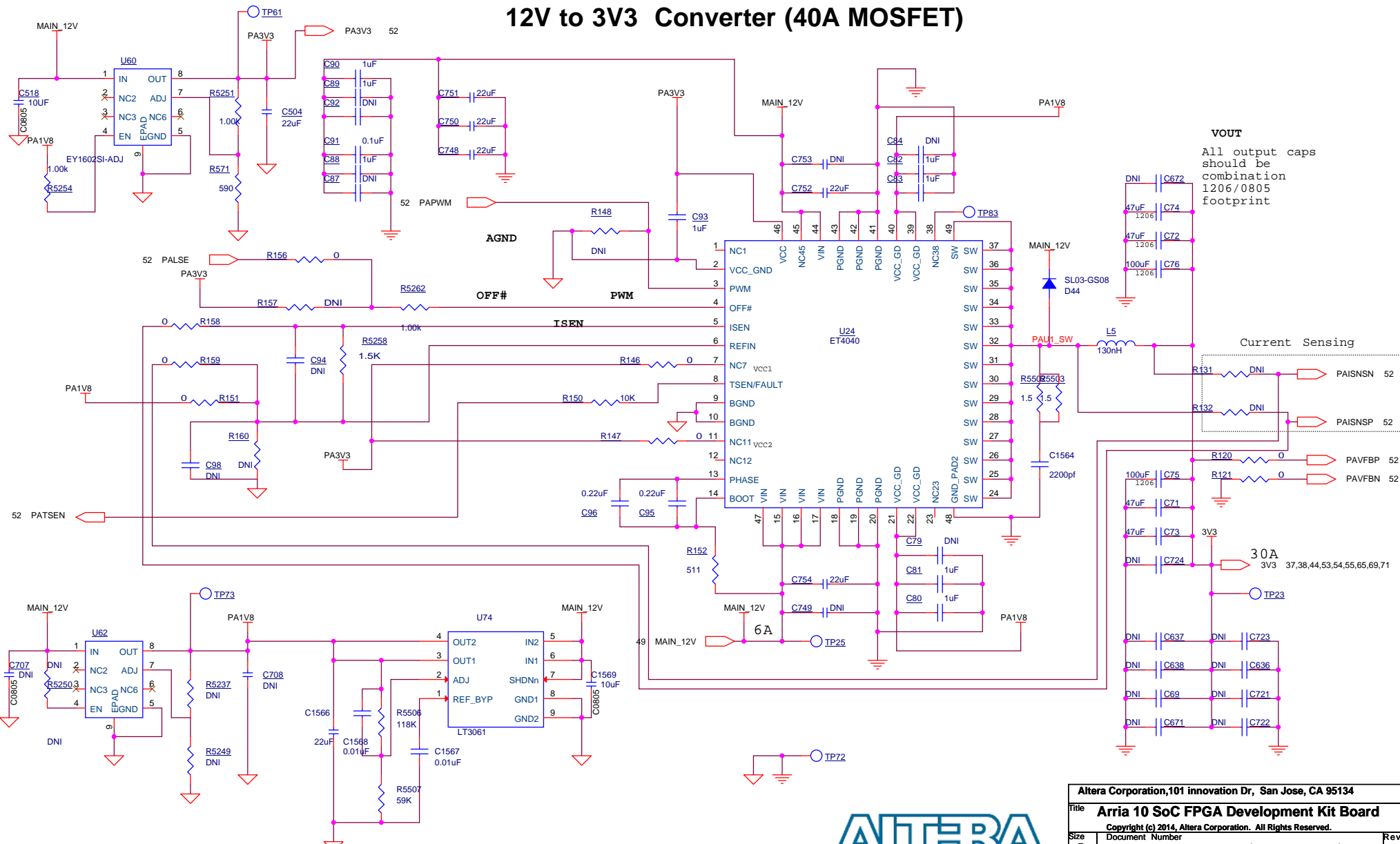
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# 12V to 5V Converter



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# 12V to 3V3 Converter (40A MOSFET)



**VOUT**  
 All output caps should be combination 1206/0805 footprint

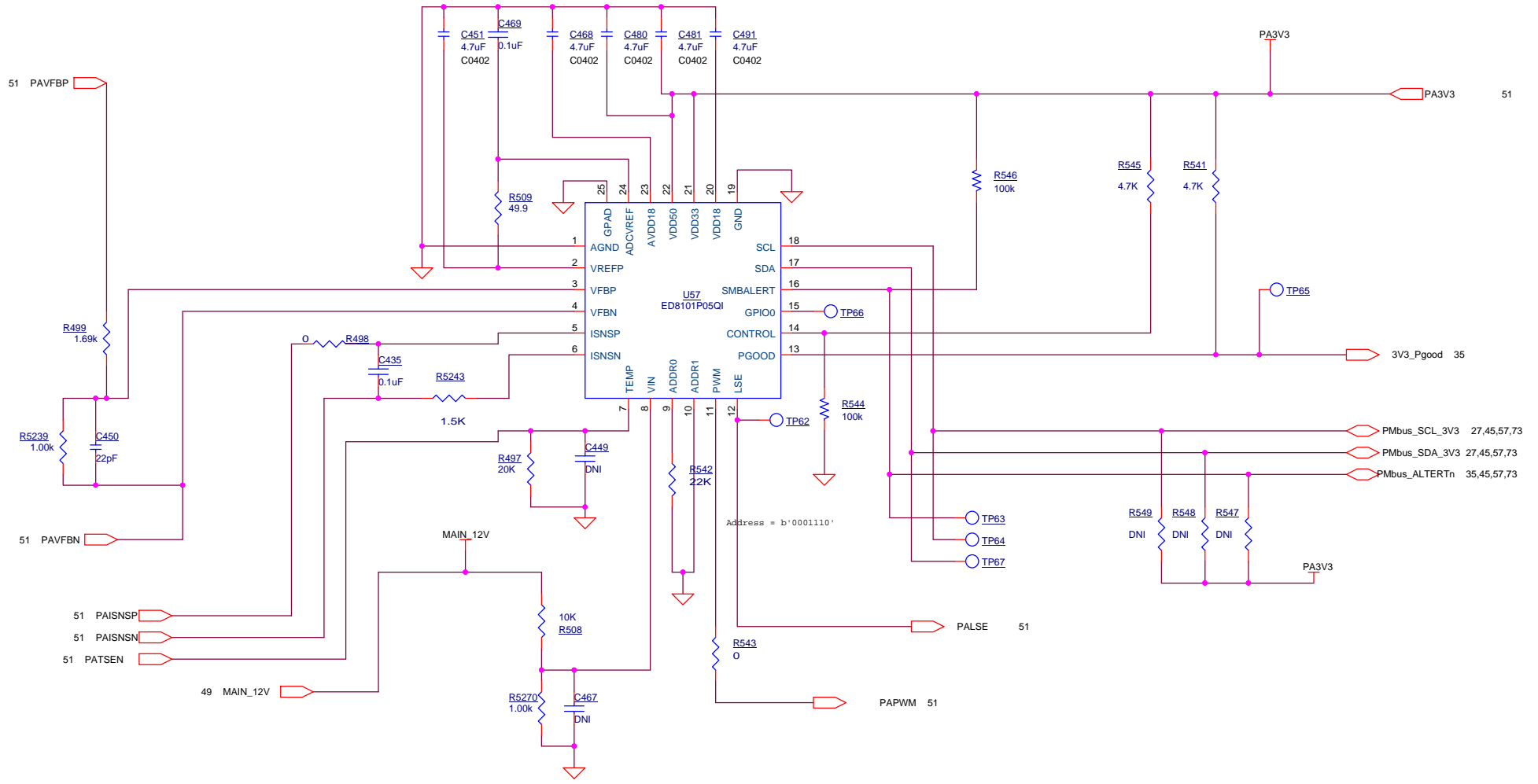
**Current Sensing**  
 PAISNSN 52  
 PAISNSP 52

**30A**  
 3V3 37,38,44,53,54,55,65,69,71

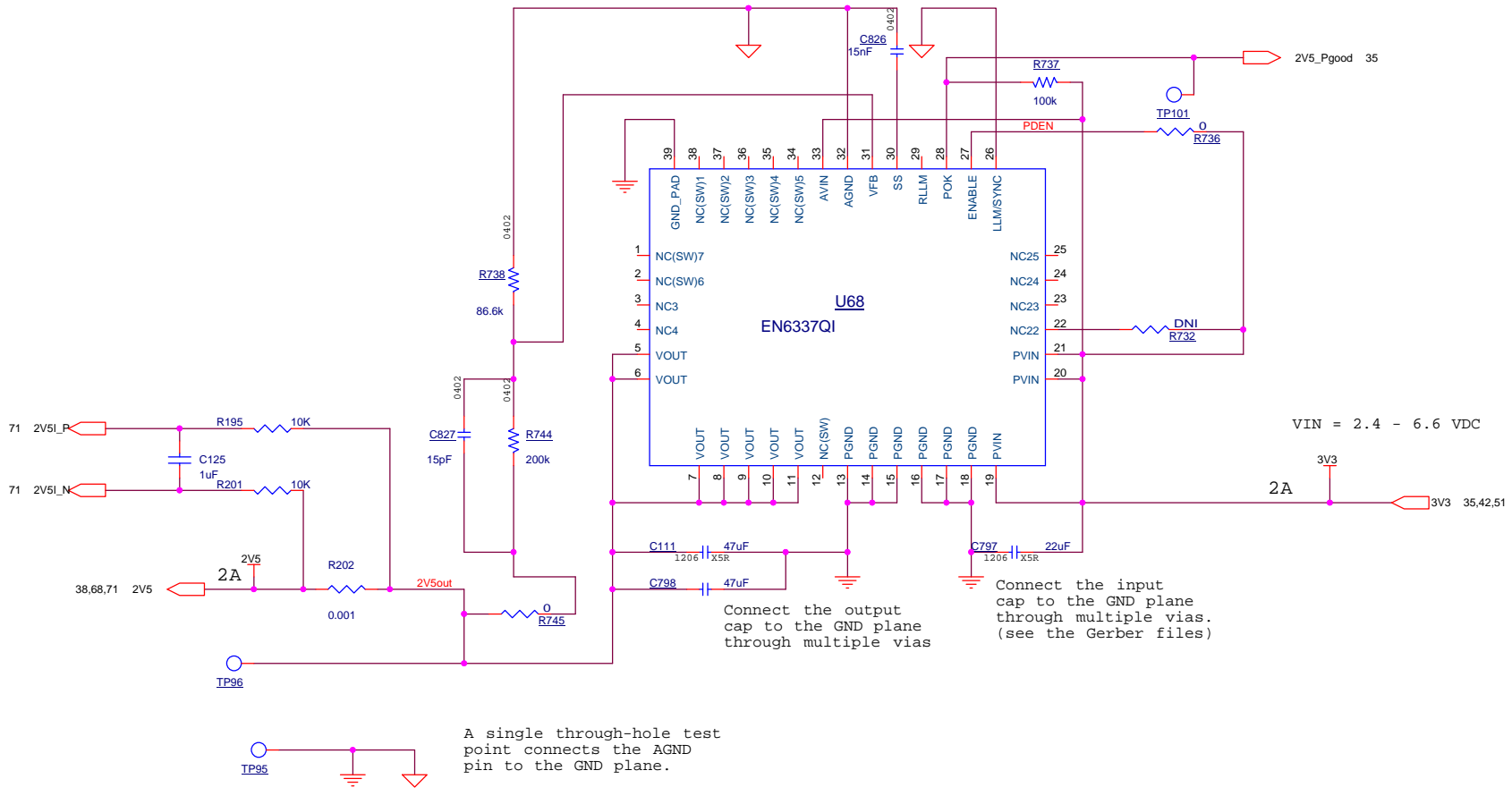
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# 12V to 3V3 Converter (Controller)



# 3V3 to 2V5 Converter

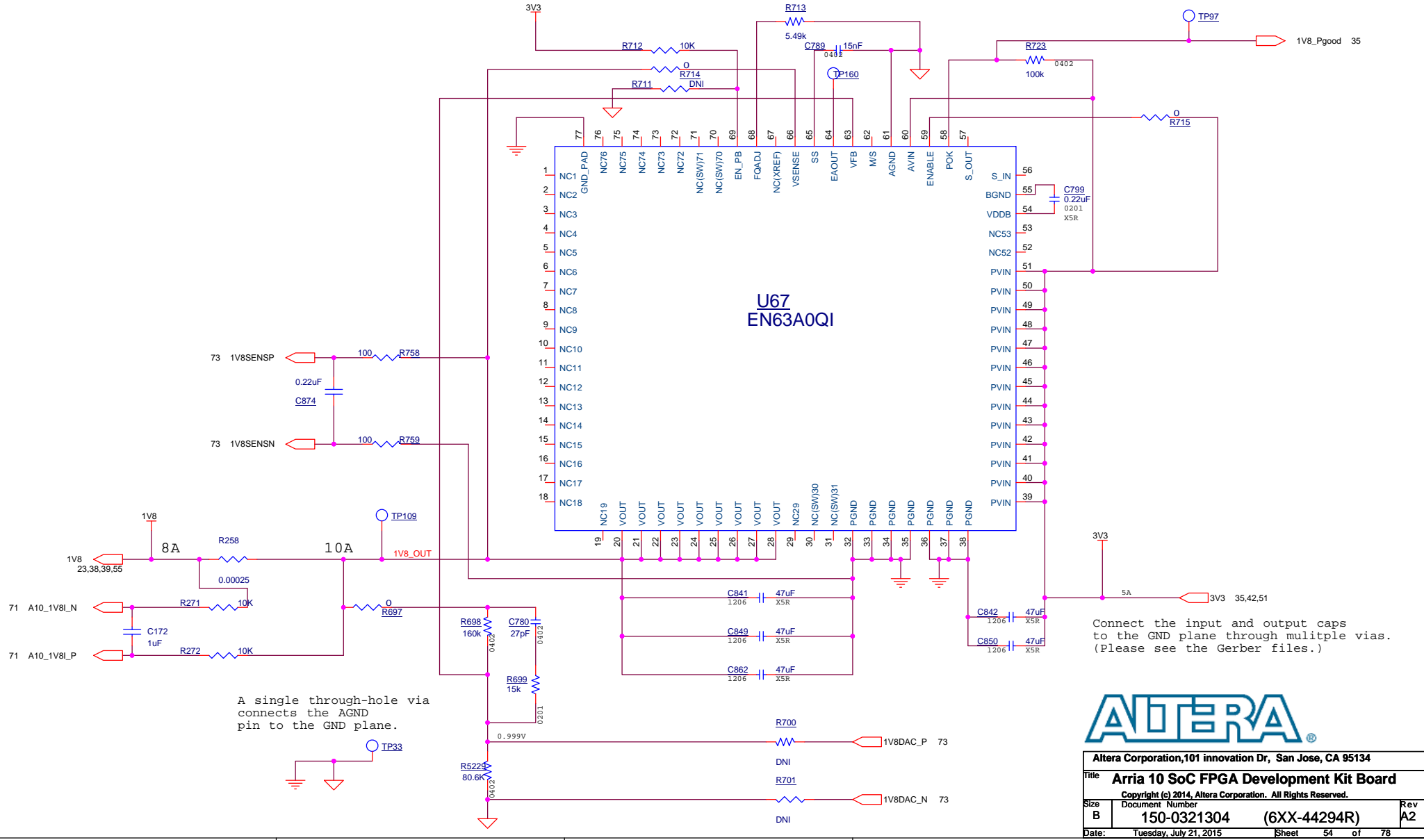


A single through-hole test point connects the AGND pin to the GND plane.



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# 3.3V to 1.8V Converter



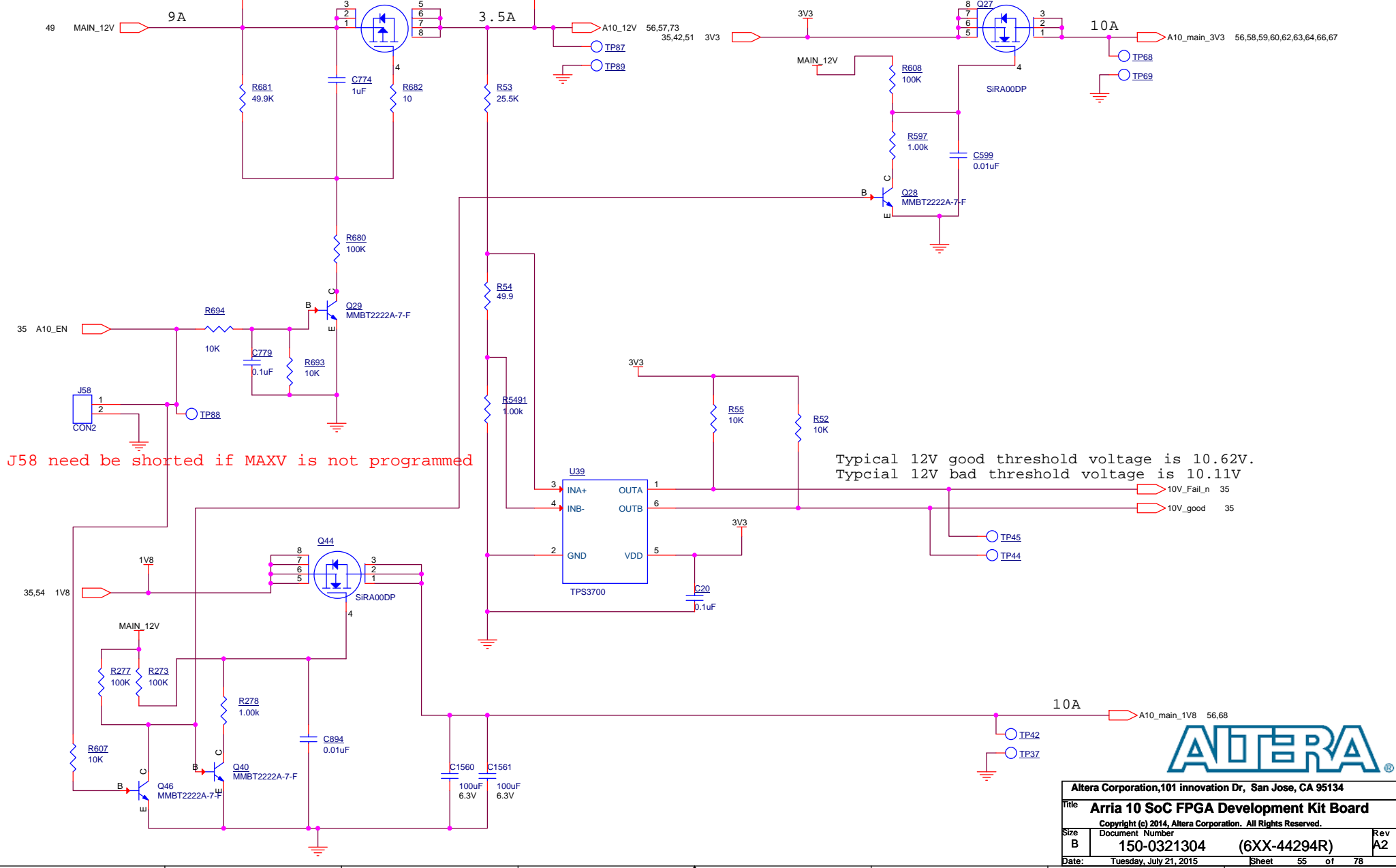
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Connect the input and output caps to the GND plane through multiple vias. (Please see the Gerber files.)

A single through-hole via connects the AGND pin to the GND plane.

# A10 12V,3V3 and 1V8 PMOS Switches



J58 need be shorted if MAXV is not programmed

Typical 12V good threshold voltage is 10.62V.  
 Typical 12V bad threshold voltage is 10.11V

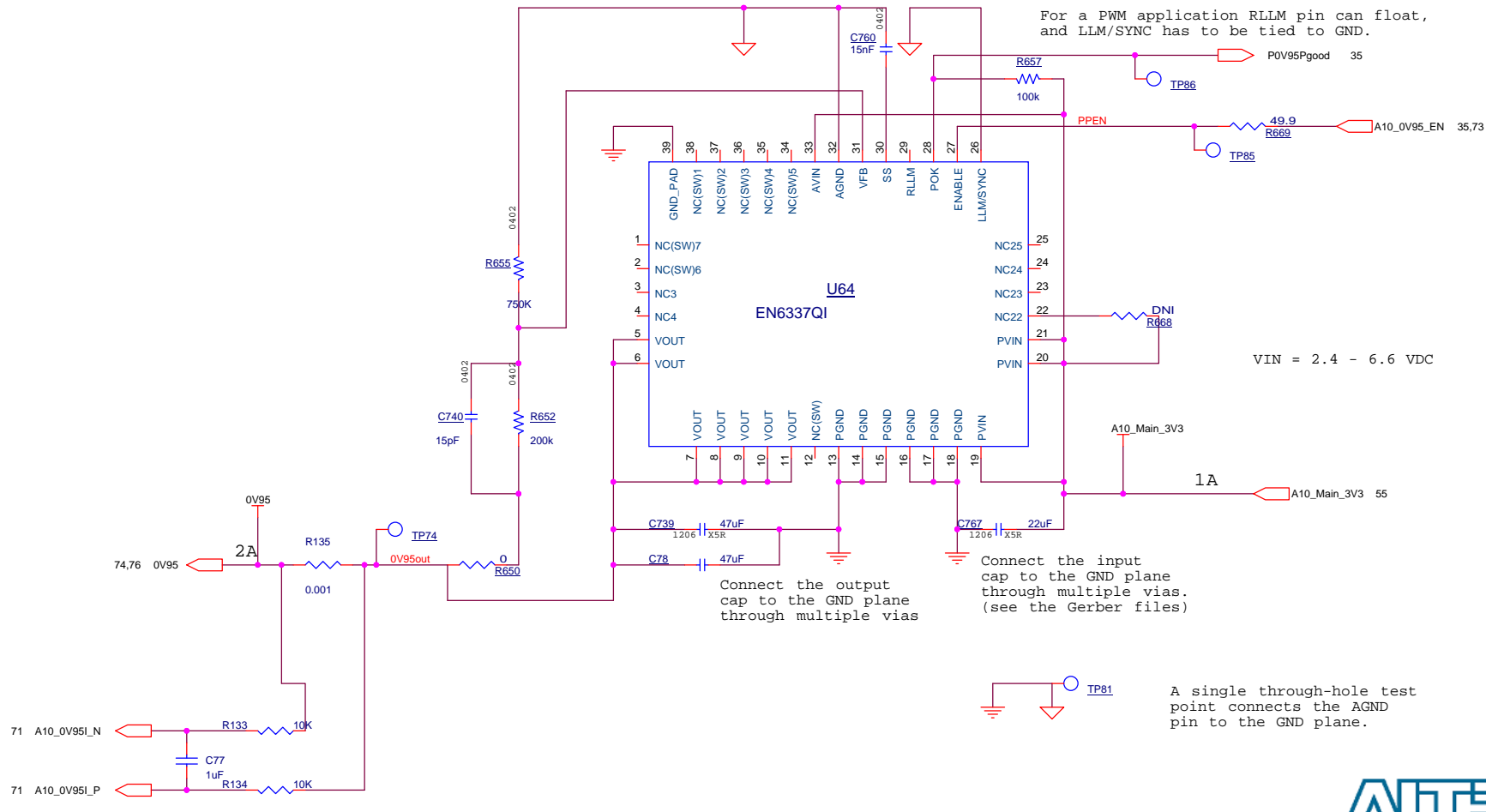


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# 3.3V to 0.95V Converter

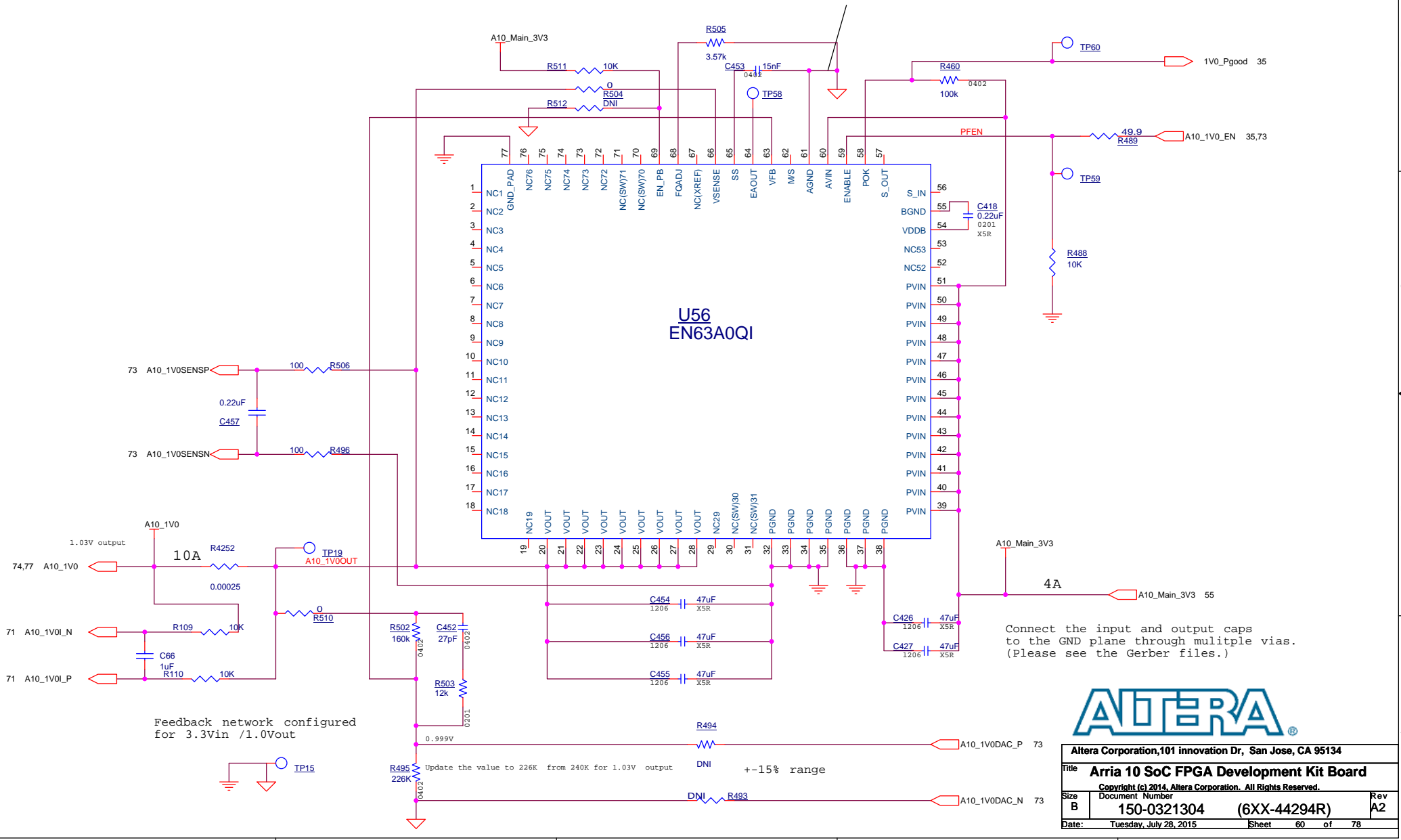


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# 3.3V to 1.0V Converter

A single through-hole via connects the AGND pin to the GND plane.



Connect the input and output caps to the GND plane through multiple vias. (Please see the Gerber files.)



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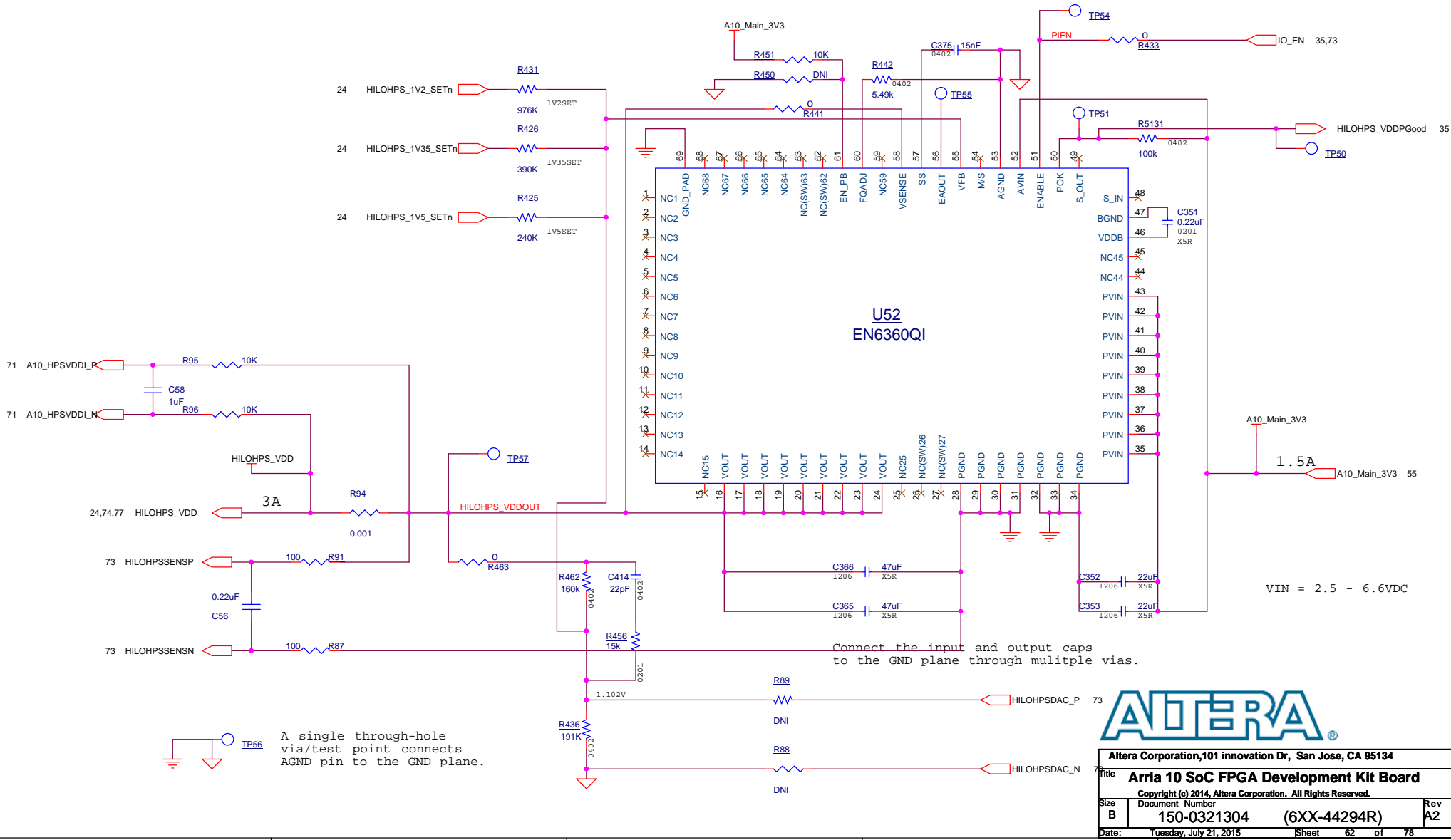
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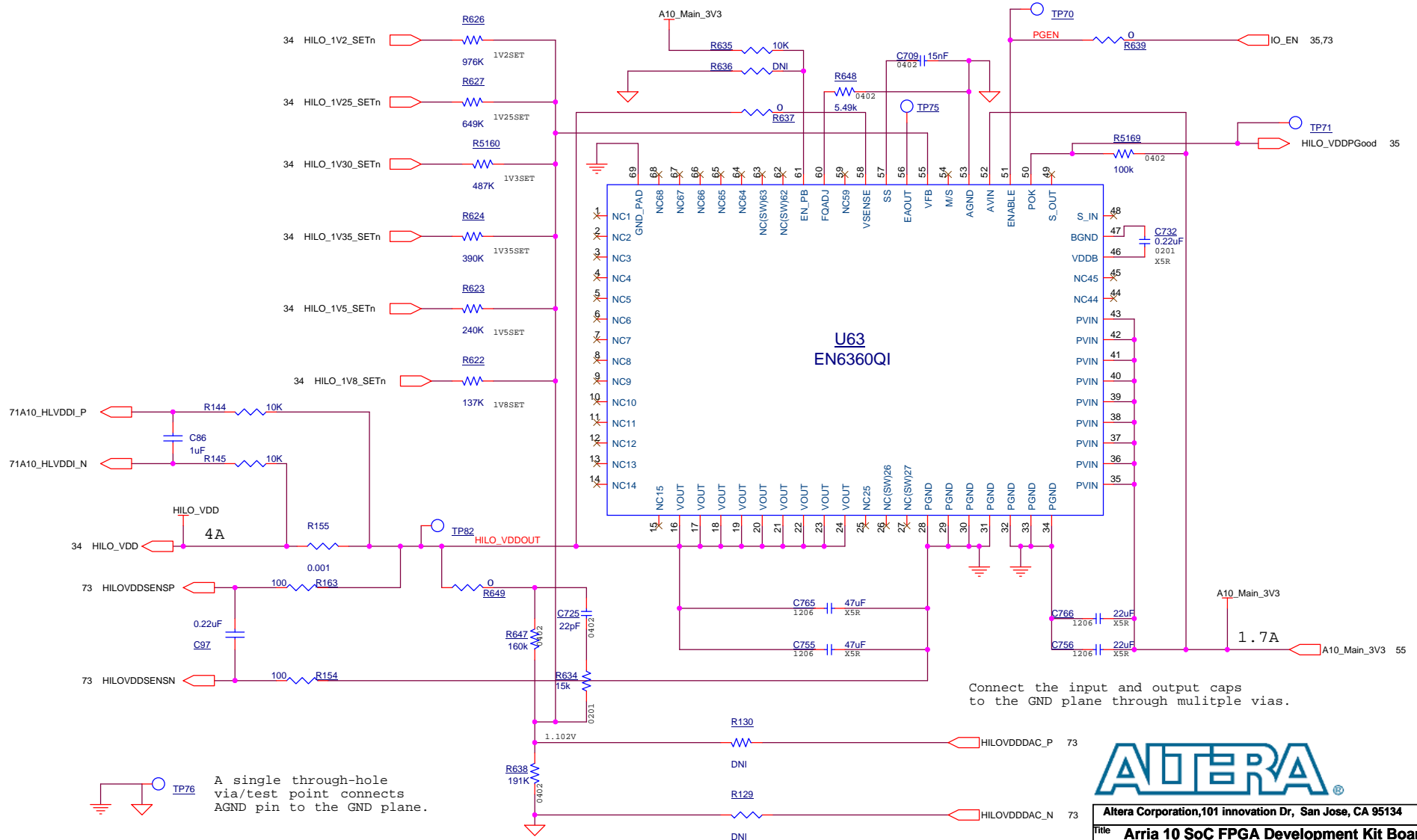
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# 3.3V to HPS HILO VDD converter



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# 3.3V to HILO VDD converter



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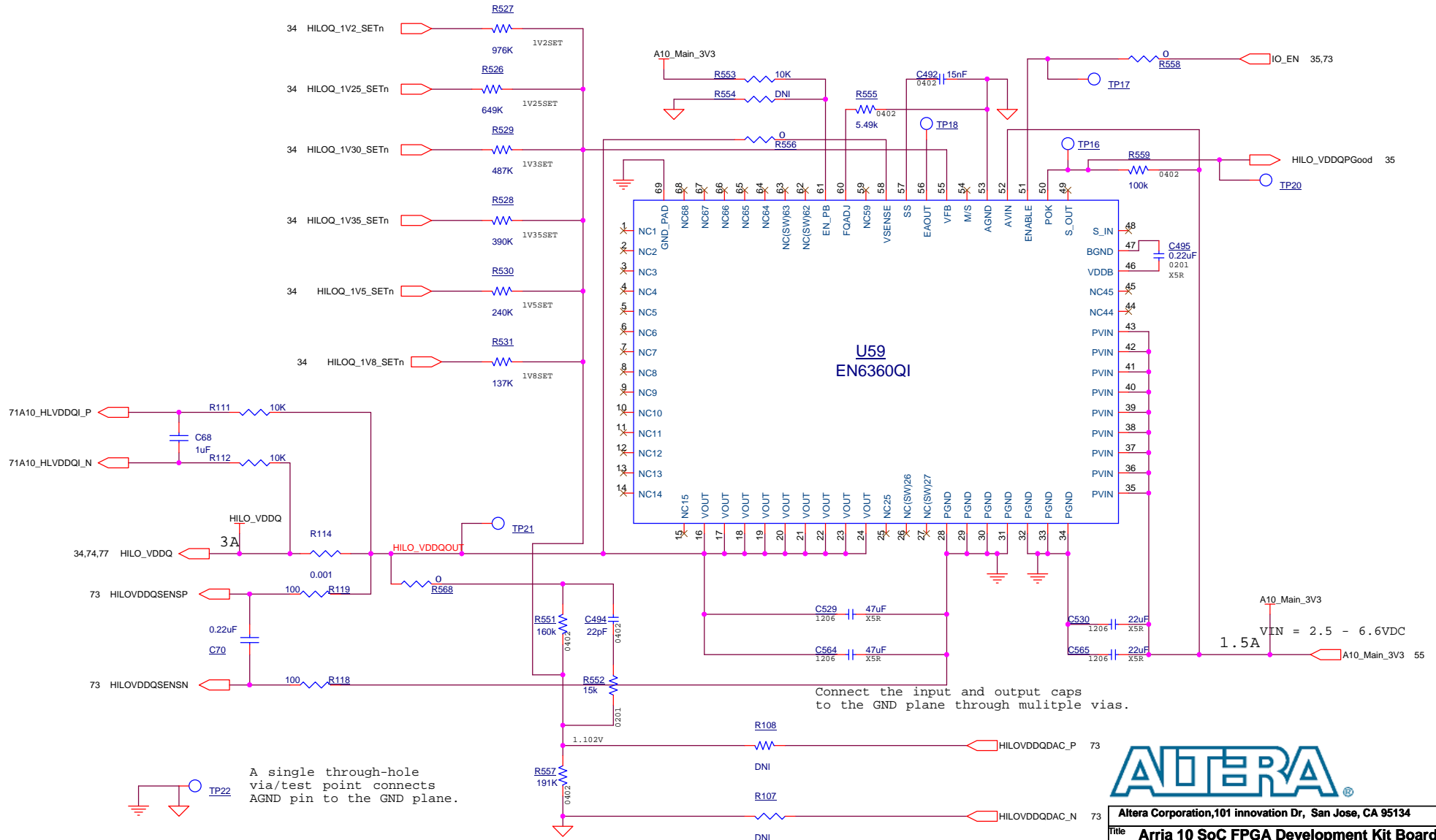
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# 3.3V to HILO VDDQ converter



TP22  
A single through-hole via/test point connects AGND pin to the GND plane.

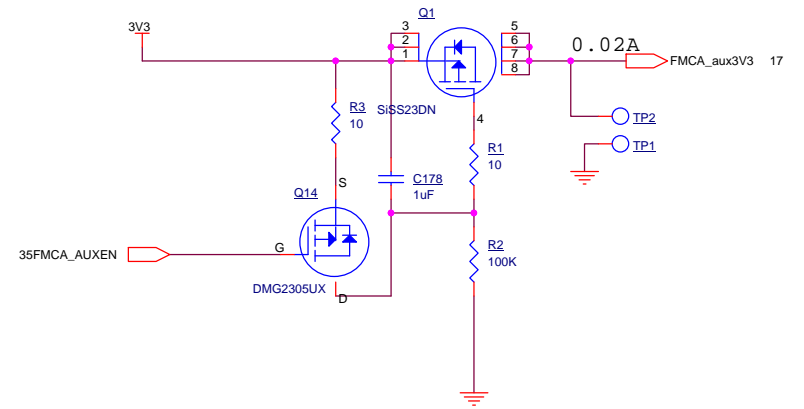
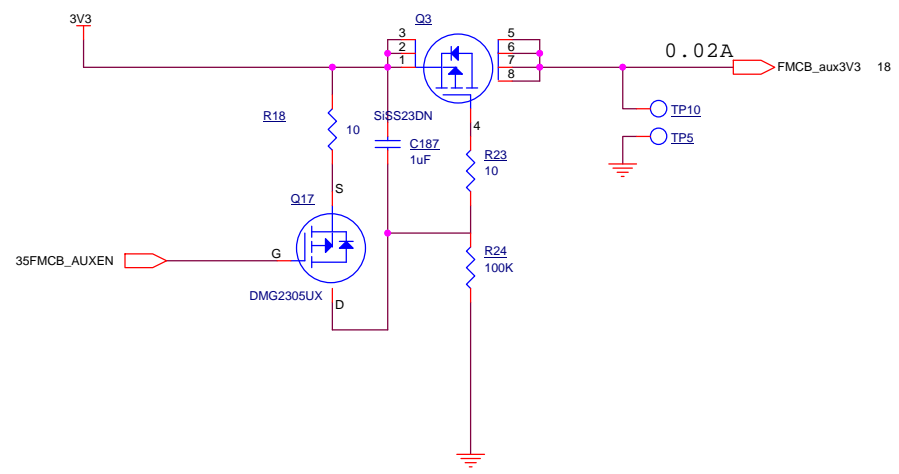
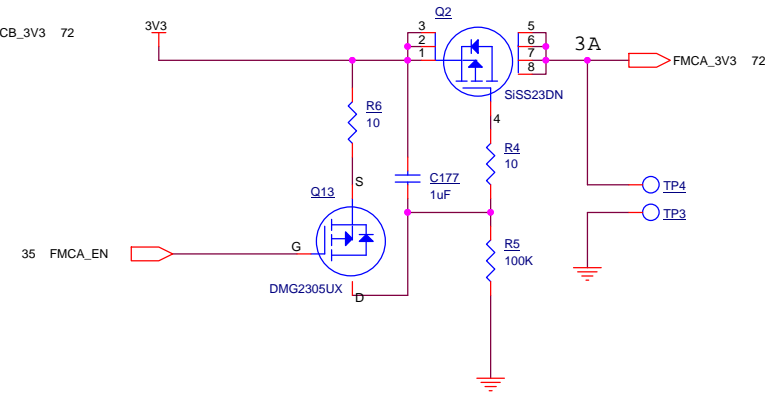
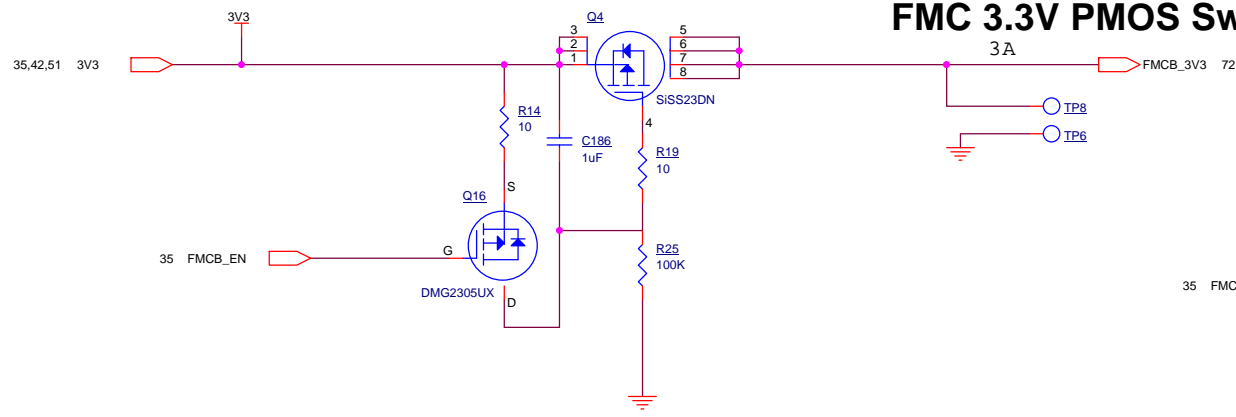
Connect the input and output caps to the GND plane through multiple vias.



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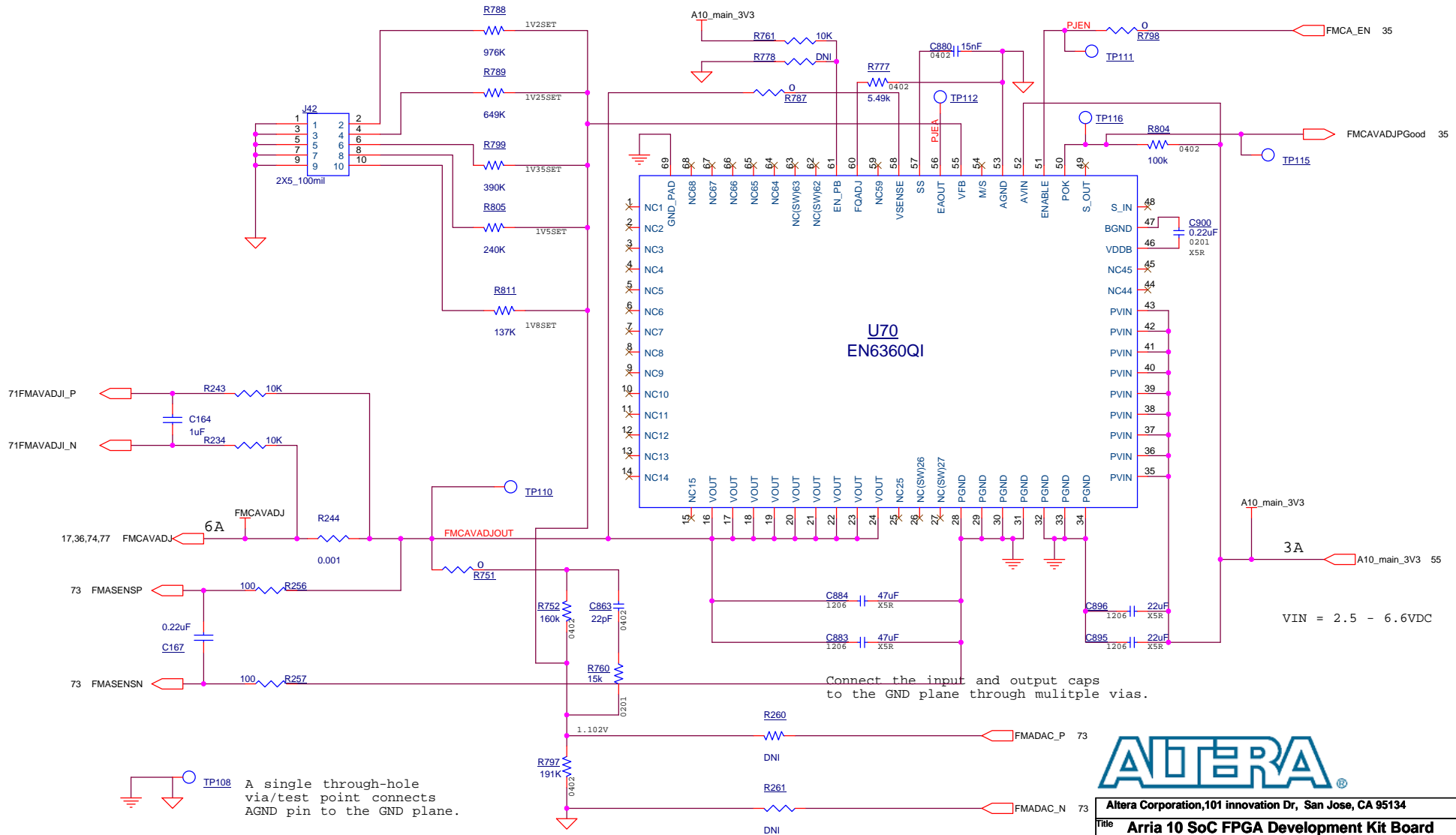
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# FMC 3.3V PMOS Switches



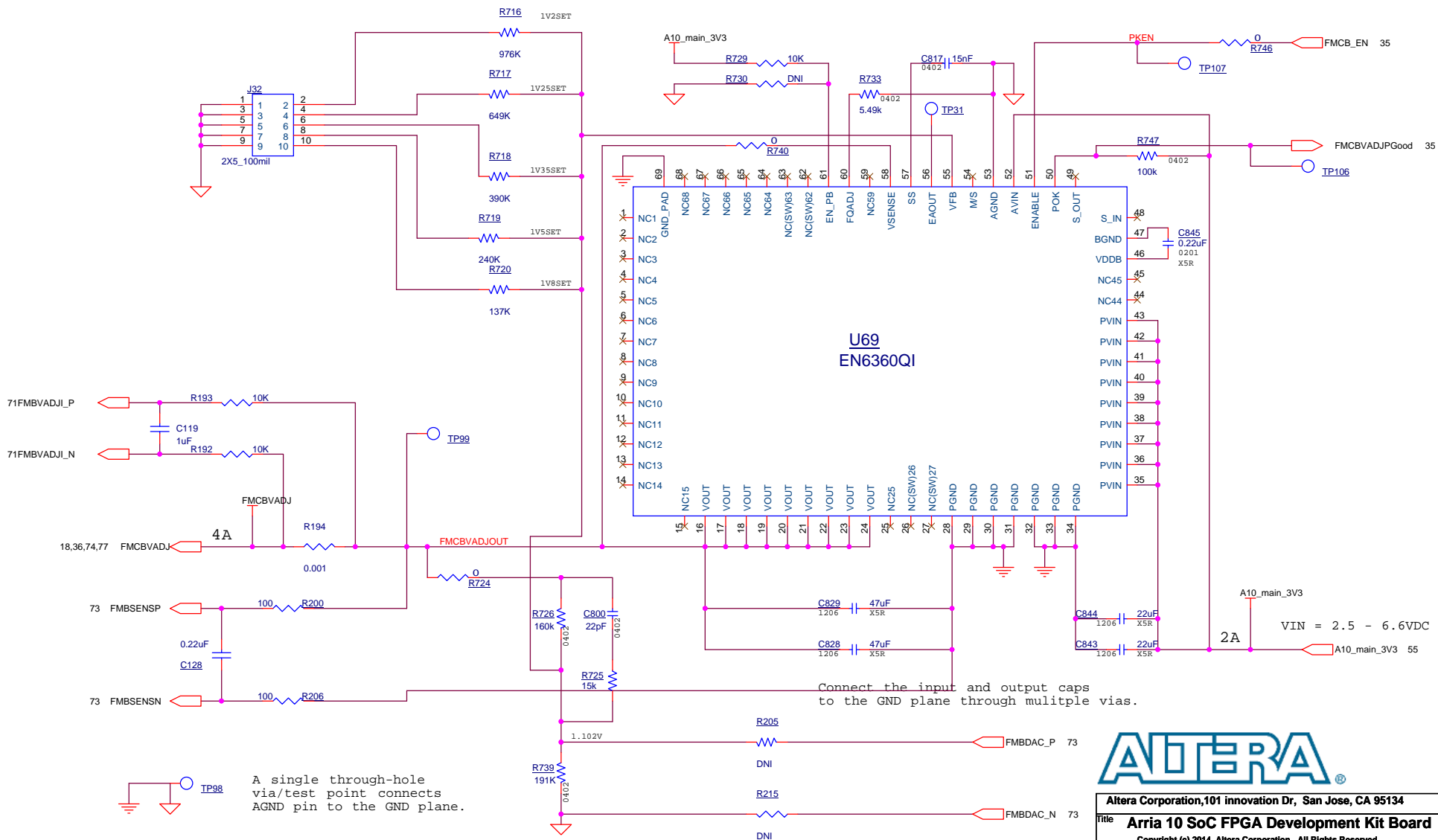
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# 3.3V to FMC A VADJ converter



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# 3.3V to FMC B VADJ converter



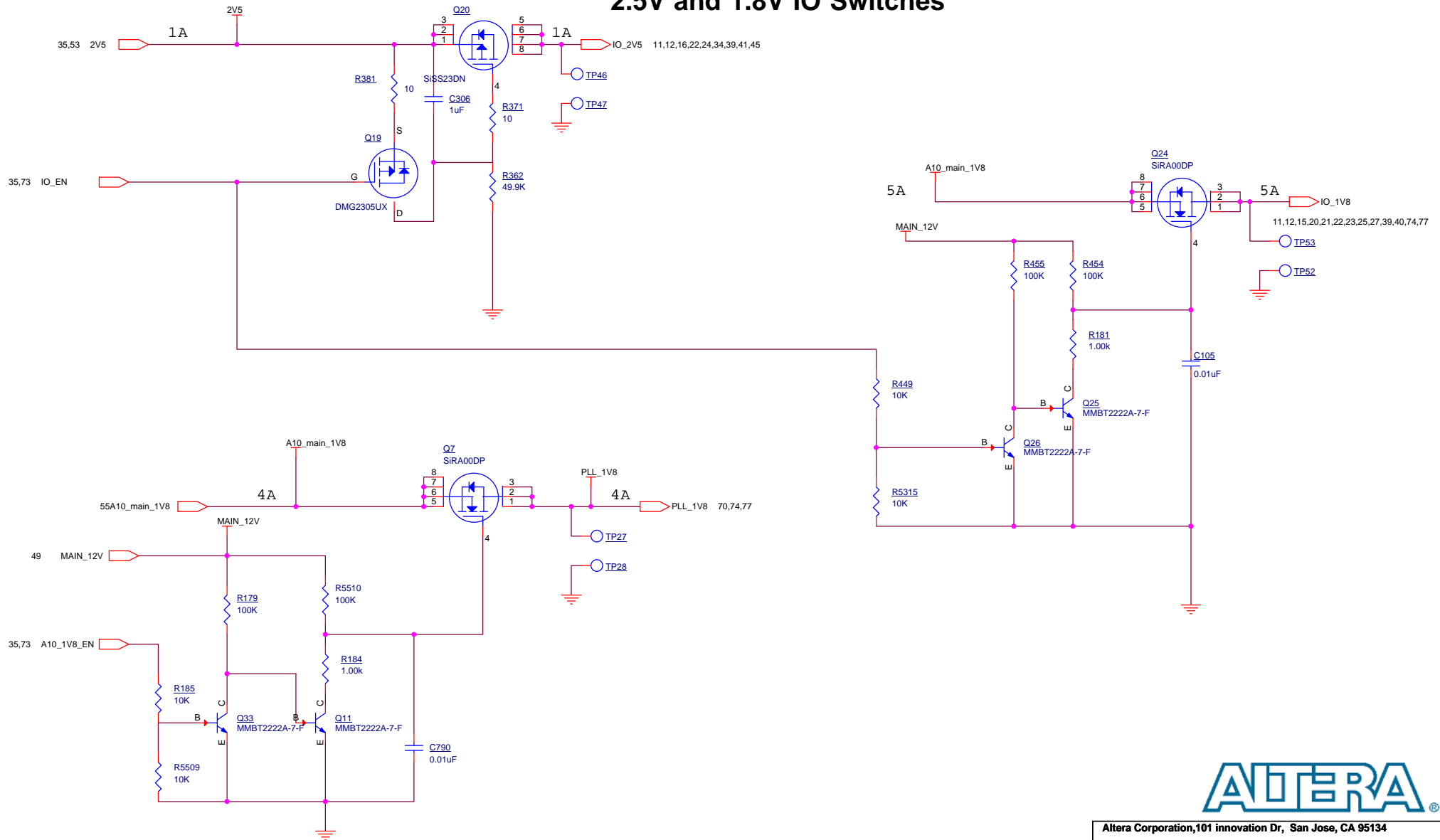
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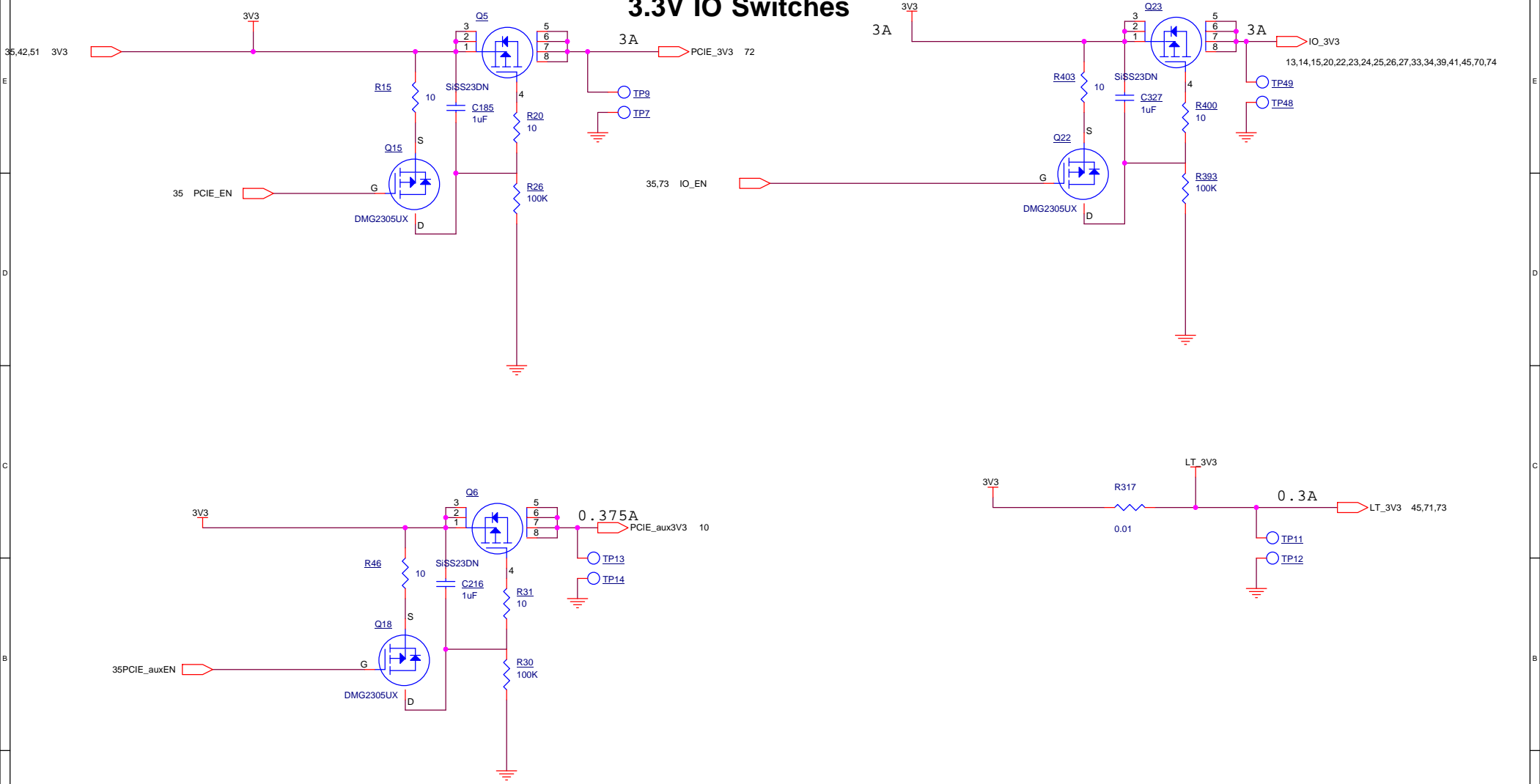
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# 2.5V and 1.8V IO Switches



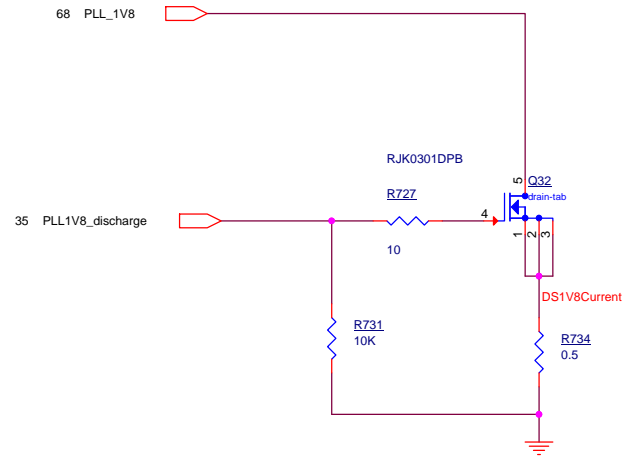
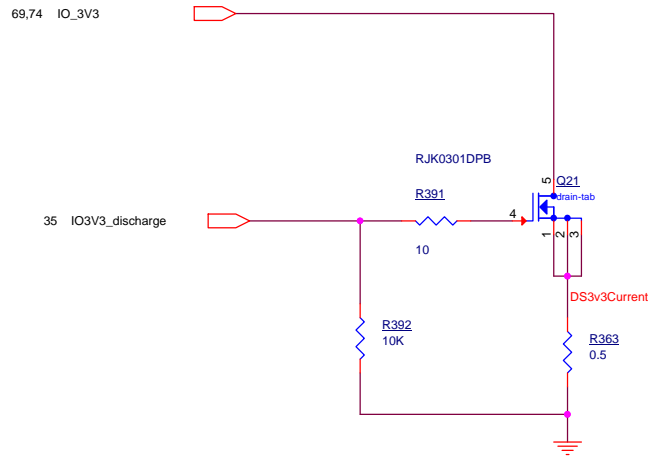
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# 3.3V IO Switches



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# 3.3V and 1.8V Discharge Load

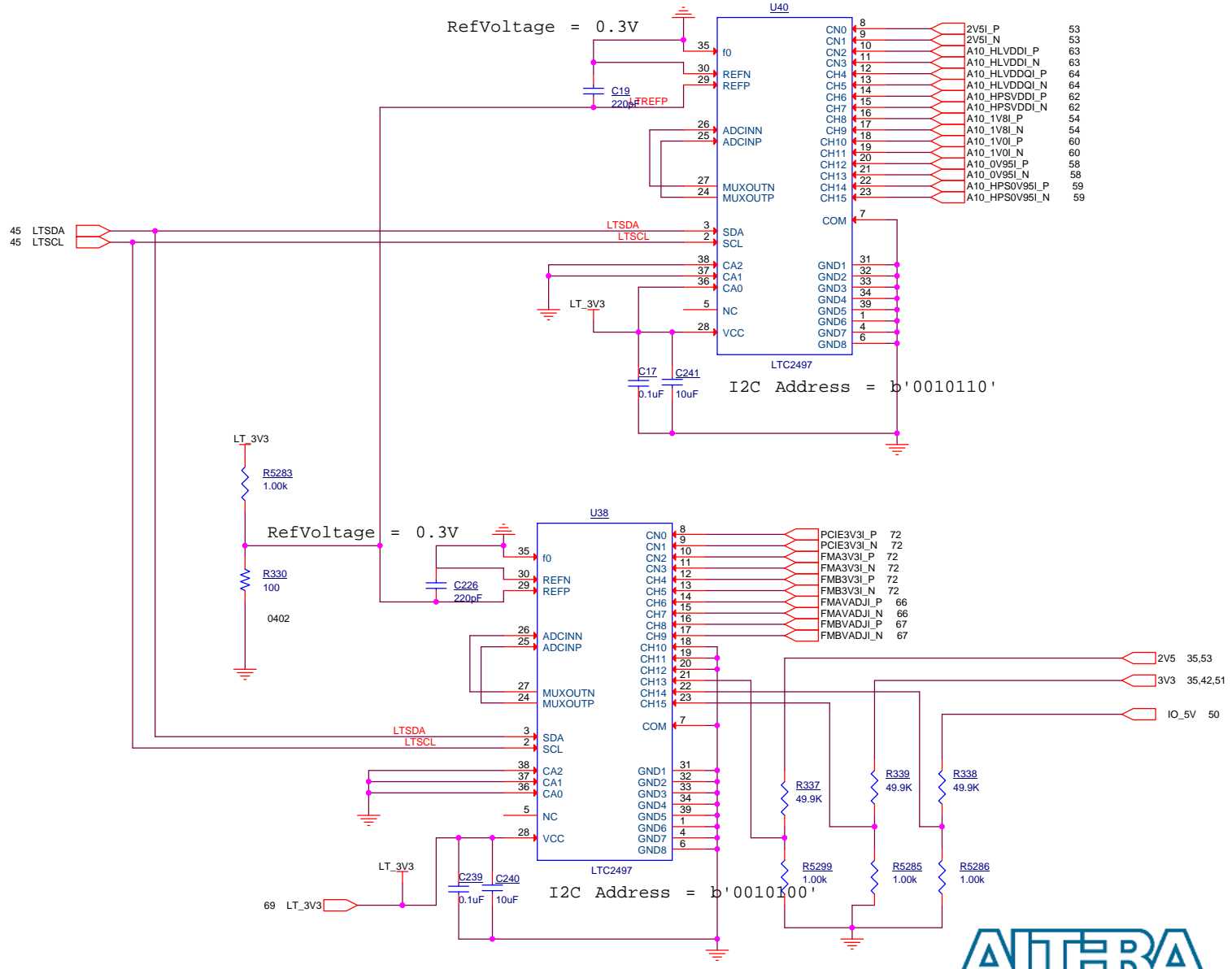


50us Discharge time



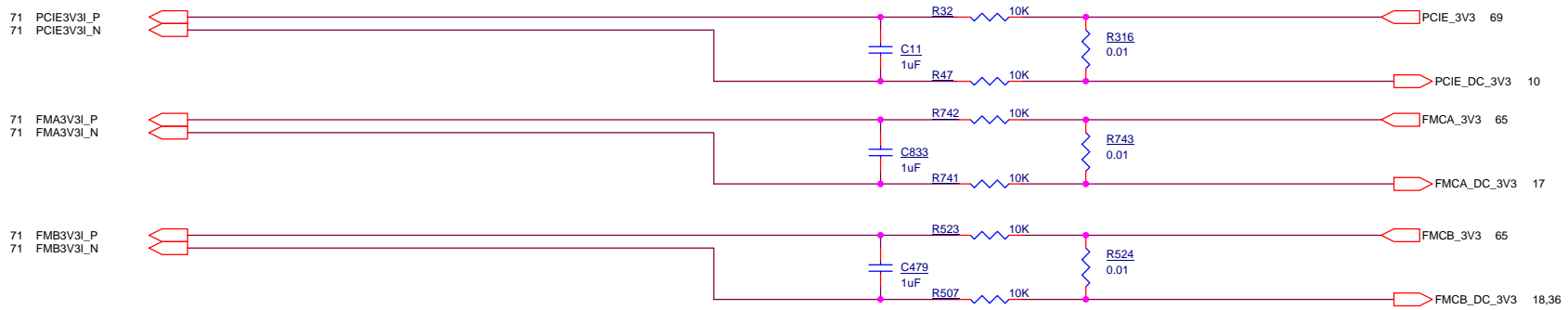
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# I2C Current ADC (A)



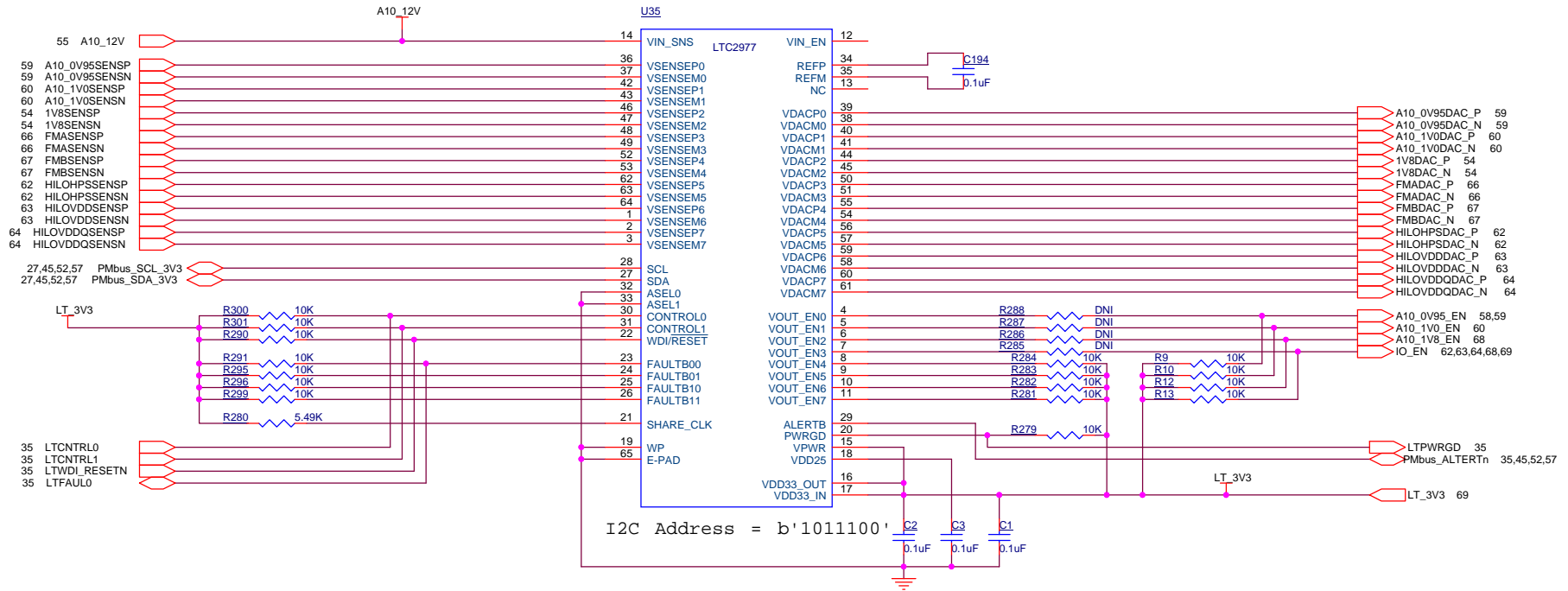
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# User DC card 3.3V Current Sensors



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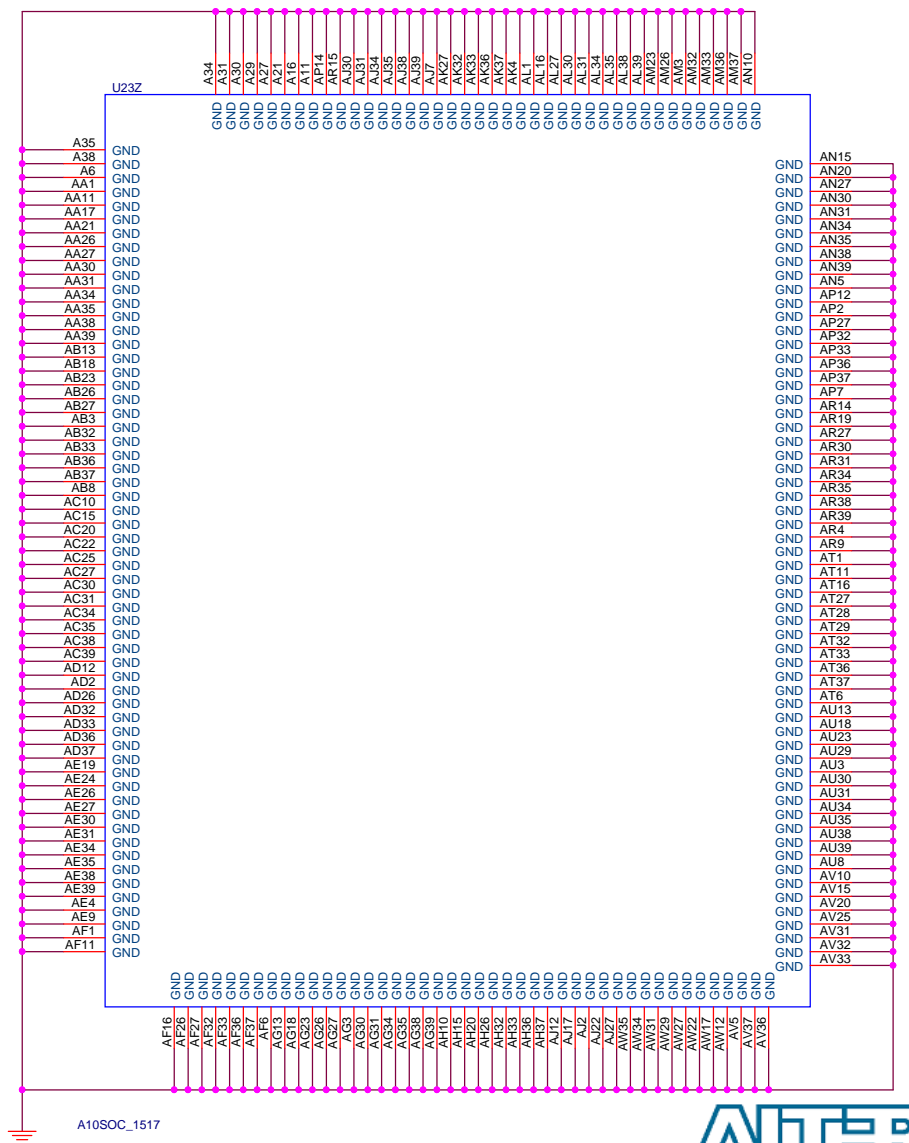
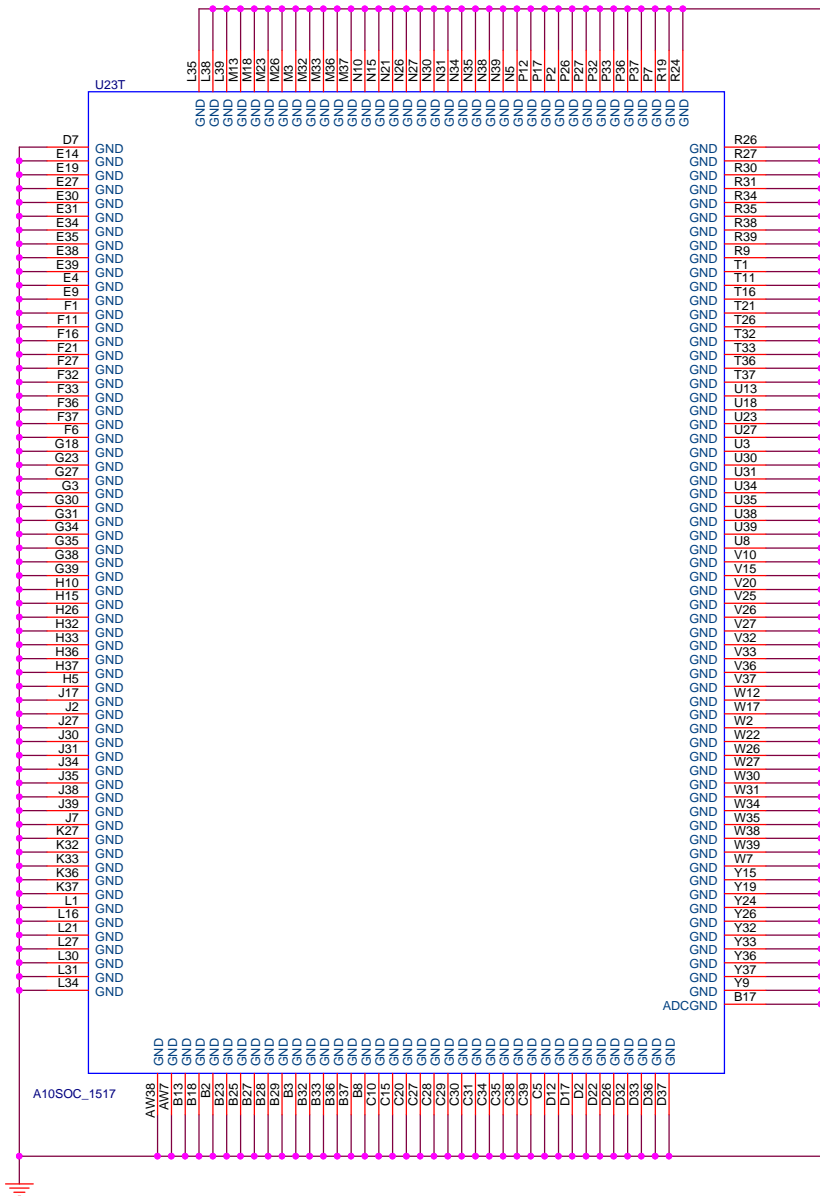
# I2C Power ADC, DAC Controller



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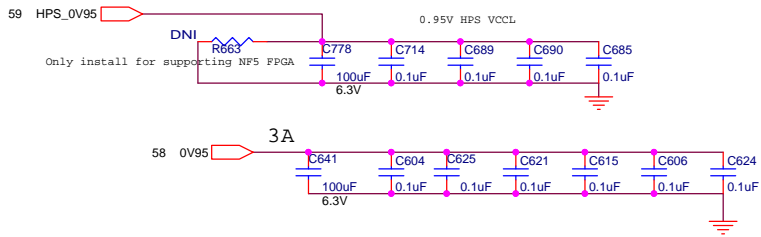
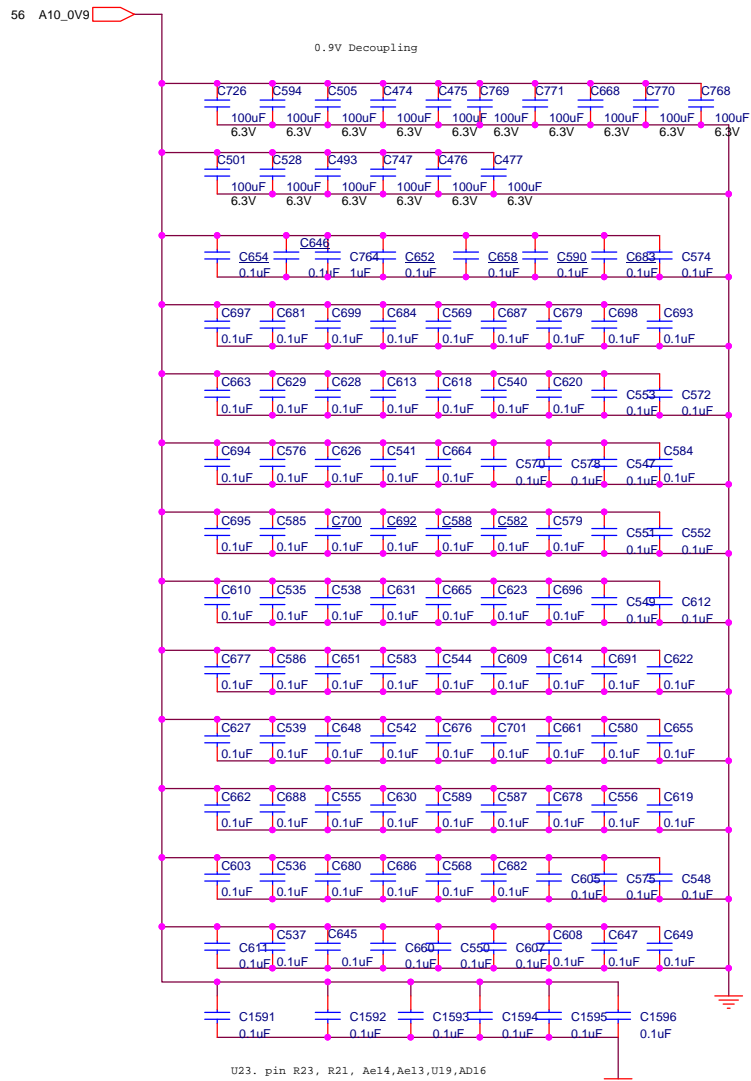
# Arria 10 Ground Connections



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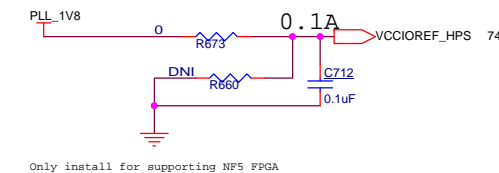
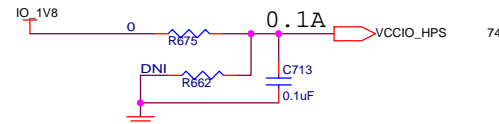
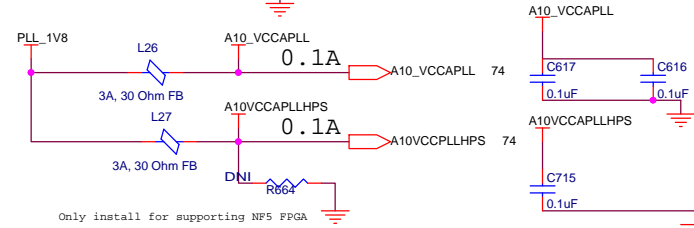
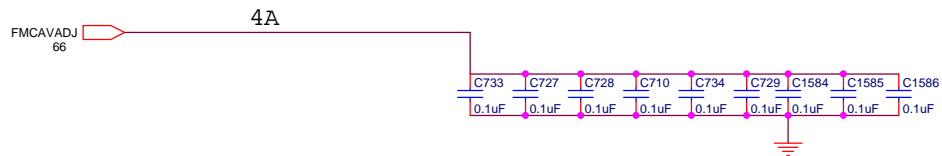
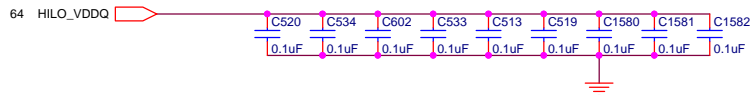
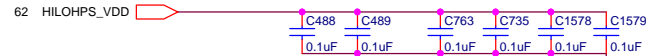
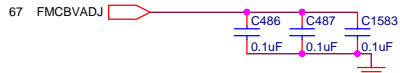
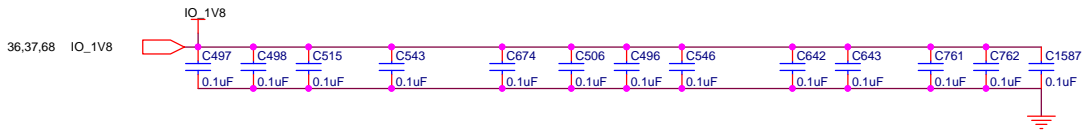
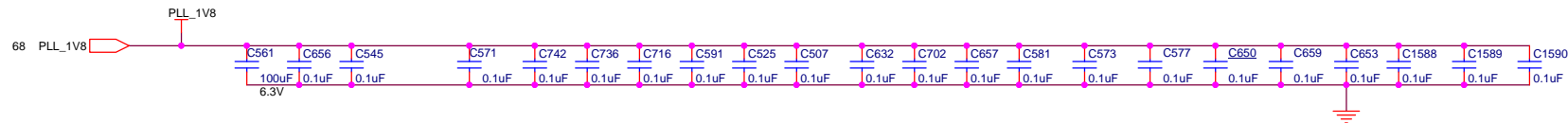
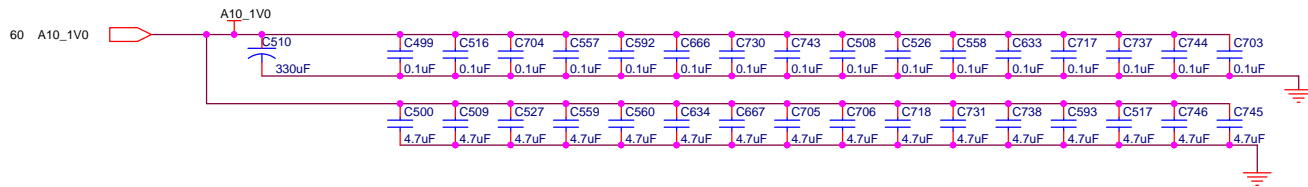
# Core Power Decoupling

0.95V HPS is for boost mode



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# IO Power Decoupling



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