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THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG DEVICES.

RELAY CONTROL CHART

CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR

JUMPER TABLE

JP#	ON	OFF
1		
2		
3		
4		
5		

* SEE ASSEMBLY INSTRUCTIONS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

P.O SPEC.	BK/BD SPEC.	SOCKET OEM	OEM PART#	HANDLER

	DATE
TEMPLATE ENGINEER -	
HARDWARE SERVICES Pat Sheahan	18JAN2018
HARDWARE SYSTEMS -	
TEST ENGINEER -	
COMPONENT ENGINEER -	
TEST PROCESS -	
HARDWARE RELEASE -	
DESIGNER -	
PTD ENGINEER Lluis Beltran Gil	18JAN2018
CHECKER -	

SCHEMATIC

ANALOG DEVICES

HW TYPE : Customer Evaluation
EVAL-AD7606BFMCZ

MASTER PROJECT TEMPLATE TBD
TESTER TEMPLATE N/A

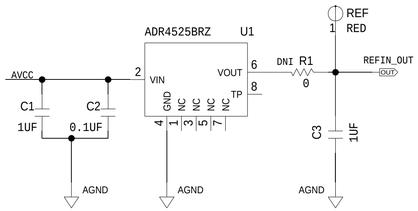
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS X.XX +-0.010 X.XXX +-0.005
FRACTIONS +-1/32
ANGLES +-2

DRAWING NO. 02-047053
REV. G

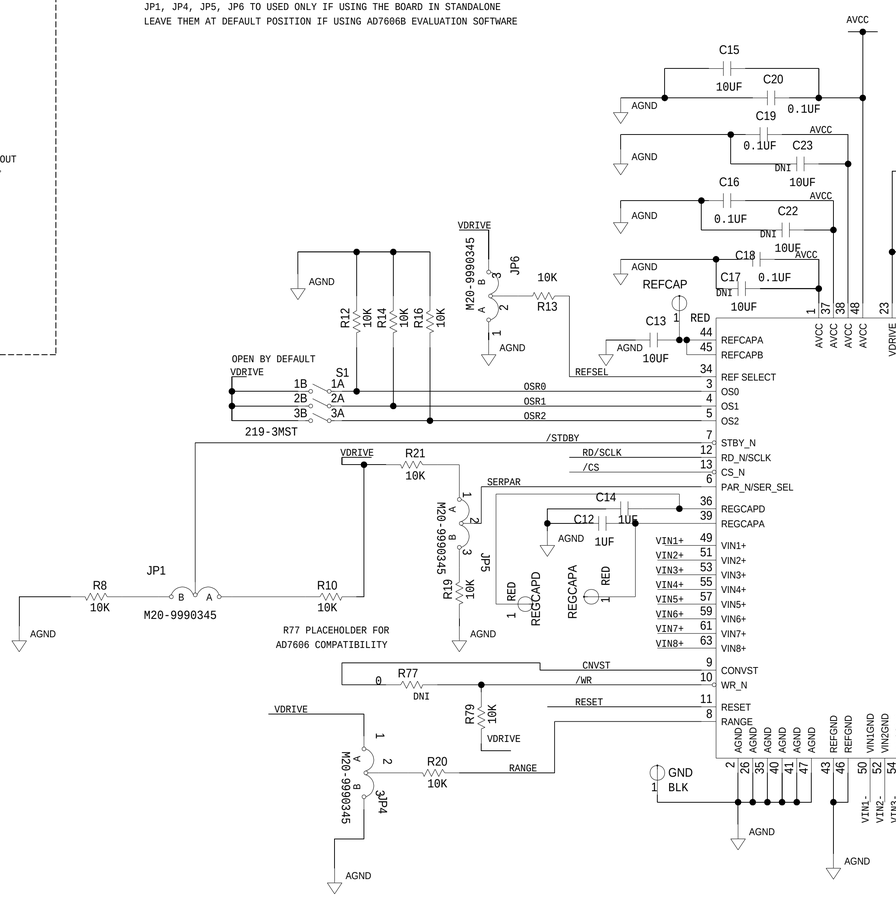
SIZE D | SCALE 1:1 | CODE ID NO. CodeID | SHEET 1 OF 4

EXTERNAL REFERENCE

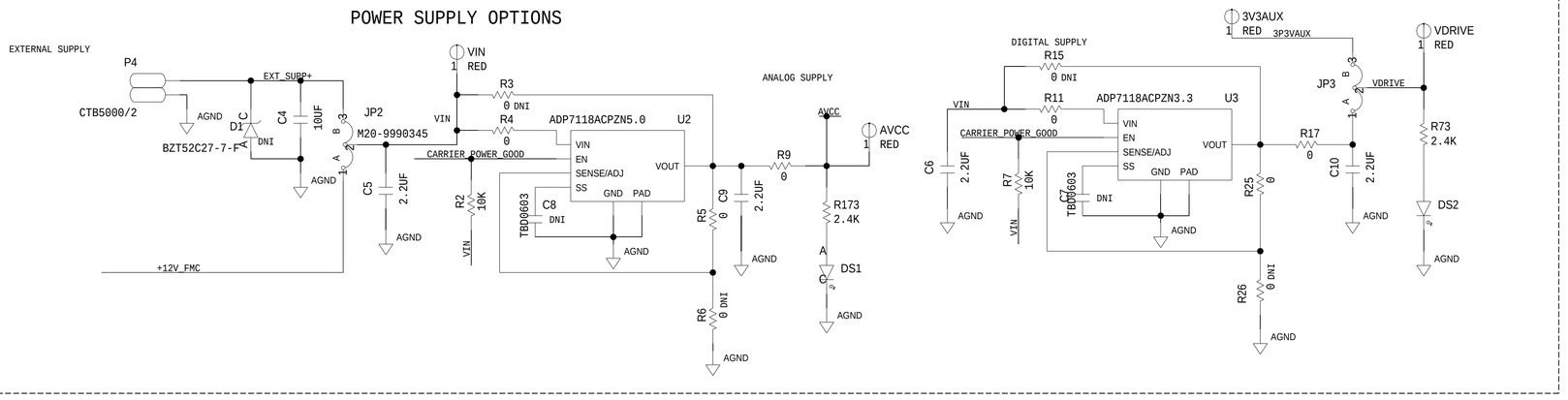
POPULATE R1 IN ORDER TO USE THE EXTERNAL REFERENCE

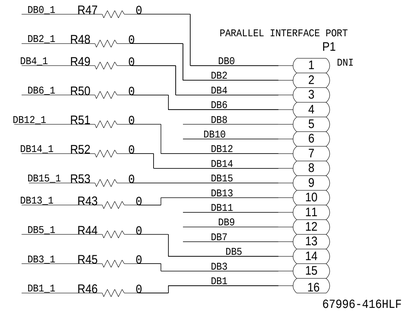


JP1, JP4, JP5, JP6 TO USED ONLY IF USING THE BOARD IN STANDALONE
LEAVE THEM AT DEFAULT POSITION IF USING AD7606B EVALUATION SOFTWARE



POWER SUPPLY OPTIONS





REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANALOG DEVICES	SCHEMATIC
	HW TYPE : Customer Evaluation EVAL-AD7606BFMCZ
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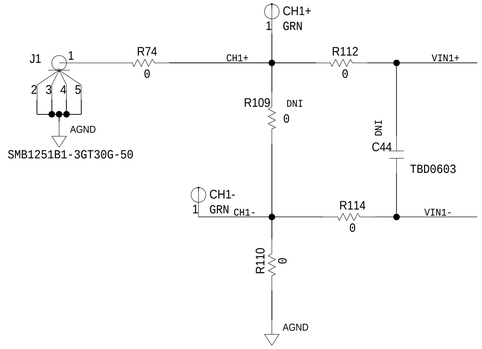
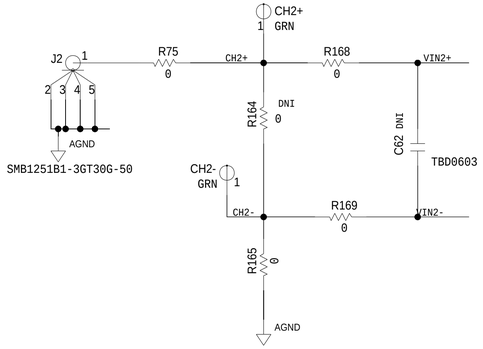
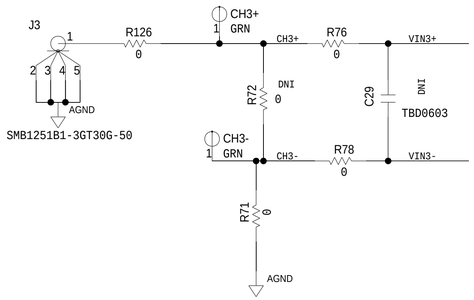
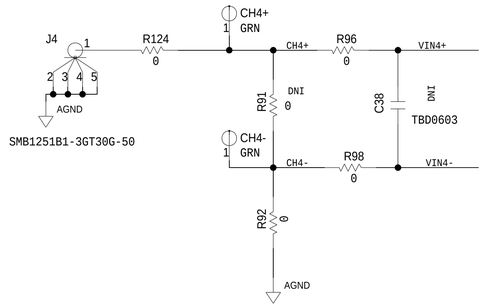
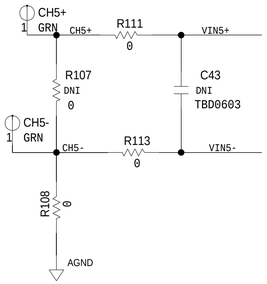
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

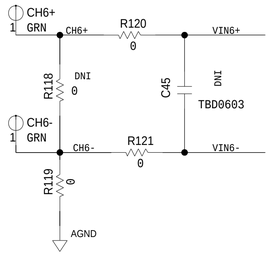


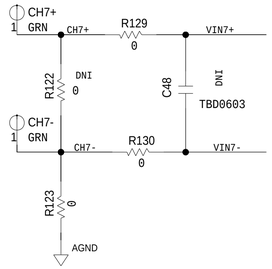


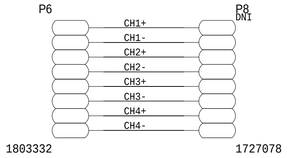


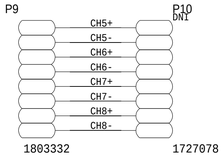


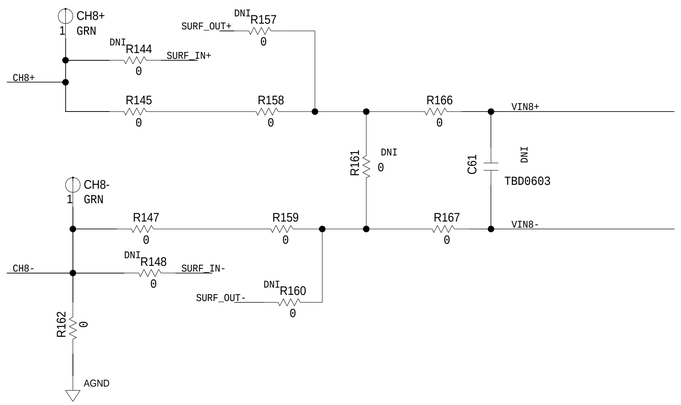


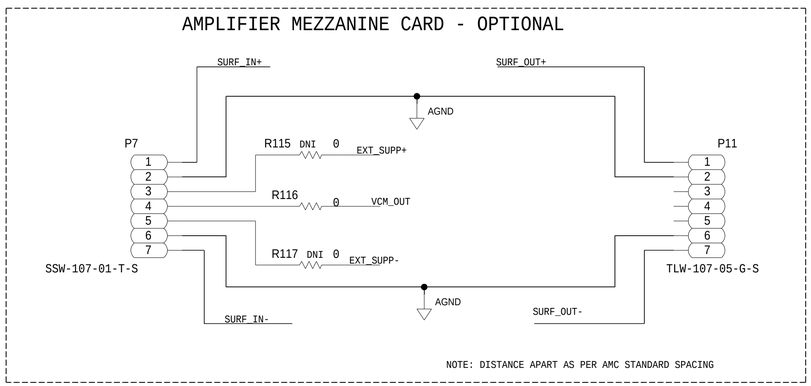












ANALOG DEVICES

SCHEMATIC

HW TYPE : Customer Evaluation
EVAL-AD7606BFMCZ

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02-047053	G

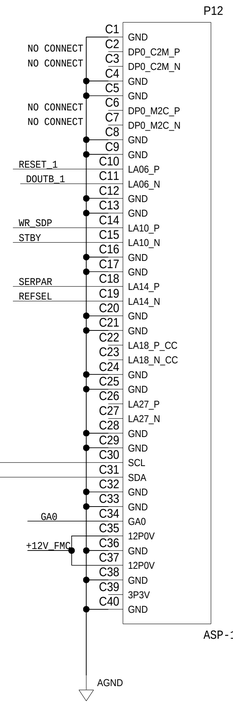
PTD ENGINEER	SIZE	SCALE	SHEET
Lluis Beltran Gil	D	1:1	3 OF 4

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

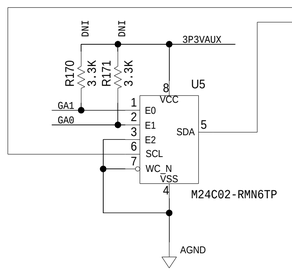
FPGA FMC CONNECTIONS

LIST OF FMC-LPC CONNECTOR PINS THAT
ARE NOT CONNECTED ON THE SDP-H1:

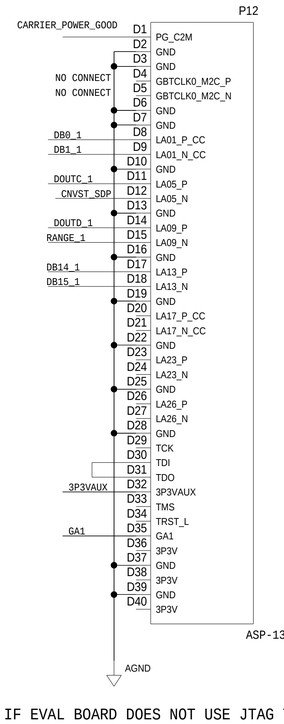
C2 (DP0_C2M_P)
C3 (DP0_C2M_N)
C6 (DP0_M2C_P)
C7 (DP0_M2C_N)
D4 (GBTCLK0_M2C_P)
D5 (GBTCLK0_M2C_N)
H1 (VREF_A_M2C)



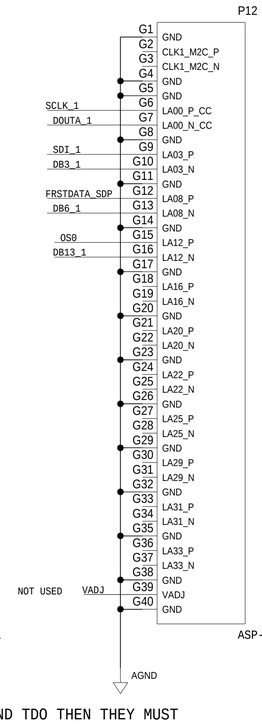
EEPROM

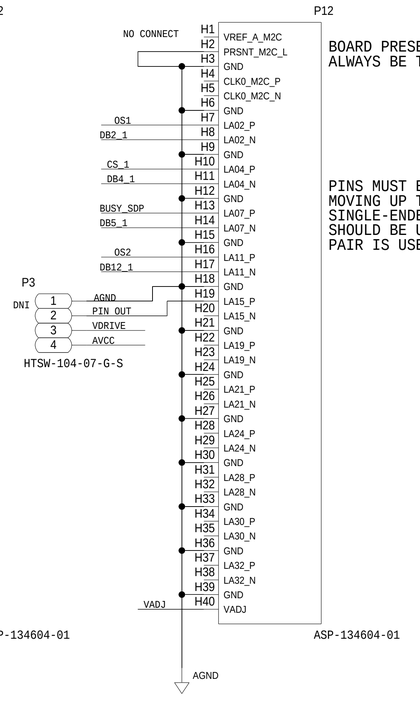


EEPROM REQUIRED IN VITA57.1 STANDARD.
I2C LINE PULL-UP RESISTORS ON FPGA BOARD.
I2C ADDRESS SET BY CONTROLLER BOARD.



IF EVAL BOARD DOES NOT USE JTAG TDI AND TDO THEN THEY MUST
BE SHORTED TOGETHER (AS SHOWN) SO AS NOT TO BREAK JTAG CHAIN





BOARD PRESENT PIN (H2) MUST
ALWAYS BE TIED TO GROUND

PINS MUST BE ASSIGNED STARTING WITH LA00 AND
MOVING UP THE LA BUS UNTIL IT IS FULL. WHEN
SINGLE-ENDED SIGNALING IS USED, THE _P LINE
SHOULD BE USED BEFORE THE _N LINE OF THE SAME
PAIR IS USED.

POWER SUPPLIES:
12P0V. 1A MAX CURRENT LIMIT
3P3V. 3A MAX CURRENT LIMIT
VADJ. 2A MAX CURRENT LIMIT. 1.2V TO 3.3V.

ANALOG DEVICES

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DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02-047053	G
PTD ENGINEER: Lluis Beltran Gil	SIZE: D / SCALE: 1:1	SHEET 4 OF 4